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Novel Reduced Switches Single-Phase to Three-Phase On-line Uninterruptible Power Supply

Mehrnaz Sharifian[1] Mehdi Niroomand[2]

Abstract—This paper describes design considerations and performance analysis of a novel on-line single-phase to three-phase uninterruptible power supply (UPS) with reduced number of switches. The proposed topology uses only 5 active switches reducing the cost of the system compared to the traditional 10-switch topologies. The proposed UPS consists of a single-phase rectifier/charger, a two-leg/three-phase inverter connected to load, battery bank, DC link capacitor and an AC inductor. Detailed circuit operation and analysis as well as simulation results are also presented to verify its feasibility.

Keywords-Uninterruptible Power Supply (UPS); Single-Phase to Three-Phase Conversion; Reduced Switches

I. INTRODUCTION

Uninterruptible Power Supplies (UPS's) are nowadays indispensable equipment in supplying power to critical and sensitive loads. They protect sensitive loads against many existing disturbances in utility network like voltage variations, transients and harmonics. Applications of UPS systems include medical facilities, life supporting systems, data centers, emergency equipment, telecommunications and industrial processing systems.

Ideally, a UPS should deliver clean and uninterrupted power to the load, and at the same time draw sinusoidal, near unity power factor current from input supply. Additionally, static UPS's must be able to switch between utility and storage batteries as alternate energy sources. This switching must take place in zero or minimum time in order to avoid any malfunctioning of the supplied equipment. Other specifications like high reliability, high efficiency, low EMI and acoustic noise, electric isolation, low maintenance, low cost, weight and size must be also considered in a high performance UPS [1].

IEC-62040-3 standard classifies UPS's as passive-standby, line-interactive and double-conversion (on-line UPS). Each topology has its own characteristics and is used based on the load requirements and the severity and type of network disturbances [2].

The main advantages of a passive-standby UPS are its design, low cost and small size. The line conditioning is passive which makes this topology fairly robust. On the other hand, rather long switching time between standby and backup modes is the main disadvantage of this topology.

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The line-interactive topology has simple design, fairly high reliability and lower cost, and thus is becoming more attractive as compared to the double-conversion solutions. Since there is just a single stage conversion in this topology, the efficiency is inherently higher than that of the double-conversion UPS. The main disadvantage is the fact that there is no output voltage conditioning during normal mode because the inverter is not connected in series with the load [3], [4].

The double-conversion or on-line topology is considered as the superior topology in performance, and is widely used as standard solution for protecting sensitive loads. However, it has lower efficiency as compared to other topologies due to two conversion stages in its structure. In other words, power flow through the rectifier and inverter even during the standby mode means higher power losses and lower efficiency compared to passive-standby and line-interactive UPS systems.

Another important feature of the online topology is the decoupling of the input from the output, which allows converting single-phase to three-phase UPS [5].

In view of the machine efficiency, power factor, and torque ripples, a three-phase induction motor is preferable to a single-phase induction motor. Therefore, it is desirable to replace the single-phase induction motor drives by the three phase induction motor drives .Even if the distribution of electric power is typically three phase, where only a single-phase utility is available, a single-phase-to-three-phase power converter system is required to feed the three-phase induction motor drives. In rural electric systems, the cost of bringing three-phase power to a remote location is often high due to high cost for a three-phase extension. Furthermore the rate structure of a three-phase service is higher than that for single-phase service. Therefore, single-phase to three-phase power converters are excellent choices for situations where three-phase power is not available. Sometimes, a specific appliance needs three-phase power, requiring some kind of power conversion [6]. Such converters have a wide range of applications in which a three-phase motor is a main component and the available supply is single-phase. This happens in residential, light industrial, farming, low-power industrial applications and rural areas [7], [8], and [9]. Fig.1 shows a typical 1-phase to 3-phase dual bridge converter topology.

The simplicity of these circuits inherently requires a simple control. However, they suffer from large number of switches and from here high cost. The problem of reduction the cost of converters has been recently attracting the attention of researchers [10]-[12].

Reducing the number of switches brings one of the most significant cost reductions. Another method of cost reduction is replacing active switches, such as MOSFETs, IGBTs and thyristors with diodes. Not only diodes are cheaper than active switches, but there is also cost reduction from eliminating gate drivers for active switches. Replacing active switches with diodes usually complicates circuit topology and reduces degrees of freedom in the control system. Therefore, the control is usually more sophisticated [5].

One way to increase the efficiency of the drive is by reducing its losses. These losses are computed as switching losses and conduction losses. It may also be improved as the number of circuit elements is minimized, because as the number of devices reduces the associated amount of switching reduces and so the losses are minimized. Also too many power switches at the same time reduces the reliability of the power conversion system [13].

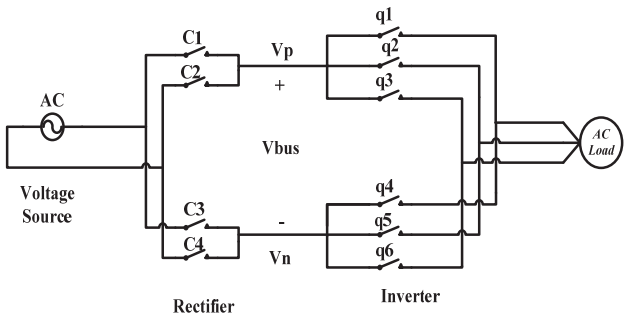

Fig. 1: A typical dual bridge single phase to three phase converter topology.

In this paper, after a brief presentation of several topologies, reduced number of switches is studied. The concept of reducing the cost of converters is applied by using four-switch three-phase DC/AC inverter instead of six switch three-phase DC/AC topology, but with similar functionality. In addition, the cost of the proposed UPS system is reduced further by employing a novel single-phase AC/DC rectifier topology with just one switch and four diodes. Also a balancing control of the neutral voltage in the dc link is applied for the symmetrical output voltage of the DC/AC converter. Finally, simulation results are provided to validate its operation.

II. Steps to Reduce the Switch Number

A. Reduced steps of the AC to AC converters

Considering the conventional AC to AC converter topology was shown in Fig. 1. In general, the ten ideal switches in Fig. 1 requiring, in principle, twenty unidirectional current conducting, bidirectional voltage blocking switches can be implemented in a number of simpler realizations by appropriate assumptions. For example, if Vp is always higher than Vn, the bidirectional switches on the load side can be replaced by uni-directional voltage blocking switches as shown in Fig. 2. In this case, the topology of [14], [15], and [16] is realized.

Fig. 3 shows the equivalent circuit of input side phase. Noting that the switches Spp and Snp can share the same gate drives signal. These two switches can be replaced by one single switch and two clamp diodes. As a result, a 12-switch topology is developed as shown in Fig. 4. [17], [18]. Compared to the 14-switch topology, this circuit possesses the same performance measures such as four-quadrant operation, unity power factor and low harmonic content. The first difference is that, when DC current, i_{dc}, is positive, its conduction losses for the line side switches are higher than the 14-switch topology.

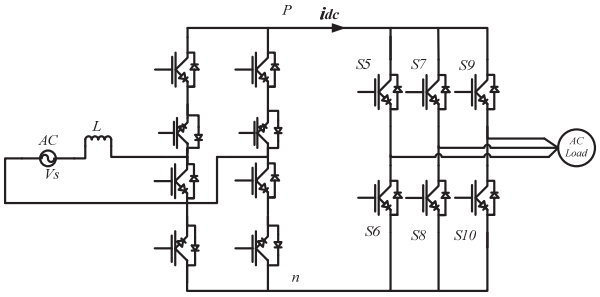

Fig. 2: Topology with 14 uni-directional voltage blocking switches.

If the condition that link current, $i_{dc} > 0$ is guaranteed, the number of switches can be further reduced. If the 12-switch topology in Fig. 4 is analyzed in detail, a 10-switch topology can be derived as presented in Fig. 5.

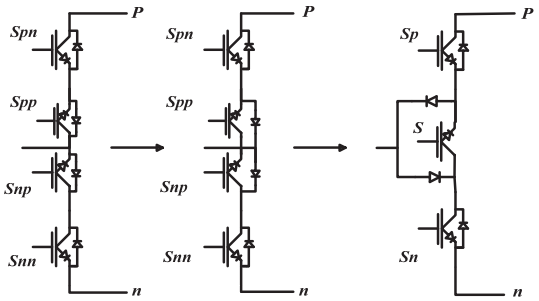

Fig. 3: Steps to reduce the switch number.

From Fig. 4, it can also be determined that no current flows through Sjp and Sjn, (j € a, b) and only the two intermediate switches are conducting. Thus, an 8-switch topology can be obtained as shown in Fig. 6. Generally, both the 8-switch and the 10-switch topologies show the same performance except that the 8-switch topology has somewhat larger conduction losses than the 10-switch topology.

Because an 8-switch topology can only be used when DC Current, i_{dc}, is greater than or equal to zero, the power through that, can only flow from the line side to the load side. In order to ensure positive DC current flow with three-phase sinusoidal output current, it can obtain that the power factor on the load side should always be higher than 0.87. As a result, the application of this topology is somewhat limited but suitable, for example, for permanent magnet motor drives [19].

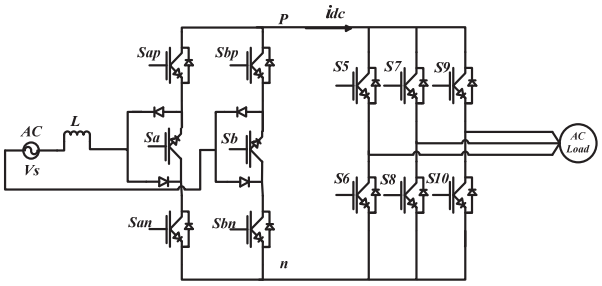

Fig. 4: A Reduction of switch number from 14 to 12.

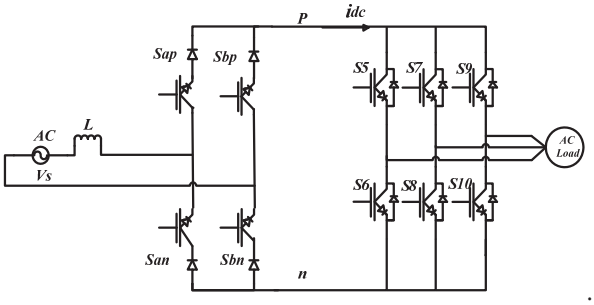

Fig. 5: 10-switch topology.

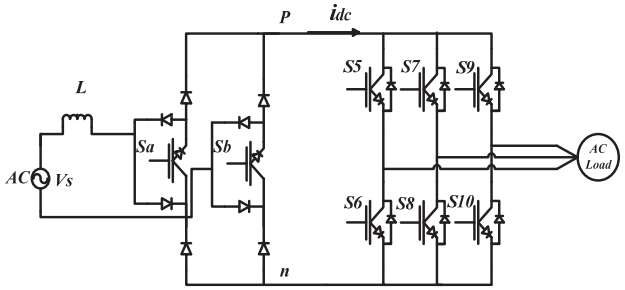

Fig. 6: 8-switch topology

B. Reduced steps of the single-phase to three phase UPS

Typical single-phase to three-phase on-line UPS topology is shown in Fig. 7. In circuit of Fig. 8, compared with the circuit of Fig. 7, the number of the converter's switches is reduced to 8, whereas it retains the function of the topology in Fig. 7. However, it also has some disadvantages such as higher output current distortion and doubly high dc-link voltage requirement [20].

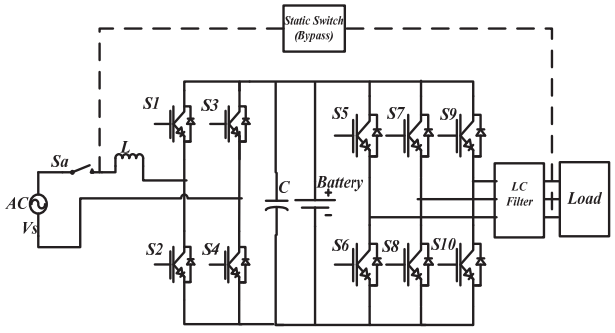

Fig. 7: A 10-switches typical single-phase to three-phase on-line UPS topology

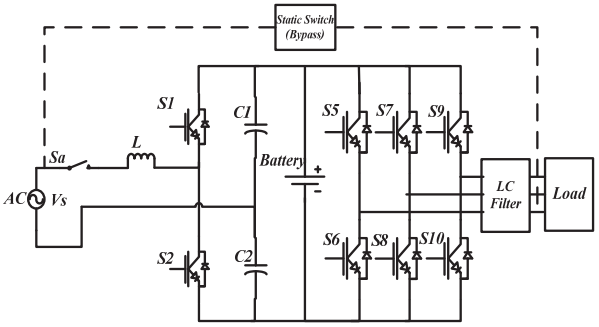

Fig. 8: 8-switches typical single-phase to three-phase on-line UPS topology

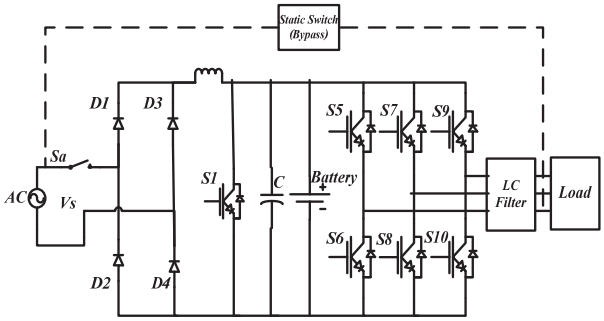

Fig. 9: 7-switches typical single-phase to three-phase on-line UPS topology

Also, in circuit of Fig. 9, the number of the converter's switches is reduced to 7. It has 4 rectifier diodes too. In fact, reduced switch count can be obtained by using capacitor midpoint connection [21] or sharing converter legs [22].

III. PROPOSED SYSTEM

The proposed new UPS system is shown in Fig. 10. It consists of a rectifier, two battery sets and a two-leg inverter. The rectifier consists of four diodes D1, D2, D3, D4, one inductor *Lf*, one IGBT, and two electrolytic capacitors C1, C2.

The two battery sets are directly connected to the split capacitor dc bus resulting in a simple system. The three-phase inverter consists of four switches *S1*, *S2*, *S3* and *S4* [5]. Voltage conversion ratio in proposed topology is equal to previous topologies.

There are two operating modes related to this topology: normal mode and stored energy mode:

- *Normal Mode of Operation*

During this mode of operation, the power to the load is continuously supplied via the rectifier/charger and inverter. In fact, a double conversion, that is, AC/DC and DC/AC, takes place. It allows very good line conditioning .The AC/DC converter charges the battery set and supplies power to the load via the inverter. Therefore, it has the highest power rating in this topology, increasing the cost.

- *Stored-Energy Mode of Operation*

When the AC input voltage is outside the preset tolerance, the inverter and battery maintain continuity of power to the load. The duration of this mode is the duration of the

preset UPS backup time or until the AC line returns within the preset tolerance. When the AC line returns, a phase-locked loop (PLL) makes the load voltage in phase with the input voltage and after that the UPS system returns to the normal operating mode.

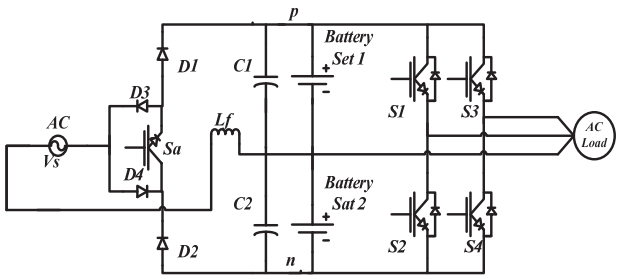

Fig. 10: The proposed new single-phase to three-phase on-line UPS topology

IV. Simulation Results

Time-domain simulations are carried out to verify the theoretical studies and evaluate the performance of the proposed topology. The simulations are performed using PSIM software. The simulated system parameters are given in Table I.

TABLE 1
System Parameters

Parameters	Rating
Power	1.2 kW
Input Voltage	220 VAC
Input Filter	L=100μH
Output Voltage (line-line)	300 VAC
Output Voltage THD	3.1 %
Load	L=10 mH , R= 40 Ω
DC-Link Voltage	650-700 VDC

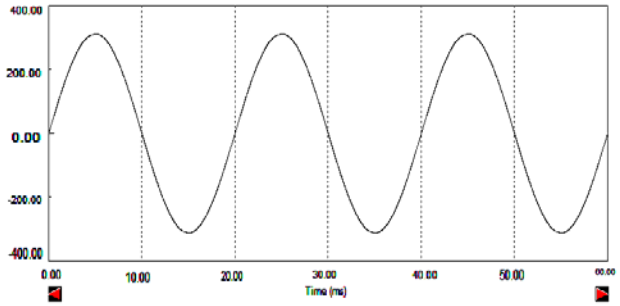

Fig. 11: Simulation results for the input voltage

Fig. 11 to 15 show the simulation results for the proposed system. Fig. 11 shows the input ac line voltage. Fig. 12 shows the simulation results for DC link voltage of proposed system. Fig. 13 and 14 show the simulation results for output current and output voltage, respectively. Also, Fig. 15 shows the frequency domain of output voltage. It can be found that the output voltage is regulated sinusoidal waveform.

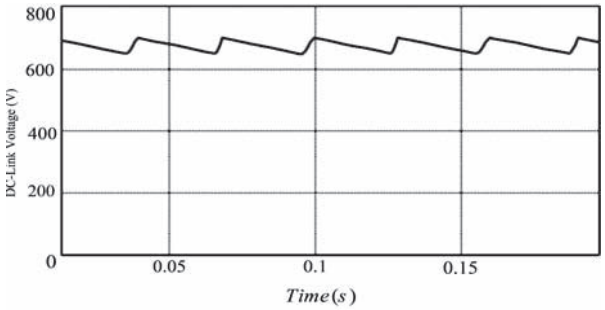

Fig. 12: Simulation results for DC link voltage

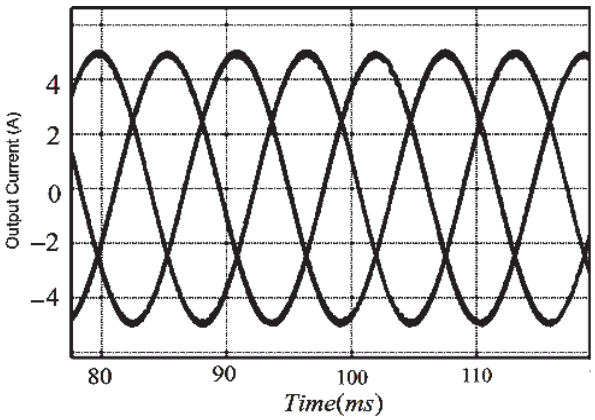

Fig. 13: Simulation results for output current

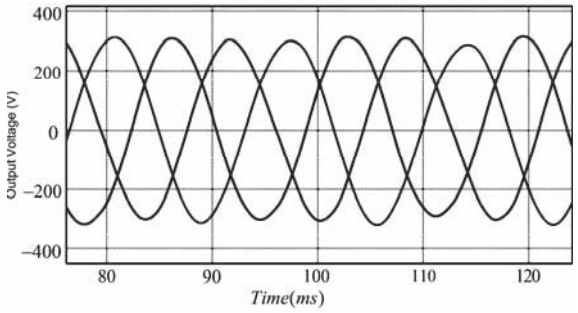

Fig. 14: Simulation results for three-phase phase to neutral output voltage.

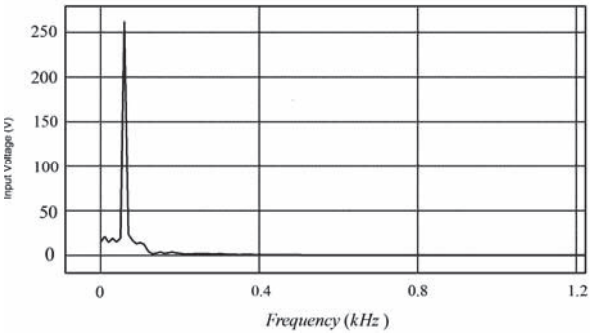

Fig. 15: Simulation results for output voltage frequency domain

V. Conclusion

This paper investigates the performance of a new reduced switch online single-phase to three-phase UPS topology. It is based on a single phase AC/DC rectifier converter and a three-phase two leg DC/AC inverter. It is suitable for sensitive loads because it guarantees the three-phase power quality that means: sinusoidal, balanced, and symmetrical voltages even with nonlinear and unbalanced

loads. The topology has only 5 switches. The concept of cost reduction for the converters is applied by reducing the number of switches. The reduced number of switches results in lower cost, greater compactness, and higher reliability than those of the conventional counterparts. The circuit topology, operation, and control strategy have been described and as simulation results are also presented to verify its feasibility.

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BIOGRAPHIES

Mehrnaz Sharifian Isfahani was born in Isfahan, Iran, on 1987. She received the B.S. in Electrical Engineering from department of Technology and Engineering, University of Isfahan (UI), Iran in 2010 where she was assisting as a scientific researcher after her graduation. Her main research interests are in the industrial and power electronics fields and are specifically related to uninterruptible power supplies, electrical drives, digital control, renewable energy supplies. She is currently the graduate student in Computer and Electronics Engineering Department of University of Nebraska-Lincoln.

Mehdi Niroomand was born in Isfahan, Iran, on 1979. He received the B.S., M.S. and PhD in electrical engineering from Isfahan University of Technology (IUT), Iran in 2001, 2004 and 2010 respectively. His research interests include uninterruptible power supplies, switching power supplies, control in power electronics, renewable energy and other fields of power electronics.
Since 2010, he has been with the Department of Technology and Engineering at University of Isfahan, where he is presently an Assistant Professor.

A Novel Speed Controller Based on Lagrange's Interpolation for Closed-loop Control of a CSI-fed Induction Motor Drive

S. M. Tripathi [1] A. K. Srivastava [2] A. K. Pandey [3]

Abstract–This work aims to investigate the feasibility of a novel speed controller based on Lagrange's interpolation (LI) for better performance of a self-commutated current source inverter-fed induction motor drive. The LI speed controller is based upon the look-up table prepared from a series of simulated patterns of 'reference slip speed' *vs.* 'speed error' of the classical PI speed controller. The performance of the drive employing this novel LI speed controller is evaluated analytically for a 1-hp induction motor and is compared to that with classical PI speed controller using MATLAB simulation.

Keywords–Closed-loop control, current source inverter, induction motor drive, Lagrange's interpolation (LI), speed controller.

I. Introduction

Induction motors in high performance variable speed drive applications have a series of advantages. For such kind of application, the variable speed drive requires a good power processing system and a good controller. A good power processing system is characterized by its simplicity, ruggedness, and lower cost. The current source inverter (CSI) has all these features. In CSI-fed induction motor drive, the current source at the front end makes the system naturally capable of power regeneration [1]-[3].

Proportional plus integral (PI) controllers, which are conventionally employed for CSI-fed induction motor drives; suffer from some limitations as the design of these controllers depends on exact mathematical model with accurate parameters [4]. A model reference adaptive controller (MRAC) was reported to improve the behavior of CSI-fed induction motor drive. However, in wide range of speed control, the design of MRAC controller becomes rather complicated [4].

The design of intelligent controllers based on artificial intelligence (AI) does not need the exact mathematical model of the system. Therefore, artificial neural network (ANN) and fuzzy logic control (FLC) demand special attention for speed control of high performance induction motor drives [5]-[6]. The main design problem with FLC lies in the determination of consistent and complete rule set and shape of the membership functions.

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On the other hand, ANN alone is insufficient if the training data are not enough to take care of all the operating modes [6].

In the present paper, the closed-loop scheme of a self-commutated current source inverter-fed induction motor drive employing a novel Lagrange's interpolation (LI) based speed controller is investigated for better performance.

II. Lagrange's Interpolation (LI) Based Speed Controller

The conventional CSI-fed induction motor drive system essentially consists of a three-phase AC source, a PWM rectifier, a DC link smoothening reactor, a current-controlled inverter, a three-phase squirrel cage induction motor, a three-phase capacitor bank, and two PI controllers – one in the outer speed feedback loop and the other in the inner current feedback loop. In the present work, the outer PI speed controller of the conventional CSI-fed induction motor drive system [7]-[8] has been replaced by a novel speed controller based on the Lagrange's interpolation (LI) technique as shown in Figure 1.

The closed-form mathematical model of the CSI-fed induction motor drive system has been considered the same as developed in [8] excluding the speed controller in outer feedback loop. The control law for the LI based speed controller in outer feedback loop is developed in this section.

The LI based speed controller compares the reference speed and the actual rotor speed and processes the speed error to obtain the reference slip speed (ω_{sl}^{*}). The functional relationship between reference slip speed ω_{sl}^{*} and the speed error $\Delta\omega$ ($=\omega_{ref}-\omega_r$) can be expressed as:

$$\omega_{sl}^{*}=\psi(\Delta\omega)\ ;\ \Delta\omega_0\le\Delta\omega\le\Delta\omega_n \qquad (1)$$

Polynomial interpolation is based on the well known fact that any n^{th} order polynomial is uniquely determined by $(n+1)$ points with distinct argument values. Compliant with a famous theorem due to Weierstrass [9], the single-valued function $\psi(\Delta\omega)$ can be approximated by a polynomial $P_n(\Delta\omega)$ passing through the $(n+1)$ points $[\Delta\omega_i\ ,\psi(\Delta\omega_i)]\ ;\ i=0,1,2,\cdots\cdots n$ with very small error, *i.e.*

$$\psi(\Delta\omega)\cong P_n(\Delta\omega)=A_0+A_1\Delta\omega+A_2(\Delta\omega)^2+\cdots\cdots+A_n(\Delta\omega)^n \qquad (2)$$

where A_i 's are constants.

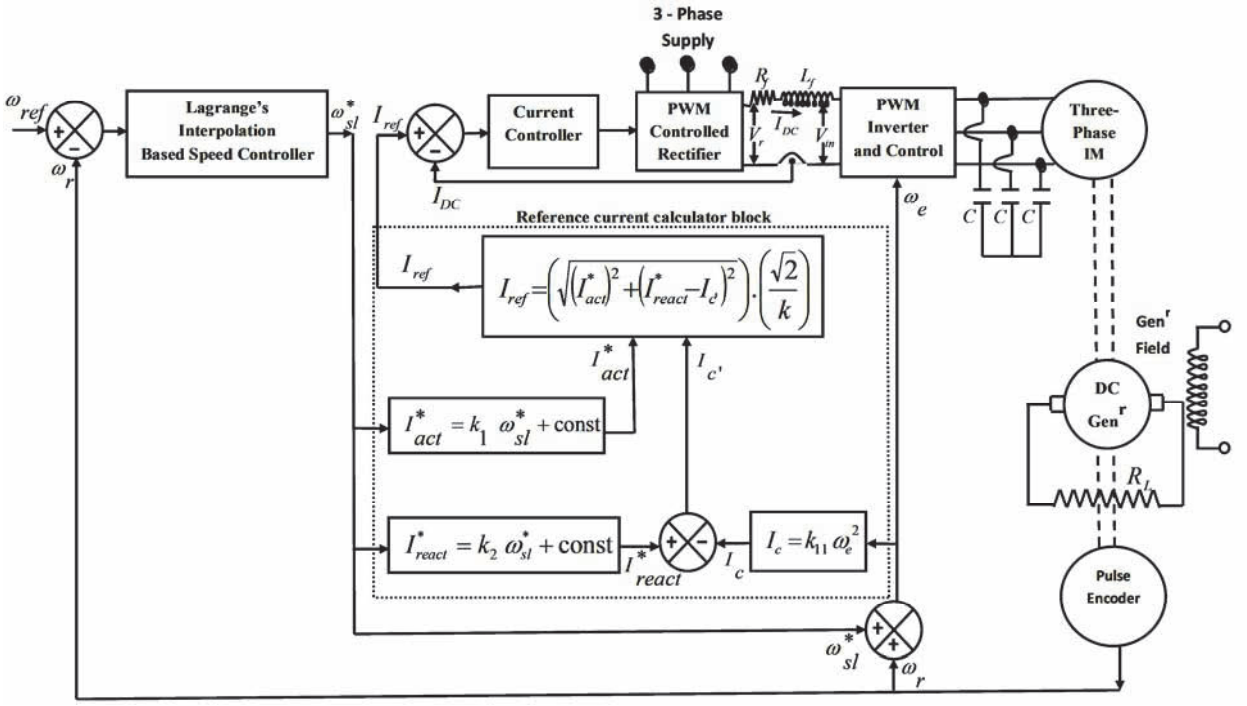

Fig. 1: Variable speed self-commutated current source inverter-fed induction motor drive with LI speed controller

On putting, $P_n(\Delta\omega_i) = \psi(\Delta\omega_i)$; $i = 0, 1, 2, \cdots\cdots n$ in (2), and eliminating $A_0, A_1, A_2, \cdots\cdots A_n$ the following expression is obtained:

$$\begin{vmatrix} \psi(\Delta\omega) & 1 & \Delta\omega & (\Delta\omega)^2 & \cdots & (\Delta\omega)^n \\ \psi(\Delta\omega_0) & 1 & \Delta\omega_0 & (\Delta\omega_0)^2 & \cdots & (\Delta\omega_0)^n \\ \psi(\Delta\omega_1) & 1 & \Delta\omega_1 & (\Delta\omega_1)^2 & \cdots & (\Delta\omega_1)^n \\ \psi(\Delta\omega_2) & 1 & \Delta\omega_2 & (\Delta\omega_2)^2 & \cdots & (\Delta\omega_2)^n \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \psi(\Delta\omega_n) & 1 & \Delta\omega_n & (\Delta\omega_n)^2 & \cdots & (\Delta\omega_n)^n \end{vmatrix} = 0 \quad (3)$$

Expanding in terms of the elements of the first column, the required control law for Lagrange's interpolation based speed controller is obtained as follows:

$$\omega_{sl}^* = \psi(\Delta\omega) = \sum_{i=0}^{n} \left[\left\{ \prod_{\substack{j=0 \\ j\neq i}}^{n} \left(\frac{\Delta\omega - \Delta\omega_j}{\Delta\omega_i - \Delta\omega_j} \right) \right\} \psi(\Delta\omega_i) \right] \quad (4)$$

Numerous patterns for 'reference slip speed' *vs.* 'speed error' with conventional PI speed controller, keeping parameters such as k_{p_s} and k_{i_s} to optimal values for a given loading condition, are obtained through a MATLAB program. A few of these patterns are selected to constitute a look-up table, which of course is the result of a few repeated trials. These look-up data sets are considered as $(n+1)$ points *viz.* $[\Delta\omega_i, \psi(\Delta\omega_i)]$; $i = 0, 1, 2, \cdots\cdots n$ in the control law (4) for Lagrange's interpolation based speed controller. Using (4) the value of reference slip speed ω_{sl}^* can be determined whenever speed error is $\Delta\omega$. This reference slip speed (ω_{sl}^*) is required to estimate the reference stator active current (I_{act}^*), reference stator reactive current (I_{react}^*) of the induction motor and the switching frequency of the inverter (ω_e) using the following equations:

$$I_{act}^* = k_1\, \omega_{sl}^* + \text{constant} \quad (5)$$

$$I_{react}^* = k_2\, \omega_{sl}^* + \text{constant} \quad (6)$$

$$\omega_e = \omega_r + \omega_{sl}^* \quad (7)$$

Here, k_1 and k_2 are the slopes of the 'stator active current' *vs.* 'slip speed' and 'stator reactive current' *vs.* 'slip speed' characteristics respectively. These characteristics are obtained experimentally [7]. The reference DC link current is determined using the equations:

$$I_{ref} = \left(\sqrt{\left(I_{act}^*\right)^2 + \left(I_{react}^* - I_{c'}\right)^2} \right) \cdot \left(\frac{\sqrt{2}}{k} \right) \quad (8)$$

$$I_{c'} = I_{react}^* - I_c \quad (9)$$

$$I_c = k_{11}\, \omega_e^{\,2} \quad (10)$$

$$k_{11} = \frac{I_{c\,(rated)}}{(\omega_{e\,(rated)})^2} \quad (11)$$

III. Simulation Results and Discussions

Simulations are factually focused on whether or not the performance of the drive with LI-PI (LI speed and PI current) controllers is better than that with PI-PI (PI speed and PI current) controllers. For the comparison in terms of the percentage overshoot, settling time and steady-state error, MATLAB simulations of the conventional CSI drive employing PI-PI controllers and the proposed CSI drive employing LI-PI controllers are performed for different step variations in reference speed each after an interval of 10 seconds as shown in Fig. 2. For a clear judgment, the responses of the drive are considered separately for each alteration in reference speed.

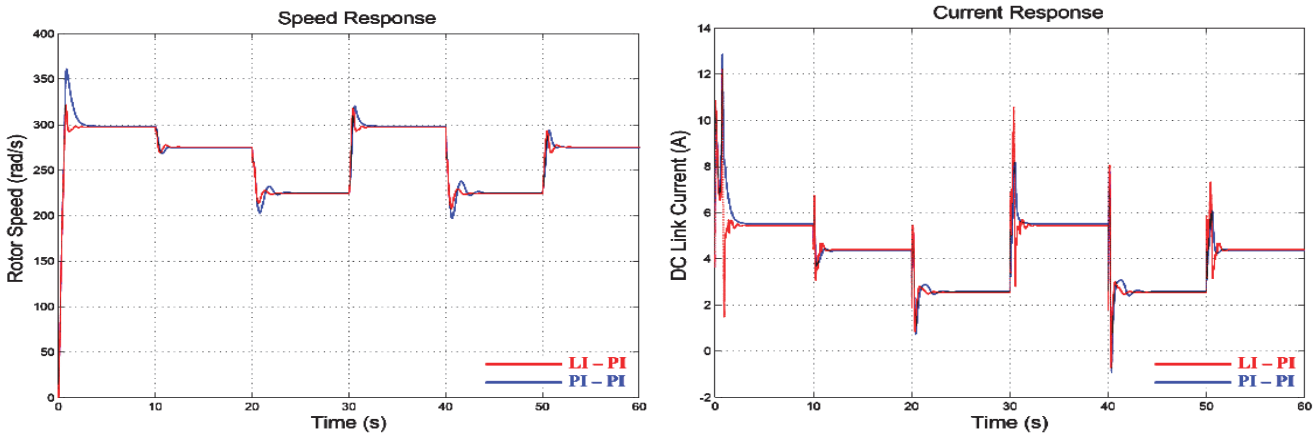

Fig. 2: Response of the drive for step changes in reference speed each after an interval of 10 seconds

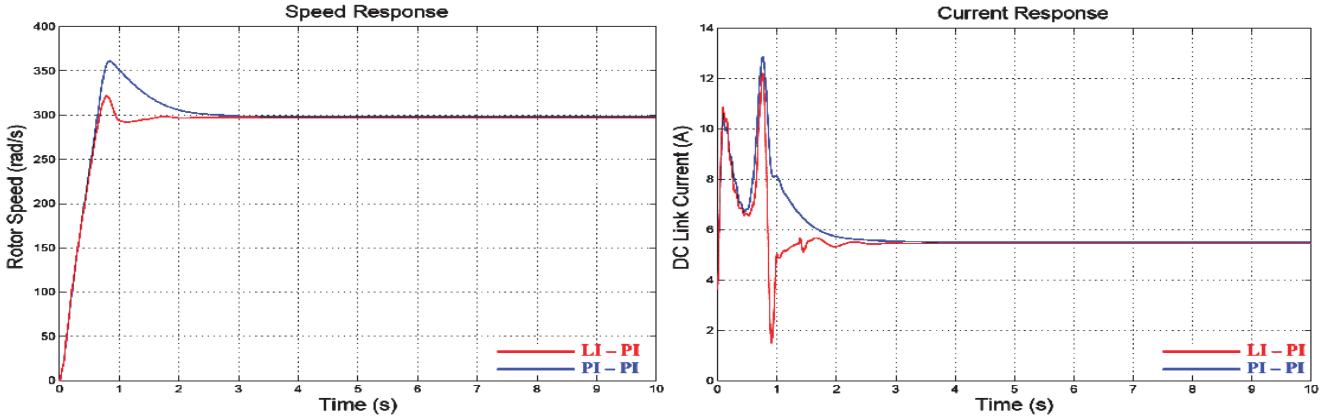

Fig.3: Response of the drive for step changes in reference speed from 0 rad/s to 298.29 rad/s

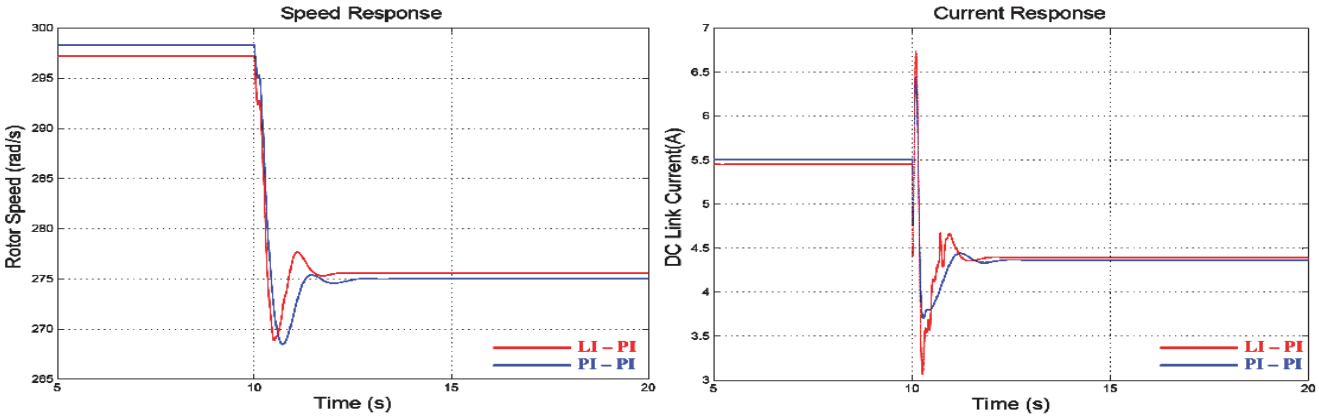

Fig.4: Response of the drive for step changes in reference speed from 298.29 rad/s to 275 rad/s

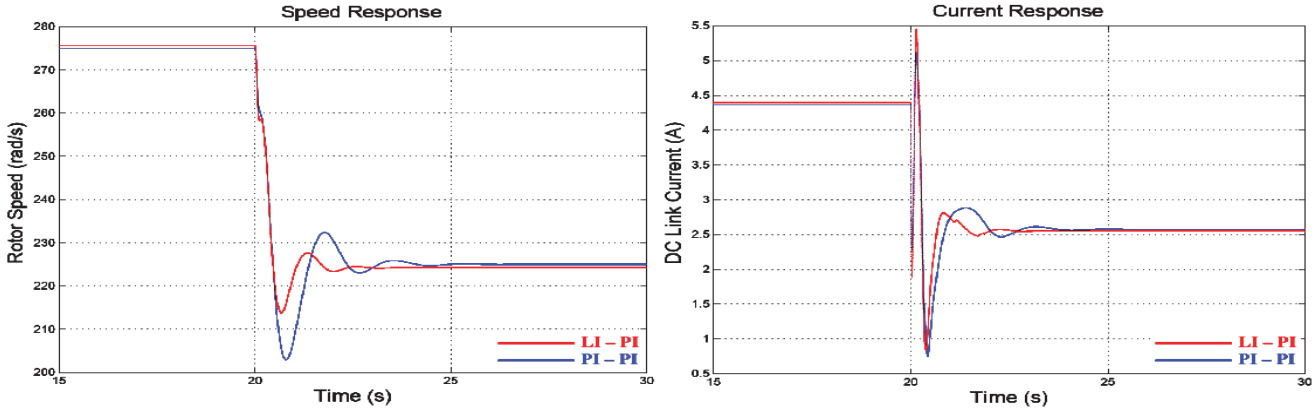

Fig. 5: Response of the drive for step changes in reference speed from 275 rad/s to 225 rad/s

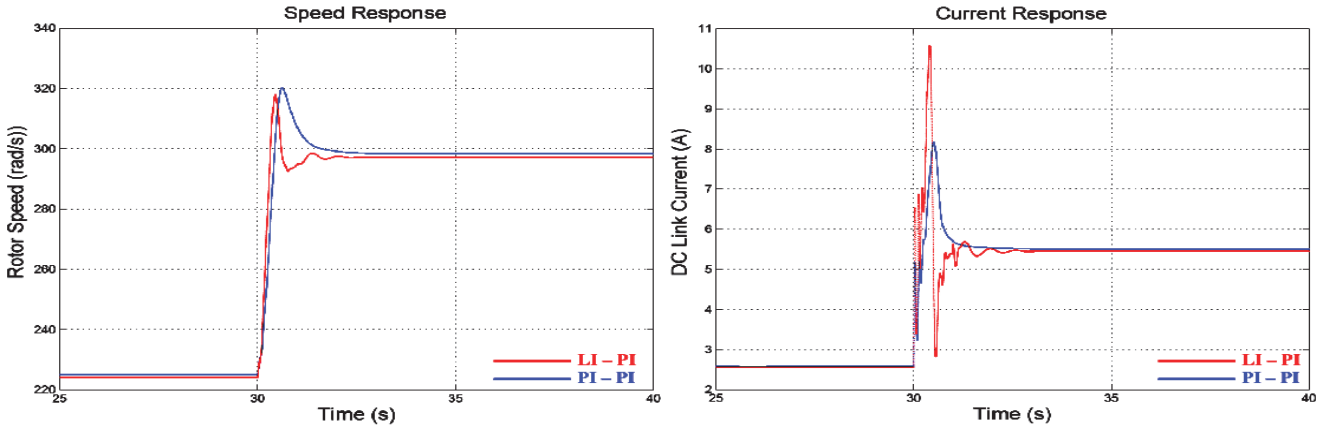

Fig. 6: Response of the drive for step changes in reference speed from 225 rad/s to 298.29 rad/s

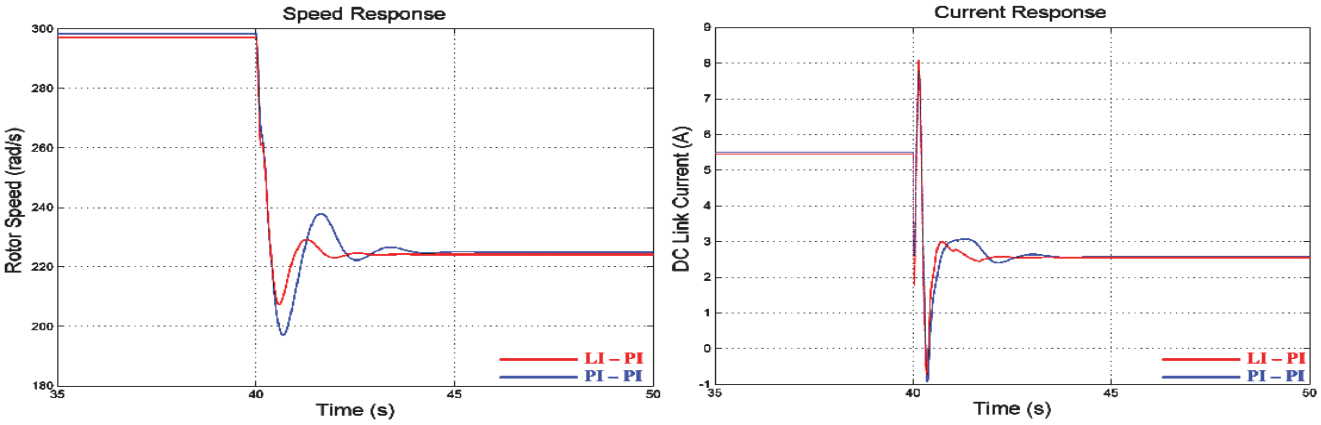

Fig. 7: Response of the drive for step changes in reference speed from 298.29 rad/s to 225 rad/s

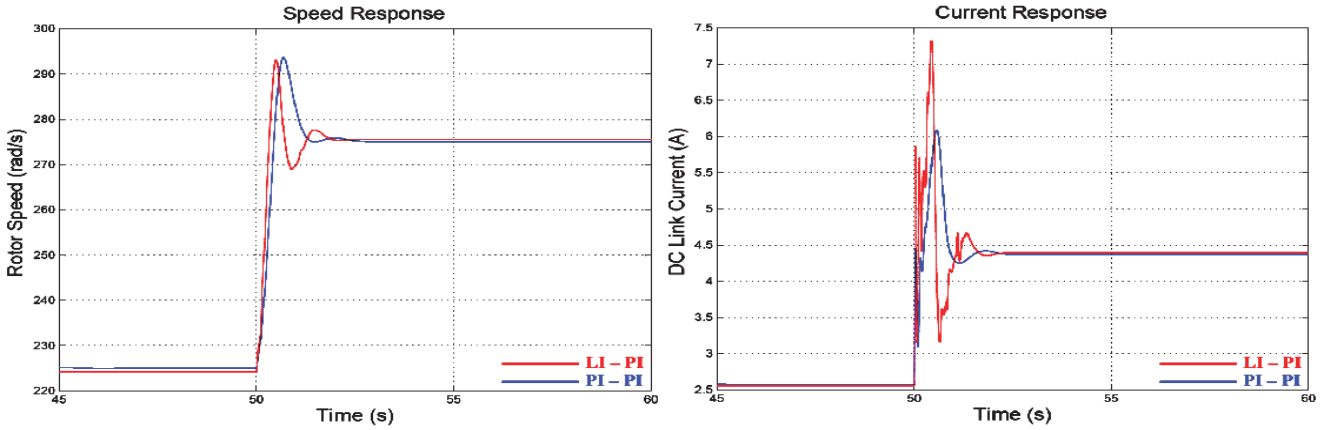

Fig.8: Response of the drive for step changes in reference speed from 225 rad/s to 275 rad/s

Figs: 3-8 show the speed and DC link current responses of the drive separately for step changes in reference speed from 0 rad/s to 298.29 rad/s (start-up), 298.29 rad/s to 275 rad/s (deceleration), 275 rad/s to 225 rad/s (deceleration), 225 rad/s to 298.29 rad/s (acceleration), 298.29 rad/s to 225 rad/s (deceleration), and 225 rad/s to 275 rad/s (acceleration) respectively.

The steady-state DC link current, percentage overshoot, drive settling time and steady-state error corresponding to different alterations in reference speed stated aforesaid, are summarized in Table-1. It has been found that the steady-state value of the DC link current is increased / decreased with increase / decrease in motor speed. The percentage overshoot and settling time of the drive with LI based speed controller is less than that with the conventional PI speed controller. It is also observed that the steady-state error in speed response of the drive with LI based speed controller is more than that with conventional PI speed controller. In fact, this is due to the error associated with the approximation of the function $\psi(\Delta\omega)$ by means of a polynomial $P_n(\Delta\omega)$. However, the percentage steady-state error is within the prescribed limit of 2%.

This way the speed and current response curves obtained through MATLAB simulation and facts in Table 1 show the success of proposed LI based speed controller.

Table 1: Performance of the drive for each alteration in reference speed

Sr.	Step-change in reference speed (rad/s)		Steady-state DC link current (A)		Speed overshoot (%)		Drive settling time (s)		Steady-state speed error (%)	
	From	To	LI - PI	PI - PI	LI – PI	PI - PI	LI – PI	PI - PI	LI - PI	PI - PI
1.	0	298.29	5.446	5.506	7.78	20.98	2.41	3.24	0.365	0.010
2.	298.29	275	4.391	4.365	2.23	2.36	2.20	2.75	0.204	0.014
3.	275	225	2.554	2.573	5.01	9.82	2.85	3.92	0.364	0.009
4.	225	298.29	5.446	5.506	6.56	7.27	2.53	2.75	0.365	0.010
5.	298.29	225	2.554	2.573	7.84	12.4	2.93	3.96	0.364	0.009
6.	225	275	4.391	4.365	6.59	6.76	2.10	2.49	0.204	0.014

IV. Conclusions

A novel speed controller based on Lagrange's interpolation has been introduced for CSI-fed induction motor drive and the control law for LI speed controller is established. The drive is simulated for both PI and LI speed controllers for different speed variations in the reference speed. The results for both controllers under each variation in reference speed are compared and analyzed. It is observed that the changes in the DC link currents, in accordance with any disturbances in the reference speed, are immediate with LI-PI controllers when compared with PI-PI controllers. Though, it is also seen that the steady state error in the speed response of the drive is more with LI speed controller than that with conventional PI speed controller, yet it is within prescribed limit and is, therefore, acceptable. Moreover, the CSI fed induction motor drive system using an LI speed controller has reduced speed overshoot and settling time compared to the system with a PI speed controller. This way, the simulation results have proved the feasibility and better performance of the proposed speed controller based on Lagrange's interpolation for closed-loop control of a self-commutated CSI-fed induction motor drive.

Appendix

Name plate ratings of induction motor

1 hp, three-phase, 400 V, 50 Hz, 4-pole, 1425 rpm, star

Induction motor parameters

R_s = 3.520 Ω R_r = 2.780 Ω L_s = 0.165 H
L_r = 0.165 H L_m = 0.150 H J = 0.01289 kg-m^2

Parameters of DC link and capacitor bank

R_f = 0.250 Ω, L_f = 0.040 H, C = 150 µF

DC Generator specification

1 hp, 220 V, 4 A, 1500 rpm, shunt connected

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Improved Power Quality Based Electronic Ballast for a Fluorescent Lamp with Constant DC Link Voltage

Ashish Shrivastava[1] and Bhim Singh[2]

Abstract–This paper deals with the analysis, design, modeling and simulation of a low crest factor (CF) and a high power factor (PF) electronic ballast for a fluorescent lamp. The proposed ballast uses a boost converter in continuous conduction mode (CCM) as a power factor corrector (PFC). In this topology, a half bridge series resonant parallel loaded inverter is used to convert dc to high frequency ac to feed fluorescent lamp. The modeling and simulation of this topology are carried out in Matlab-Simulink environment for a fluorescent lamp fed from 220V, 50Hz ac mains. The power quality indices are estimated such as total harmonic distortion of ac mains current (THD_i), power factor (PF) and crest factor (CF).

Keywords–Power factor correction (PFC), Continuous conduction mode (CCM), Electronic ballast, Fluorescent lamp, Zero voltage switching (ZVS), and Series resonant parallel loaded inverter (SRPLI).

I. Introduction

In recent years fluorescent lamps have become increasingly popular as an alternative to conventional incandescent lamps because of their better luminous efficacy (Lm/Watt) and power consumption. Fluorescent lamps exhibit negative resistance characteristic in the desired region of operation. This produces an unstable condition if a fluorescent lamp is directly connected across a voltage source to cause ionization. Therefore, a current-limiting device called ballast is required [1]. Compared to conventional magnetic ballasts, high frequency (20-100 kHz) electronic ballasts offer significant advantages such as reduction in power consumption, flicker, audible noise and weight [2-5]. The electronic ballast consists of a power factor correction ac-dc converter, high frequency inverter and a matching resonant circuit. The resonant circuit enables a high ignition voltage to be generated and makes the lamp current essentially sinusoidal. In electronic ballast, high frequency dc-ac conversion becomes possible with the invention of solid state switching devices namely MOSFETs which have high switching capability with almost negligible losses. The preferred method to drive the fluorescent lamp is by using an unmodulated sine wave current with a minimal ripple content. The input current crest factor (I_{peak}/I_{rms}) for the operating condition should be as low as possible, not exceeding 1.7 [1, 6].

Besides this, in comparison of magnetic ballast, electronic ballast can control lamp power more easily and has higher efficiency. Normally, a power factor corrected electronic ballast needs two level of power conversion. First level of power conversion is for ac-dc conversion and second level is for dc-ac conversion.

In this paper, a power factor corrected topology with constant dc link voltage is proposed for an electronic ballast. The power factor correction (PFC) converter improves the input power factor nearly close to unity and regulates dc voltage and the half bridge resonant inverter maintains the constant load power supplied at high frequency. Because of the zero voltage switching (ZVS), the switching losses are reduced significantly which enhances the efficiency of the electronic ballast.

II. Proposed Topology of Electronic Ballast

Fig. 1 has shown the schematic of the proposed electronic ballast, which consists of a PFC converter and a lamp driving dc-ac converter in cascade connection. The ac-dc converter achieves power factor correction (PFC) and the dc-ac converter supplies high frequency voltage to the fluorescent lamp [8-13]. In proposed electronic ballast the selection of a proper converter is made based upon the following guidelines.

- An energy storage element is used between a PFC converter and a lamp-driving dc-ac converter to prevent the lamp current from being modulated by the line voltage. For this purpose a dc capacitor is preferred over an inductor due to its lesser cost and size.
- A lamp-driving dc-ac converter is selected to be a voltage-fed inverter to save filter components.
- Low source voltage is needed to boost-up for generating a high voltage to ignite lamp without the need of a boost-up transformer.

As per the considerations given above, a boost converter is selected as the PFC converter, and a quasi-half-bridge series resonant parallel loaded inverter is used to drive the lamp. Fig. 1 shows the proposed electronic ballast derived from CCM boost converter and quasi-half-bridge series resonant parallel loaded inverter (SRPLI).

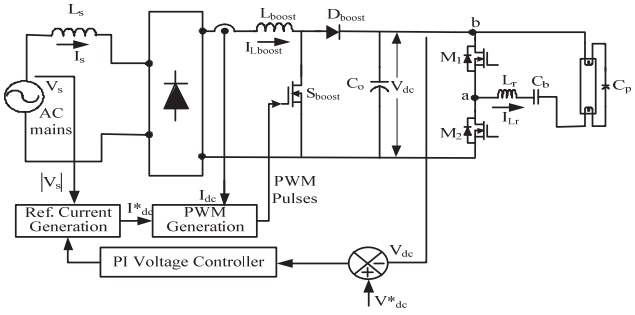

Fig.1: Proposed Topology of a Boost PFC Electronic Ballast

The active power switches of series resonant inverter M_1 and M_2 are alternately turned on and off at a 40 kHz frequency. The switching frequency of the inverter should be more than the resonant frequency of the load circuit to achieve the ZVS (zero voltage switching),

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which reduces the switching losses and improves the overall efficiency of electronic ballast.

III. Analysis and Design of Proposed Electronic Ballast

Following considerations are made to analyze the proposed topology of electronic ballast [7-9].

- At the time of starting, the fluorescent lamp behaves as an open circuit and during steady state operation it is considered as a pure resistor.
- As compared to the lamp resistance the filament resistance is neglected and switching devices are considered ideal switches.
- The dc blocking capacitor C_b is much larger than the resonant capacitance C_p so that its voltage ripple is negligible.

The detailed design of the boost inductor and the resonant inverter components are as follows.

A. Design of Boost Inductor

The value of boost inductor is evaluated by using the below mentioned equations. The duty ratio, D is expressed in terms of dc inverse voltage gain as,

$$D = 1 - \alpha \tag{1}$$

where, α is defined as,

$$\alpha = \frac{V_{sm}}{V_{dc}} \tag{2}$$

The coefficient $Y(\alpha)$ is defined as,

$$Y(\alpha) = -2 - \frac{\pi}{\alpha} + \frac{2}{\alpha\sqrt{1-\alpha^2}}\left\{\frac{\pi}{2} + \tan^{-1}\left(\frac{\alpha}{\sqrt{1-\alpha^2}}\right)\right\} \tag{3}$$

From (3), the value of boost inductor is given as,

$$L_{boost} = \left(\frac{V_{sm}}{\omega_{switching} P_o}\right)\frac{(1-\alpha^2)Y(\alpha)}{\alpha} \tag{4}$$

where, D is duty ratio, α is dc inverse voltage gain, V_{sm} is peak value of the input rms voltage, V_{dc} is dc link voltage, P_o is rated output power of fluorescent lamp.

B. Design of Resonant Circuit Parameters

At the time of starting, the self oscillating technique provides a resonant frequency ($\omega_{starting}$) which is made equal to the switching frequency ($\omega_{switching}$). The relationship between the resonant parameters and the starting resonant frequency is given by (5) as,

$$\omega_{starting} = \omega_{switching} = \frac{1}{\sqrt{L_r\left(\frac{C_b C_p}{C_{b+} C_p}\right)}} \tag{5}$$

The steady-state resonant frequency is given by (6) as,

$$\omega_{running} = \frac{1}{\sqrt{L_r C_b}} \tag{6}$$

If the switching frequency is more than the steady-state resonant frequency then the zero voltage switching (ZVS) is ensured. Considering that,

$$\omega_{switching} = 4\omega_{running} \tag{7}$$

Fig.2 shows the equivalent circuit of the series resonant parallel loaded inverter (SRPLI) under the steady-state operation of the lamp. In this circuit L_r, C_b and C_p are the resonant circuit parameters and R_{lamp} is the resistance of the fluorescent lamp.

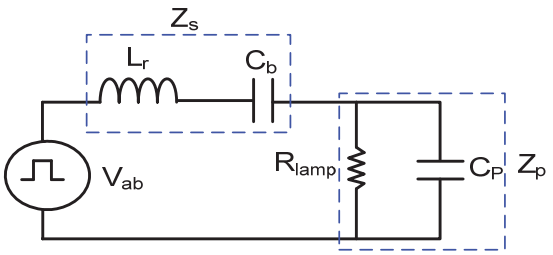

Fig. 2: Equivalent circuit of the inverter

The relationship between the rated lamp voltage and the fundamental component of the output of voltage source inverter is given in (8) in the frequency domain as,

$$\left|\frac{V_{lamp}(j\omega)}{V_{ab}(j\omega)}\right| = \left|\frac{Z_p(j\omega)}{Z_s(j\omega) + Z_p(j\omega)}\right| \tag{8}$$

By solving (5), (6), (7) and (8), the resonant parameters can be given as,

$$C_b = 15\left(\frac{V_{lamp}}{V_{ab}}\right)\left(\frac{1}{R_{lamp}\omega_{switching}}\right) \tag{9}$$

$$C_P = \frac{C_b}{15} \tag{10}$$

$$L_r = \frac{16}{C_b(\omega_{switching})^2} \tag{11}$$

This design procedure includes the calculation of the boost inductor and resonant circuit parameters.

IV. Operating Modes of Proposed Ballast

The operating modes of the proposed Electronic ballast are gives as below in Figs 3a-3d.

(a) At $t_0 < t < t_1$, body diode D_2 is conducting and dc link capacitor is charged in the process. In this duration also gate pulse has been applied to the solid state active power switch M_2. The sequence of flow of current is given and also shown in Fig.3a,

$C_o(-) \rightarrow D_2 \rightarrow L_r \rightarrow C_b \rightarrow (R_{lamp} \| C_P) \rightarrow C_o(+)$

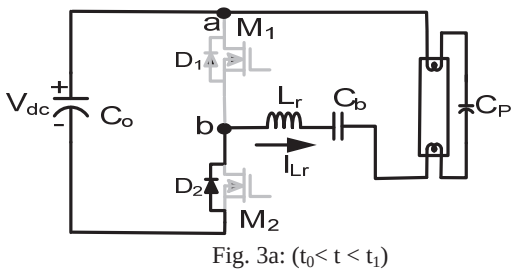

Fig. 3a: ($t_0 < t < t_1$)

At $t_1 < t < t_2$, MOSFET M_2 starts conducting and dc link capacitor is discharged in the process. The direction of resonant current changes as the current is shifted from diode D_2 to active power switch M_2. The sequence of flow of current is given and also shown in Fig.3b,

$C_o(+) \rightarrow (R_{lamp} \| C_P) \rightarrow C_b \rightarrow L_r \rightarrow M_2 \rightarrow C_o(-)$

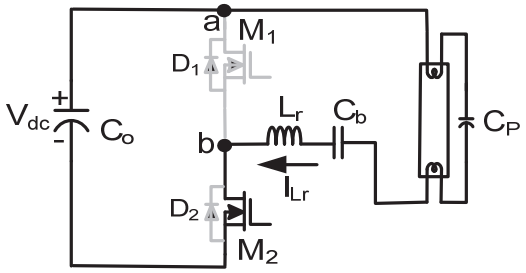

Fig. 3b: ($t_1 < t < t_2$)

At $t_2 < t < t_3$, body diode D_1 is conducting and the direction of current remains the same due to resonating nature of the circuit. In this duration gate pulse has also been applied to the active power switch M_1. The sequence of flow of current is given and also shown in Fig.3c,

$D_1 \rightarrow (R_{lamp} \| C_P) \rightarrow C_b \rightarrow L_r \rightarrow D_1$

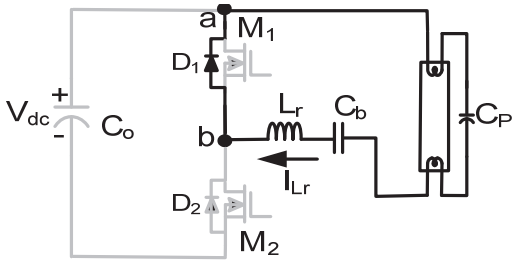

Fig. 3c: ($t_2 < t < t_3$)

At $t_2 < t < t_3$, MOSFET M_1 starts conducting and the current shifted from body diode D_1 to active power switch M_1. Hence the direction of current changes from positive to negative. The sequence of flow of current is given and also shown in Fig.3d,

$M_1 \rightarrow L_r \rightarrow C_b \rightarrow (R_{lamp} \| C_P) \rightarrow M_1$

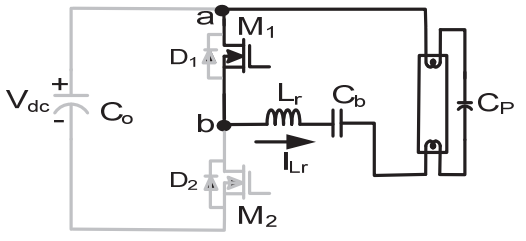

Fig. 3d: ($t_3 < t < t_4$)

Since the circuit is working at lagging power factor ($f_r < f_s$) as confirmed from Fig. 3e, the zero voltage switching (ZVS) has been achieved in resonant converter operation. Moreover, it is clearly observed from the operating modes of the above circuit that both MOSFETs (M_1 and M_2) are operating at zero voltage switching (ZVS). The theoretical waveform of series resonant inverter is given in Fig.3e.

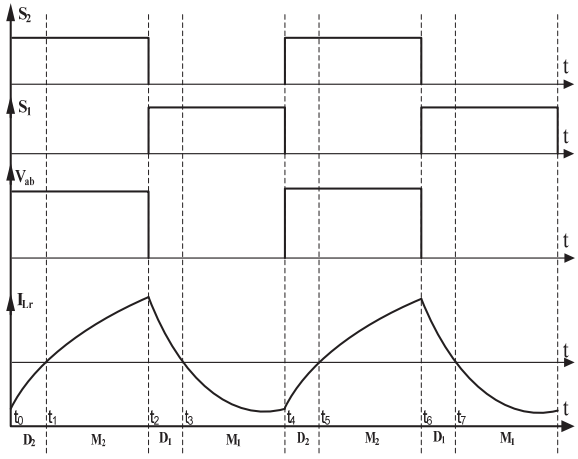

Fig. 3e: Theoretical waveforms of series resonant inverter of proposed electronic ballast

V. MATLAB MODEL OF PROPOSED BALLAST

The Matlab model of the proposed electronic ballast is developed as shown in Fig.4 in which the lamp is considered as a resistor at high frequency. The PFC topology is modeled in Matlab-Simulink model using PI (Proportional Integral) controller with current multiplier approach.

A 40 kHz triangular carrier wave is used for PWM generation. The design values of the components obtained from various design equations are appropriately selected to have desired power quality at the AC mains. These component values are given in Appendix along with other control parameters.

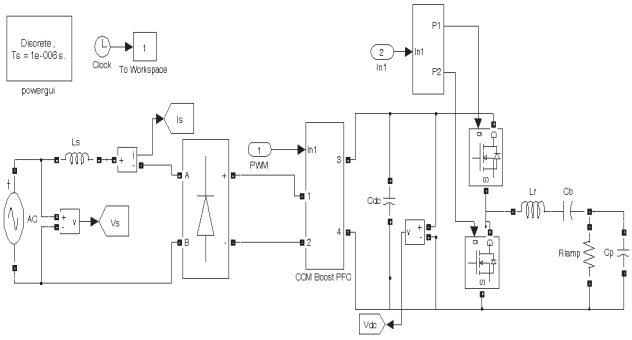

Fig. 4 Matlab model of proposed electronic ballast

VI. RESULTS AND DISCUSSION

The objective of the modeling and simulation is to validate the design of proposed electronic ballast which has improved power factor, low THD and low crest factor of ac mains current. As the ac input voltage increases from 100 V-270V, the dc link voltage remains constant at 400 V, thus the lamp current remains constant throughout this wide input ac voltage range, which realizes the constant lamp power. The input ac voltage and current waveforms, dc link voltage, boost inductor current at 100 V, 220 V and 270 V are shown in Fig. 5, Fig. 7, and Fig. 9. The lamp voltage and lamp current waveforms at 100 V, 220 V and 270 V are shown in Fig. 6, Fig. 8 and Fig. 10.

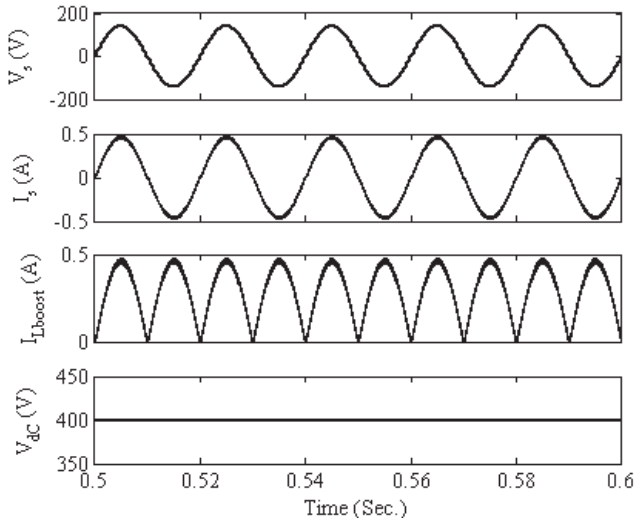

Fig.5: Performance of proposed electronic ballast in terms of source voltage (V_s), source current (I_s), boost inductor current (I_{Lboost}) and dc link voltage (V_{dc}) at 100 V

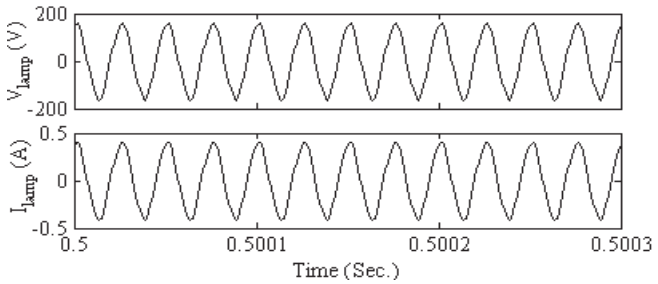

Fig.6: Performance of proposed electronic ballast in terms of lamp voltage (V_{lamp}) and lamp current (I_{lamp}) at 100 V

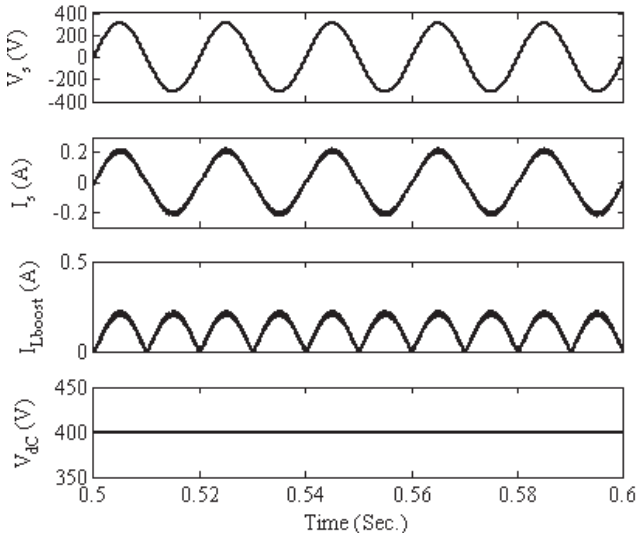

Fig.7: Performance of proposed electronic ballast in terms of source voltage (V_s), source current (I_s), boost inductor current (I_{Lboost}) and dc link voltage (V_{dc}) at 220 V

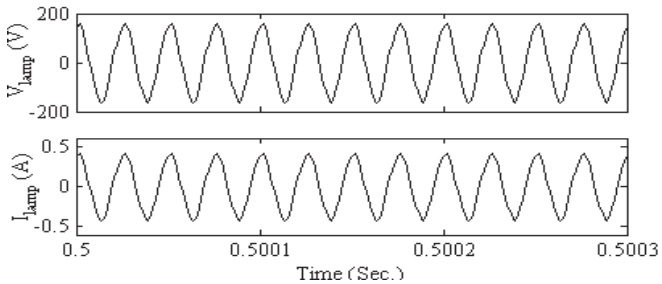

Fig.8: Performance of proposed electronic ballast in terms of lamp voltage (V_{lamp}) and lamp current (I_{lamp}) at 220 V

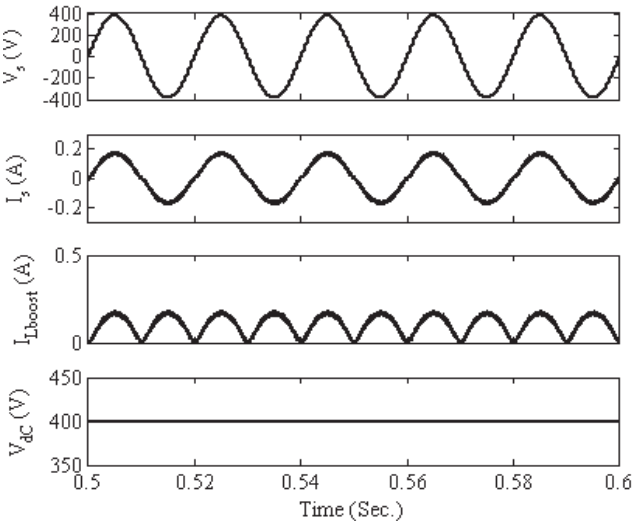

Fig.9: Performance of proposed electronic ballast in terms of source voltage (V_s), source current (I_s), boost inductor current (I_{Lboost}) and dc link voltage (V_{dc}) at 270 V

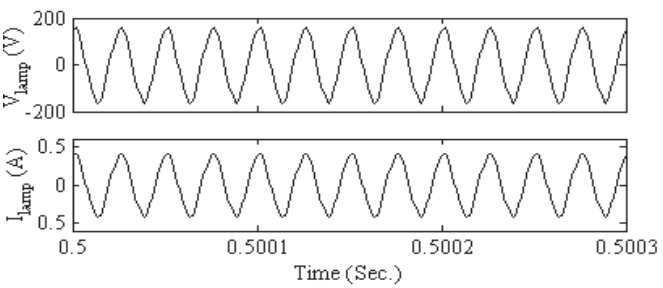

Fig.10: Performance of proposed electronic ballast in terms of lamp voltage (V_{lamp}) and lamp current (I_{lamp}) at 270 V

The fluorescent lamp is driven by a high frequency sinusoidal current generated from an LCC series resonant parallel converter, which operates above the resonant frequency to a zero voltage switching (ZVS). Fig. 11 shows the switch voltage (V_{M2}) and switch current (I_{M2}) waveforms (which is amplified 600 times to show on same scale as of V_{M2}), which confirms the zero voltage switching (ZVS).

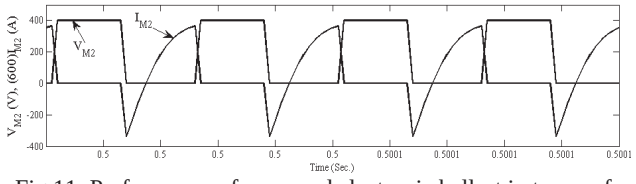

Fig.11: Performance of proposed electronic ballast in terms of switch voltage (V_{M2}), switch current ($600I_{M2}$) at 220 V

The ac mains current waveform along with its harmonic spectra and THD are shown in Fig. 12, Fig. 13 and Fig. 14 at ac mains voltage of 100 V, 220 V and 270 V.

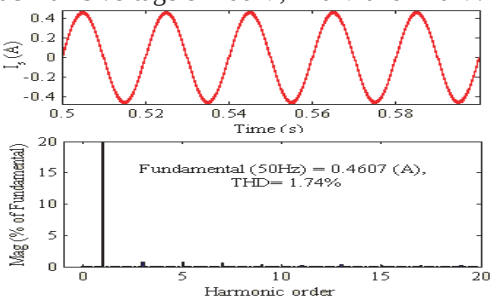

Fig. 12: Input current waveform and its harmonic spectra at ac mains voltage of 100V

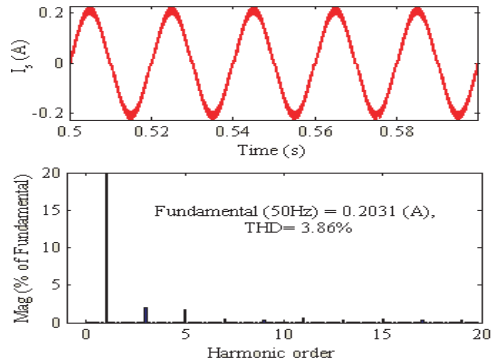

Fig. 13: Input current waveform and its harmonic spectra at ac mains voltage of 220V

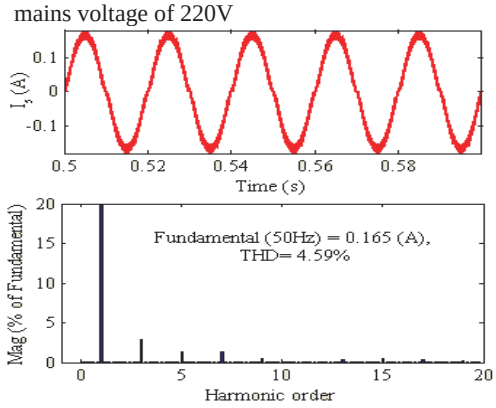

Fig. 14: Input current waveform and its harmonic spectra at ac mains voltage of 270V

The power quality parameters of the proposed boost PFC electronic ballast are listed in Table-I. The dc link voltage, lamp voltage and current have been maintained almost constant under the change in ac mains voltage from 110V-270 V. Table-I shows the variation of power factor, crest factor and % THD of ac mains current of proposed electronic ballast with input ac mains voltage. Moreover, power quality parameters of the proposed electronic ballast are within the norms of international standard IEC 61000-3-2 for class C equipment [6].

Table 1: Performance Parameters of Proposed Electronic Ballast

V_s (V)	I_s (A)	V_{dc} (V)	V_{lamp} (V)	I_{lamp} (A)	PF	THD %	CF
100	0.3258	400	109.9	0.2819	0.9997	1.74	1.41
110	0.2942	400	109.9	0.2819	0.9996	1.85	1.41
120	0.2683	400	109.9	0.2819	0.9995	2.03	1.41
130	0.2467	400	110	0.2819	0.9994	2.26	1.41
140	0.2285	400	110	0.2819	0.9993	2.39	1.41
150	0.2127	400	110	0.2819	0.9992	2.60	1.41
160	0.1989	400	110	0.2819	0.9991	2.78	1.41
170	0.1869	400	110	0.2819	0.999	3.04	1.41
180	0.1763	400	110	0.2819	0.9988	3.20	1.41
190	0.1669	400	110	0.2819	0.9987	3.40	1.41
200	0.1584	400	110	0.2819	0.9985	3.62	1.41
210	0.1508	400	110	0.2819	0.9985	3.69	1.41
220	0.1438	400	110	0.2819	0.9984	3.86	1.41
230	0.1482	400	110	0.2819	0.9983	3.88	1.41
240	0.1317	400	110	0.2819	0.9982	4.15	1.41
250	0.1264	400	110	0.2819	0.9981	4.22	1.41
260	0.1215	400	110	0.2819	0.9979	4.36	1.41
270	0.117	400	110	0.2819	0.9977	4.59	1.41

VII. Conclusion

A high power factor electronic ballast with constant dc link voltage has been designed, modeled and simulated to study its behaviour. The dc link voltage has been maintained constant, independent of changes in the ac input voltage. With an appropriate design of the resonant converter, the lamp current has been found close to the rated value. The simulation results have confirmed the low crest factor of 1.41 and high power factor almost close to unity of proposed electronic ballast. The proposed ballast has THD of ac mains current well below 5% for the universal voltage range of 100V-270V. The zero voltage switching (ZVS) has been achieved by keeping the switching frequency more than the resonance frequency of resonant inverter to reduce the switching losses.

Appendix

Rated lamp power: 31W, rated lamp current: 0.2818 A, rated lamp voltage: 110 V, switching frequency of PFC switch (f_s): 40 kHz, PI controller gains (K_p): 0.0035, (K_i): 0.0038, boost PFC inductor (L_{boost}): 15mH, dc link capacitor (C_o): 30µF, Resonant parameters: - resonant inductor (L_r): 2.7mH, dc blocking capacitor (C_b): 90nF, resonant capacitor (C_p): 6nF

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BIOGRAPHIES

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Dr. Bhim Singh was born in Rahamapur, India, in 1956. He received B.E (Electrical) degree from University of Roorkee in 1977 and M.Tech and Ph.D. degree from IIT Delhi, New Delhi, India, in 1979 and 1983, respectively. In 1983, he joined the Department of Electrical Engineering, University of Roorkee, as a lecturer, and in 1988 became a Reader. In December 1990, he joined the Department of Electrical Engineering, IIT Delhi, as an Assistant Professor. He became an Associate Professor in 1994 and Professor in 1997. He has been granted one US patent and filed nine Indian patents. He has executed more than sixty sponsored and consultancy projects. His area of interest includes power electronics, electrical machines and drives, active filters, Flexible Alternating Current Transmission System (FACTS), High Voltage Direct Current (HVDC) and power quality.

Dr. Singh is a fellow of Institute of Electrical and Electronics Engineers (FIEEE), Indian National Academy of Engineering (FINAE), National Academy of Science, India (FNASI), the Institution of Engineers (India) (FIE), and the Institution of Electronics and Telecommunication Engineers (FIETE), a life Member of the Indian Society for Technical Education (LMISTE), the System Society of India (LMSSI), and the National Institution of Quality and Reliability.

Design and Control of Small Power Standalone Solar PV Energy System

Neha Adhikari [1] Bhim Singh [2] A.L.Vyas[1]

Abstract– This paper deals with the analysis, design and control of a small power standalone solar photovoltaic (SPV) generating system. A PV array of 33V-43.2V is taken as an input and its output voltage is achieved as 360V dc using a flyback converter. The battery is charged at this voltage and using a single-phase voltage source inverter (VSI) it is converted into a single phase ac of 220Vac, 50 Hz. A closed loop control for maximum power point tracking (MPPT) and a PI (Proportional Integral) controller for output voltage control of VSI are used to optimize the system. Perturbation and observation method is applied for MPPT. The simulation of the developed model of the designed SPV system is performed in Matlab platform. Simulation results are presented with linear and nonlinear loads to demonstrate its satisfactory performance.

Keywords–Battery, Isolated flyback converter, Maximum power point tracking, Solar photovoltaic generation, Standalone system, Voltage source inverter.

I. Introduction

Solar photovoltaic (SPV) systems convert sunlight directly into electricity. A small power system enables home-owners to generate some or all of their daily electrical energy demand on their own roof top, exchanging daytime excess power for its energy needs in nights using SPV generation, if it is supported by the battery back-up. A SPV power system can be used to generate electric energy as a way of distributed generation (DG) for rural areas [1]. Several approaches have been proposed to improve efficiency of SPV system and to provide the proper ac voltage required by residential customers. For this purpose, dc-dc converters have been explored extensively to meet the required electric energy demands by these systems using a battery back-up [2]. A single switch flyback converter is designed with transformer isolation to charge the battery. The battery voltage is converted into ac supply using a voltage source inverter (VSI) and a filter. The design of a solar power system is a process which involves many variables that have to be adjusted in order to obtain optimized parameters for system components.

This paper demonstrates a step-by-step procedure to design different blocks that constitute the PV array, a controller for maximum power point tracking, a dc-dc flyback converter, a battery block, a VSI, a filter and the feedback control loop with PI (Proportional-Integral) controller. Detailed performance analysis is carried out for analyzing the controller performance in varying loading conditions [3].

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The analysis of the standalone system and results are obtained by simulations to supply average load of 300W power rating under variable input voltage range by a PV array.

II. Proposed System Configuration

Fig.1 shows a block diagram of the solar PV energy conversion system with a dc-dc converter, a battery, a VSI, an output filter and the feedback control loop.

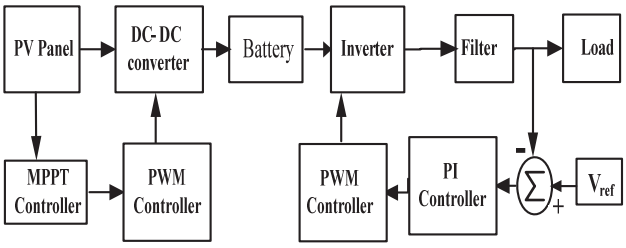

Fig.1: Block diagram of system configuration

Here, a flyback converter is operating in discontinuous conduction mode (DCM) with a very simple feedback control, which needs only output voltage sensing. The flyback converter in DCM operation is much frequently used than continuous conduction mode (CCM) operation, because the DCM contains an inherently smaller transformer magnetizing inductance, that responds more quickly and with a lower transient output voltage spike to rapid changes in output load current or input voltage. Here a flyback converter is used at the input voltage side with a feedback control loop that contains MPPT algorithm and generates PWM signal for the flyback converter and output of this converter is used to charge the battery. The perturbation and observation method is used for MPPT of PV panel. A feedback controller is applied to VSI under varying loads for regulating output voltage. The output voltage of VSI is compared with the reference output voltage and the error voltage signal is processed in the output voltage controller *G(s)*, which generates the PWM signal output for switching device of the VSI. Thus it a low cost solution for controlling duty cycle of switches and gives constant output voltage at varying loads [4-5]. Fig.2 shows the detailed circuit of proposed system.

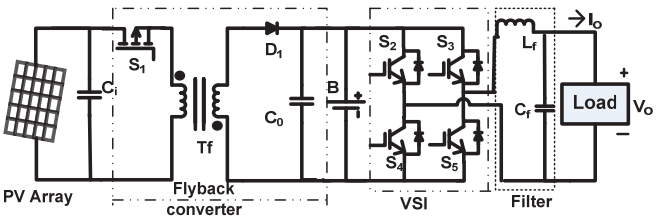

Fig.2: Proposed configuration of solar PV energy system with a flyback converter and a single-phase voltage source inverter

For modeling the PV array, the variation in solar radiation and temperature is also considered for analyzing its performance in different operating conditions.

III. Operating Principle of System Components

Solar-PV array characteristics are varying with environmental conditions and to capture the maximum energy, an MPPT controller is used with a flyback converter.

A. Flyback Converter

A flyback converter is a simplest topology of isolated dc-dc converter because it has only one switch, one transformer and there is no inductor at output stage. The topology of a flyback converter used for this system is shown in Fig.3.

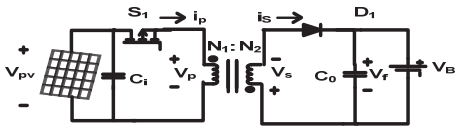

Fig.3: Circuit of flyback converter

A transformer is used here to eliminate any direct electrical connection between the PV array and the output of the converter power stage. It also has an advantage in terms of cost because of less number of components. Absence of an inductor at output side not only simplifies the circuit but also makes transient response faster. Here a transformer is in inverting mode as polarity of both primary and secondary windings are not same. Basic operation of this converter can be stated as energy is stored in primary winding when the switch is turned on and transferred to secondary winding when the switch is turned off [6]. When switch S_1 is on, a voltage is applied on the primary winding and it causes primary winding current to rise. In this period, the secondary winding and diode are oppositely polarised, a load current is supplied by a capacitor. When switch S_1 is off, stored energy in the primary winding is transferred to secondary winding and load is fed by this secondary winding current. Equivalent circuits for the flyback converter operating in discontinuous mode are shown in Fig. 4 and different operating cases are shown in Table-1

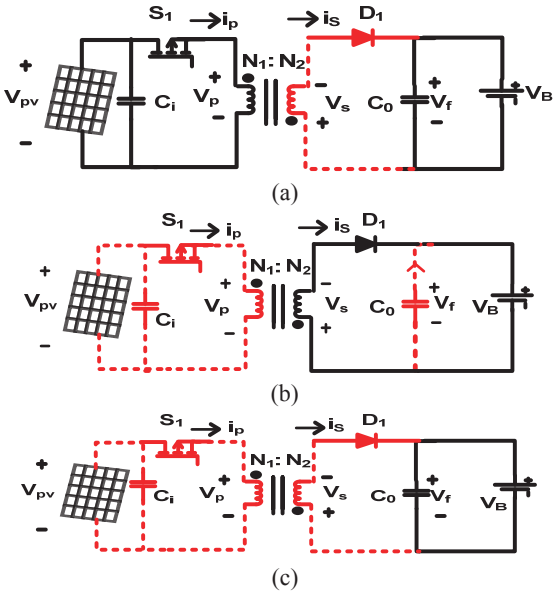

Fig. 4: Different operating conditions of flyback converter
(a) Case-1 (b) Case-2 (c) Case-3

Table 1 shows the different operating conditions of the flyback converter during one switching cycle. At initial stage, the current through the primary winding is zero.

Table1: Different operating conditions

	Case-1	Case-2	Case-3
Switch	On	Off	Off
Diode	Off	On	Off

Now in Case-1, the switch S_1 is turned on, diode D_1 is turn off, a voltage across the primary winding is V_p, a current through this increases linearly from zero. In Case-2, switch S_1 becomes turned off, diode D_1 turns on, a voltage across the primary winding becomes $-V_f$. Therefore, the current through the primary winding decreases linearly [6]. This current is reflected to the secondary winding of the transformer and flows through the diode. Once the diode current reaches zero, the diode begins to turn off and the current through the primary winding is zero until the switch is turned on. Thus one switching cycle is complete and as the switch is turned on the next cycle starts as same.

B. MPPT Algorithm

In proposed solar PV energy conversion system, the perturbation and observation method is applied in order to track maximum power point. It is an iterative method of obtaining maximum power point on operating curve of PV array. This algorithm operates by periodically measuring array terminal voltage and current and increments or decrements them after comparing it to the change in output power. Here operating voltage of PV array is perturbed by a finite increment value and due to this, the change in output power is observed. If this change is positive then it shows that operating point is moving closer to the maximum power point (MPP) else it moving away. This determines the direction of next perturbation [7]. The maximum power point can be determined when $dP/dV = 0$, where P is the output power and V is the output voltage of PV array. As the power-voltage relationship of a typical PV module is not linear, the maximum power point can be tracked using this algorithm when condition $dP/dV = 0$ is true for any value of solar radiation and temperature.

C. Voltage Source Inverter and Filter

A full-bridge voltage source inverter (VSI) is used here which consists of four switches. The function of the VSI is to convert 360 V_{dc} voltage supplied by the dc-dc converter into an ac of 220Vrms 50 Hz. Two complimentary PWM pulses are generated by the sinusoidal PWM controller. The basic principle in generating pulses with sinusoidal PWM is to divide the period of the desired sine wave output into number of intervals. In each interval, the control signal remains on for part of the time and off for the other part of the time. The ratio of the "on time" to "off time" at any given instant determines the amplitude of the desired output signal commonly known as duty cycle[8], which is fed to IGBTs (Insulated Gate Bipolar Transistors) of the VSI. One signal is sent in pair to IGBTs S_2 and S_5. The other signal is sent in IGBTs S_3 and S_4.This signal is fed like this as IGBTs $S_2$and S_5 remain on for some period and S_3, S_4 remain OFF for that time and vice-versa. Switches are one of the key components of the VSI. Its output pulse amplitude and waveform have relationship with the power switch of the switching characteristics. It affects the system efficiency and regulation characteristics. Fig.5 shows the topology of VSI and controller schematic.

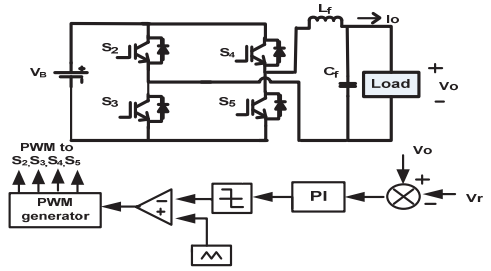

Fig.5: Topology of VSI and PI controller

The output signal from this full-bridge VSI is a pulse waveform which contains the desired output waveform along with frequency components at or around harmonics of the switching frequency. A low-pass filter is here utilized to extract the desired output voltage (50 Hz fundamental frequency) by separating it from the switching frequency.

D. PI Voltage Controller

To get good quality output voltage from a VSI a reasonably smooth dc voltage is required at input side, however this can not be guaranteed always so a PWM control technique at VSI side is used to overcome this problem. Fig. 5 shows the block diagram of the PI controller. An instantaneous voltage error is fed to a proportional integral controller. The integral component in this controller improves the tracking by reducing the instantaneous error between the reference and the actual voltages. The resulting signal is compared with a triangular carrier signal and the error is forced to remain within the band defined by the amplitude of the triangular waveform [9]. Thus it generates switching pulses for VSI.

IV. Design of System Components

The proposed system with a flyback converter, a battery, and a voltage source inverter is designed step by step procedure as follows.

A. PV Array Selection

Here a system is designed to feed an average load of 300W so the PV array is taken of total 750W and additional energy to charge the battery. Here three panels of 250W rated power are selected and connected in parallel to achieve the full power of 750W.

B. Design of Flyback Converter

In the flyback converter, during on time of the switch, the energy is stored in the flyback transformer while the load current is supplied by the output capacitor and during off time of the switch, the stored energy in the flyback transformer is delivered as the load current and to the capacitor for charging. In the flyback converter, the duty cycle is restricted up to 50%. This is due to time required to empty the flyback inductor flux to the output capacitor. The different components of the flyback converter are designed using basic equations. Table-2 shows the design equations for the proposed flyback converter [10-12]. Here this flyback converter is designed with a 100 kHz switching frequency in DCM operation. A battery is used at high voltage side of 360 V. The solar PV panel supplies at 85-120V with a little variation in the voltage to the converter, where it converts it to 360 V dc and the battery is charged at this voltage, which is supplied to the VSI for generating 220Vac at 50 Hz. Using equations given in Table 2, the parameters are calculated for the flyback converter at rated power of 750W.

Table 2: Design Equations and Calculated Values for Flyback Converter

Name of Component	Equation for Flyback	Calculated Value
Turns Ratio	$n=\frac{N_2}{N_1}=\frac{\eta D_{\max} V_{in}}{(1-D_{\max})V_o}$	1:4
Magnetizing Inductance	$L_{m(\max)}=\frac{V_{in}D_{\max}}{f_{sc}\Delta i_{Lm}}$	1.2 mH
Output Capacitance	$C_o=\frac{D_{\max}V_o}{f_{sc}R_L V_{cpp}}$	20 µF
Switching Frequency	f_{sc}	100 kHz

Considering, f_{sc} (Switching Frequency of converter switches)=100kHz, L_m (magnetizing Inductance)=1.2µH, V_o(output voltage)=360V, V_{in}(Input voltage)= 85-120 V, C_o (output capacitance, $n=N_2/N_1$ (Turns ratio for flyback transformer), P_{omax} (maximum output power)=750W, D_{max}(maximum duty cycle for operation in DCM)=0.5, η=90%, V_{cpp} (allowed ripple voltage across the output capacitor) =1V.

C. Design of Battery System

The battery plays an important role in case of the solar power system. The battery stores part of the energy generated by the solar PV power source and delivers to the load during the periods when the solar power source is unable to supply the power to the load due to any reason. The capacity of the battery depends on the daily load and days of autonomy [13]. To calculate the battery capacity for feeding 250W power at 360V, (1) is used as.

$$\text{Total Daily Load(AH)}=\frac{\text{No. of Amps}\times\text{No. of Hrs}}{\text{Day of Operation}} \quad (1)$$

The battery is considered to deliver a power for 16 hours. So here it is taken as 30 batteries of 12V, 11Ah in series connection.

D. Design of Voltage Source Inverter

A topology for a VSI chosen here is a full bridge VSI. After selecting the VSI topology, the next step is to select its device rating. To find rating of VSI switches a rated load condition as well as worst operating conditions of the load is considered. An average load of the system is considered as 300W. So the VSI should be designed to withstand at this load which gives the rated VSI output power 375VA and at a power factor of 0.8, at rated phase voltage = 220 V r.m.s. gives a peak current 2.1A. So considering worst case as a nonlinear load e.g. computer loads (SMPS) the device rating of the switches in VSI are taken as 600V, 10A. A closed loop control is also applied for changing the duty cycle of the VSI switches for maintaining the output voltage of the system under

varying load conditions using reference sine wave voltage and a PI voltage controller [14].

E. Design of PI Controller

A PI controller can be used for balancing the load variation. It performs satisfactorily during transient under limited operating range and the steady state performance is also excellent. Proportional and integral gains are constants and they are fine tuned for specific operating condition. Here Ziegler-Nichols method is used for tuning of PI controller. Ziegler and Nichols have suggested that the value of K_p (proportional gain) and K_i (integral gain) can be found by setting the controller in the proportional mode and increasing the gain until an oscillation takes place [15]. The point is then obtained from measurement of the gain and the oscillation frequency. According to this method the proportional gain K_p is increased until continuous oscillation is achieved. The period of oscillation (P_c) is measured when the amplitude of oscillation is quite small and the crossover frequency (ω_c), the critical gain (G_c) is obtained from the Nyquist and root locus plot. Characteristic equation of PI controller can be shown as (2). After obtaining all these values, Ziegler and Nichols have suggested [15], that one can set the values of the parameters K_p, K_i according to (3) and (4) as,

$$G_{PI}(S) = \frac{K_p K_i S + K_p}{K_i S} \tag{2}$$

$$K_p = 0.5 G_c \tag{3}$$

$$K_i = 0.5 P_c \tag{4}$$

The G_c is critical gain of the system. P_c is period of oscillation. G_{PI} is gain of PI controller. It is observed that for optimum performance of the controller to guarantee intersections between the triangular and the error signal, it is necessary to set the proportional gain K_p, to unity and the integral gain K_i, equal to the frequency of the triangular waveform. Here they are determined and set accordingly, K_p is set to 1 and K_i is 0.0005.

F. Design of Low Pass Filter

A low-pass (LC) filter is used to get the desired output voltage (50 Hz fundamental frequency) by separating it from the switching frequency and rejects any frequency above its cutoff frequency. The cut off frequency can be obtained by equation (5) as.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

The switching harmonics resulted from 20 kHz switching frequency are around half the switching frequency. The switching frequency is selected at 20 kHz to provide clean 50Hz fundamental frequency [16]. The design of an LC filter for VSI is carried out with following equations. Now, the peak inductor current, which is the maximum current that can pass through the inductor can be calculated using (6) as [17],

$$I_L = \frac{2V_m}{R_{L\min}} \tag{6}$$

$R_{L\min}$ is the minimum value of load resistance, and V_m is the peak magnitude of the output voltage. The value of filter capacitor for specific switching frequency may be calculated with the (7) as [17],

$$C = \frac{V_m}{2R_{L\min} f_{si} \Delta v} \tag{7}$$

Δv is the voltage ripple of the output voltage. From the volt–second balance of the inductor, the ratio of "on time" (T_{on}) and "off time" (T_{off}) which determines the duty cycle for VSI is calculated using (8) as [17],

$$\frac{T_{on}}{T_{off}} = \frac{V_d + V_o}{V_d - V_o} \tag{8}$$

where ,V_d is dc link voltage and V_o is output voltage of VSI.

Using the value of minimum switching frequency, the ration of on time and off time can be set as shown in (9) as [17-19],

$$\frac{T_{on}}{T_{off}} = \frac{1}{f_{si}} \tag{9}$$

The value of the inductor is calculated by using (8), (9) and (10).

$$L = \frac{V_d - V_o}{I_L} T_{on} \tag{10}$$

The configuration of LC low pass filter used in this system shown in Fig. 2 and calculated value of L_f=3.8mH and C_f=7.2μF considering V_d= 360V, V_o= 220V, f_{si}= 20kHz, ΔV= 1V, R_{Lmin}= 150Ω for a load of 300W.

V. Modeling and Simulation of System

Different components of solar-PV energy conversion system are modeled in Matlab platform. For maximum power point tracking, a perturbation and observation algorithm is used.

A. Modeling of PV Cell

The complete behavior of PV cells can be described by five model parameters (I_{pv}, N, I_o, R_a, R_b) which represent the physical behavior of PV cell/module. These five parameters of PV cell/module are functions of two environmental conditions of solar irradiance and temperature. Fig.6 shows an equivalent circuit model of PV array.

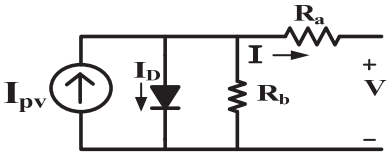

Fig.6: Equivalent circuit of PV array

The PV cell is a nonlinear device and can be represented as a current source, parallel diode, however a practical PV cell model includes the connection of series and parallel internal resistance [20], namely R_a and R_b, which is expressed as equation (11) as.

$$I = I_{pvt} - I_d \left\{ \exp\left(\frac{V + R_a}{V_t N} \right) - 1 \right\} \tag{11}$$

In (11), I = output current of PV, V =output voltage of PV, $V_t = N_s KT/q$ = thermal voltage of array, Ns=number of cells connected in series, q = electron charge (1.60 e^{-19} C), k = the Boltzmann constant (1.380 e^{-23}J K^{-1}), T = temperature of the p-n junction (K), K and N =the diode

ideality constant. Here I_{pvt} is current produced by a PV cell, it is function of solar irradiance and temperature. The diode saturation current, I_d is function of temperature, which is expressed in (12) and (13).

The performance of the transformer describing the voltage and current of primary/secondary winding of the transformer under linear load condition is shown in Fig.16. The solar radiation is considered constant at 1000 W/m^2. Due to battery connected in the system with the dc-dc converter it is not affected under varying load conditions of the system.

$$I_{pvt} = (I_{pvt} + K_a \Delta T)\frac{G_1}{G_2} \quad (12)$$

$$I_d = \frac{I_{sc} + K_a \Delta T}{\exp\left[\frac{V_{oc} + K_b \Delta T}{N V_t}\right] - 1} \quad (13)$$

The I_{pvt} is the light generated current at the nominal condition which are 25°C and 1000 W /m^2, $\Delta T = T_1 - T_2$, T_1 and T_2 = actual and nominal temperature in Kelvin, G_1 (W/ m^2) =value of solar irradiation by the PV surface and G_2 =the nominal value of solar irradiation, K_a = short-circuit current/temperature coefficient, K_b = open-circuit voltage/temperature coefficient, I_{SC} = short-circuit current, V_{OC} = open-circuit voltage under the nominal condition. The value for series resistance R_a is taken as 0.1Ω and R_b is 500Ω.

Using these equations, PV array is modeled in Matlab, from the data sheet of SPSM250 solar panel, characteristics of solar panel is taken for modeling the system [20-21]. Results for different conditions of temperature and solar irradiance are obtained through simulation. Table-3 shows the parameters taken from datasheet.

Table 3: Parameters of PV Array

Peak Power	250 W
Open Circuit Voltage	43.21 V
Short Circuit Current	7.63 A
Voltage At Max. Power	35.5 V
Current At Max. Power	7.04 A
No. of Cells	72

Characteristics of PV array are modeled under varying conditions of temperature which is 0ºC to 50ºC and solar irradiance is changing from 200 W/m^2 to 1000 W/m^2. The results obtained for these conditions and performance characteristics of this model are shown in Figs. 7-8.

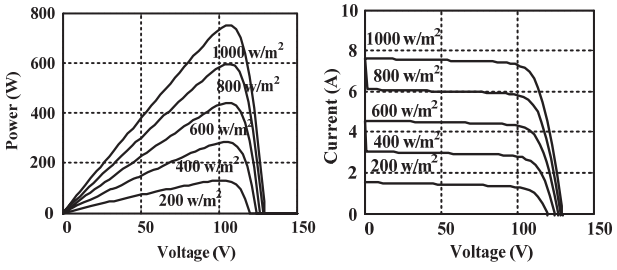

Fig.7: P-V and I-V characteristics of PV array with different solar radiation

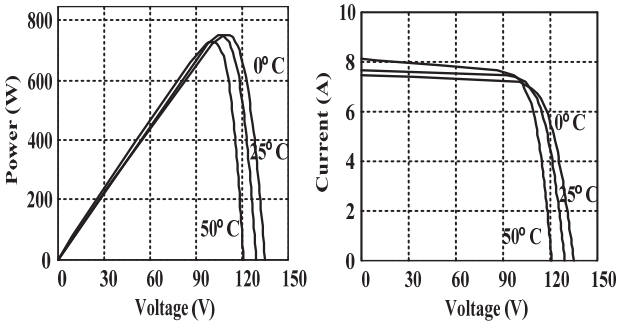

Fig.8: P-V and I-V characteristics of PV array with different temperature conditions

B. Modeling of Battery

For modeling of the battery here, its Thevenin's equivalent circuit model is used. Fig.9 shows the Thevenin's equivalent model of the battery, where R_{eq} is the equivalent series resistance of parallel/series combination of a battery which is usually a small value. For this analysis R_{eq}=0.01Ω. The parallel circuit of R and C describe the stored energy and voltage during charging or discharging [22]. R in parallel with C, represents discharging of the battery, the self discharging current of a battery is small, so the resistance R is large and the typical value of R for this battery is used 10kΩ.

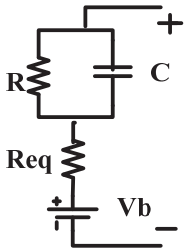

Fig.9: Equivalent model of battery

Here the battery is considered of having 450 W for 16 hours peaking capacity, and variation in the voltage of order of 355 V-365 V. The battery stores the energy from PV system. Its energy is represented in kWh. A capacitor is used in an equivalent circuit for modeling of battery, and the value of capacitance is calculated using (14) as.

$$C = \frac{kWh \times 3600 \times 16}{0.5(V_{\max}^2 - V_{\min}^2)} \quad (14)$$

V_{max} is the maximum voltage of the battery fully charged and V_{min} is the minimum voltage of the battery when it is fully discharged [22].

The calculated value of C for this battery from equation (14) is C=7200F. The main function of controller is to regulate the current for the battery charging due to variation in the voltage supplied by the PV array. A control circuit can also be added, which protects the overcharging, deep discharge and reverse current flow during discharge [23].

B. Modeling of MPPT Algorithm

For modelling of MPPT its basic principle is considered and Fig.10 shows the operating flowchart of P&O algorithm, V_{pv} and I_{pv} are output voltage and current of PV array and k is the value of variation in voltage to compute next perturbation.

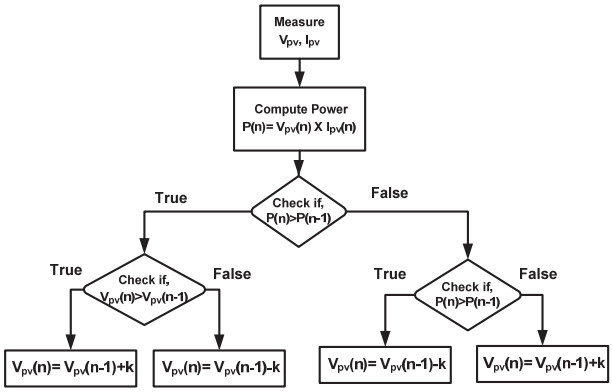

Fig. 10: Flowchart of MPPT

For a given perturbation on the voltage of the panel leads to an increase (decrease) the output power of the PV, then the subsequent perturbation is generated in the same (opposite) direction. As a consequence of the P&O algorithm, when the MPP is reached, the system may oscillate around it and this problem is overcome by reducing the perturbation step size. Here for modeling of this algorithm is carried out in Matlab, the three-point weight comparison method is used, where the perturbation direction is decided by comparing the PV output power on three points of the characteristics curve.

B. Matlab Model of Proposed System

The modeling of the complete system (detailed data are given in Appendices) is carried out in Matlab/Simulink. A PV array is modeled with consideration of changing conditions of temperature and solar insolation, which is modelled as a subsystem having input as temperature and solar insolation and panel are connected through flyback converter.

VI. Result and Discussion

A simulation model is developed of solar PV based power system with a flyback converter in discontinuous mode of operation with maximum power tracking controller for extracting maximum power from PV array and a PI controller in feedback of VSI for load variation in output. Results are obtained for different load conditions. Fig. 11 shows a harmonic analysis of the output voltage and current at linear loads which gives Total Harmonic Distortion (THD) of 2.45% and 2.21% for voltage and current respectively.

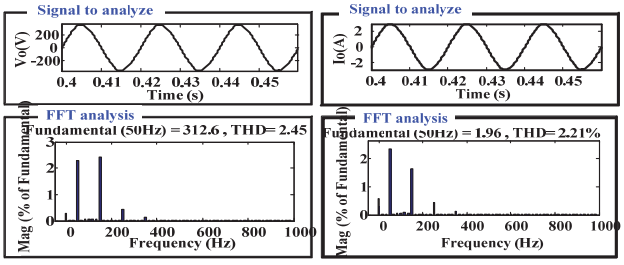

Fig.11: Waveforms and Harmonic analysis of output voltage and current at linear load

Fig.12 shows the performance of the system at a linear load under varying solar radiations. In this figure it is observed that along with the solar radiations, the output voltage of the solar-PV array is varying, while the output voltage of the flyback converter remains same. Thus it validates the performance of the MPPT controller.

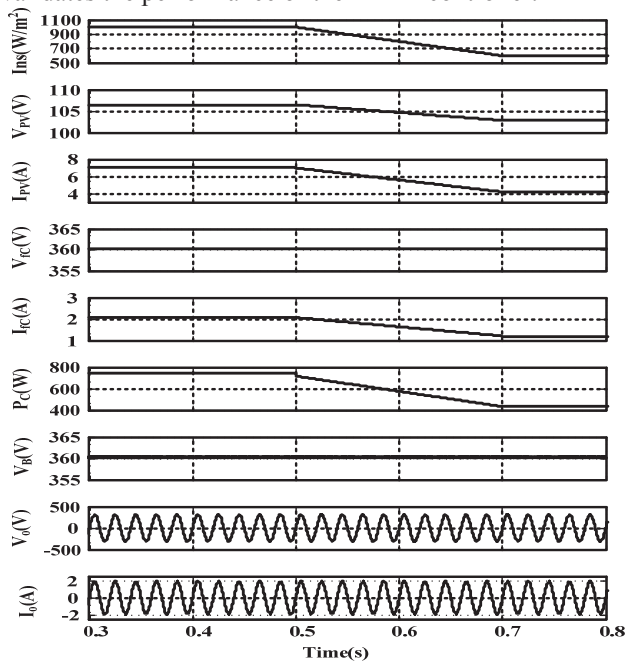

Fig.12 Performance of the system with linear load

In these figures, V_{pv} is output voltage of PV array, I_{pv} is output current of PV array, V_p and V_s are voltages of primary, secondary windings of transformer. I_p and I_s are currents of primary, secondary windings of transformer. V_{fC} is output voltage of the flyback converter. P_C is power. I_{fC} output current of the flyback converter. V_o and I_o are output voltage and current of VSI. For analyzing the performance of this system under nonlinear load condition, an SMPS (Switched Mode Power Supply) is used as a nonlinear load because it has highly nonlinear characteristics and widely used in many applications. Fig.13 shows the results of the output voltage and current of VSI at nonlinear load, which has a crest factor of 2.7 of output load current.

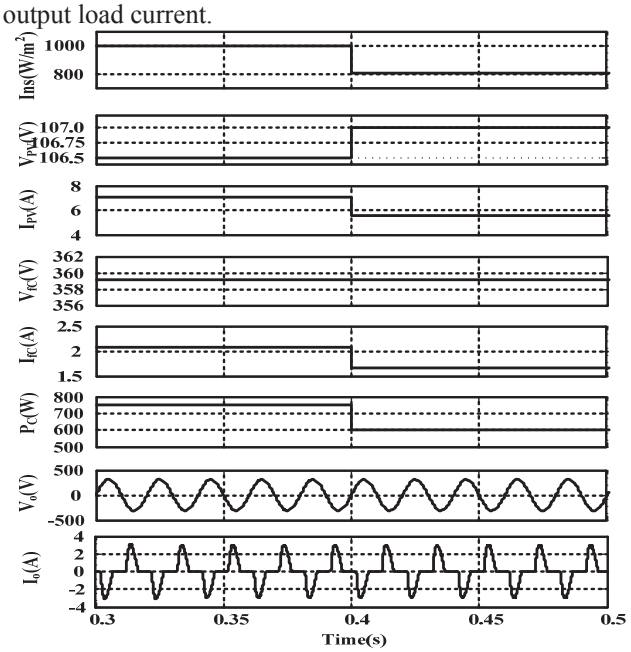

Fig.13: Performance of the system at nonlinear load

Fig.14 shows the harmonic analysis of voltage and current at nonlinear load condition. The voltage THD is as 3.13% only and even when the current THD is as 68.34%.

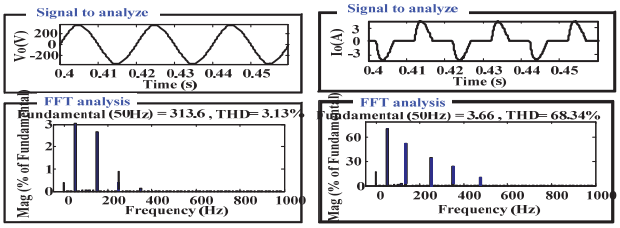

Fig.14: Waveforms and Harmonic analysis of output voltage and current at non-linear load

The system is designed for standalone operation thus the variation in the consumer load is analyzed and the results are presented in Fig.15.

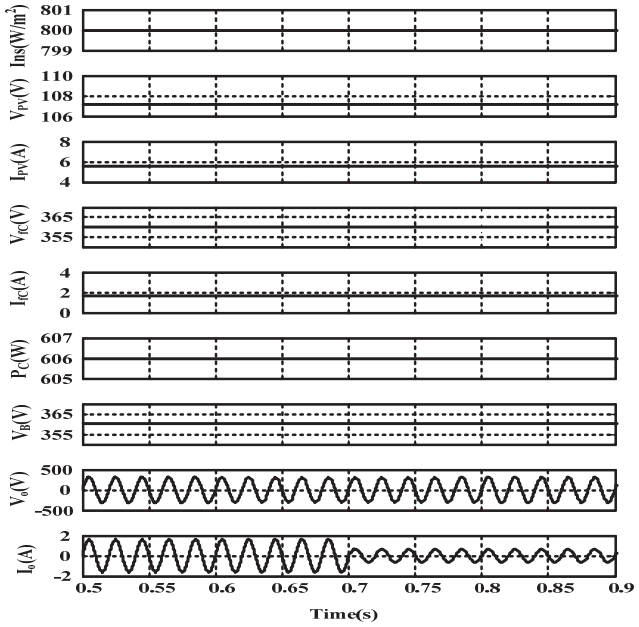

Fig.15: Performance of the system at load variation

The load is varying at time 0.7s and the solar radiation considered remains same at 800 W/m^2, thus the output current changes at the 0.7s and the output voltage is observed as not affected by the load variation. These results validate the performance of the output controller which maintains the output voltage constant in case of load variation load.

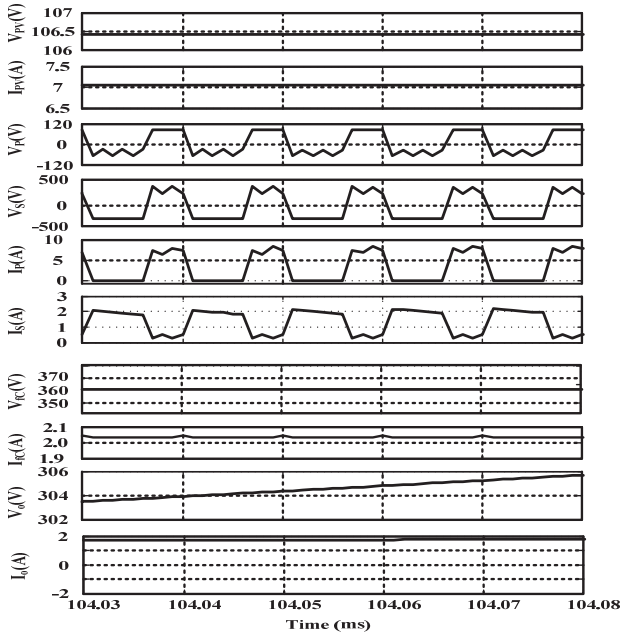

Fig.16: Performance of the system with transformer characteristics

The performance of the transformer describing the voltage and current of primary/secondary winding of the transformer under linear load condition is shown in Fig.16. The solar radiation is considered constant at 1000 W/m^2. Due to battery connected in the system with the dc-dc converter it is not affected under varying load conditions of the system.

The performance of the battery during charging and discharging is shown in Fig.17. It shows that the battery takes charging time with maximum power tracking of 8 hours and capable of supplying full load up to 16 hours, where V_b is the voltage of battery, I_b is current of battery and SOC is charging condition and time is in hours.

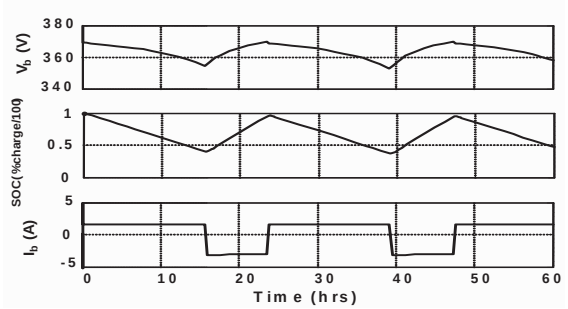

Fig.17: Performance characteristics of battery

VII. Conclusion

The design and performance study of a standalone solar PV energy system have been carried out using a flyback converter, battery and a single phase voltage source inverter. The battery charging has been achieved through maximum power point tracking which gives sufficient backup for 16 hours. The controller performance under various load conditions has been investigated and it has given required response under nonlinear load conditions. The results obtained for harmonic distortion of this system for both linear and nonlinear loads are within the 5% range specified by IEEE-519 standard. Performance of the system for the load variation is improved due to feedback PI control applied to VSI, so depending on the requirement one can choose it for low power application.

Appendices

A. PV Panel parameters

Power = 750W, Open circuit voltage = 129.63V, Short circuit current= 7.63A, Voltage at maximum power = 106.5V, Current at maximum power = 7.04A.

B. Flyback converter

Turns ratio, N_2/N_1= 1:4, magnetizing Inductance, L_m= 1.2 mH, Output capacitance, C_o = 20 µF, Switching Frequency, f_{sc}= 100 kHz.

C. Output Filter

Filter Inductance, L_f= 3.8µH, Filter Capacitance, C_f = 7.2µF.

D. Non-linear load

Fig. 18 shows a nonlinear load used in this system. SMPS with forward converter in isolated mode is considered as R_{eq} for 300W power application, C_s=5mF.

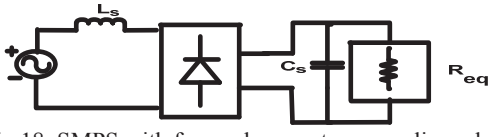

Fig.18: SMPS with forward converter as nonlinear load

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BIOGRAPHIES

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A Refined Space Vector PWM Signal Generation for Seven-Level Inverter

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Abstract– A refined space vector modulation scheme for a seven-level inverter system for dual-fed induction motor drive, using only the instantaneous sampled reference signals is presented in this paper. The dual-fed structure is realized by opening the neutral-point of the conventional squirrel cage induction motor. The seven-level inversion is obtained by feeding the dual-fed induction motor with two symmetrical three-level inverters from both ends. The proposed space vector pulse width modulation technique does not require the sector information and look-up tables to select the appropriate switching vectors. The inverter leg switching times are directly obtained from the instantaneous sampled reference signal amplitudes and centers the switching times for the middle space vectors in a sampling time interval, as in the case of conventional space vector pulse width modulation.

Keywords– dual-fed induction motor, seven-level inverter, space vector PWM, sampled sinusoidal reference signals, middle space vectors.

I. Introduction

The two most widely used pulse width modulation (PWM) schemes for multilevel inverters are the carrier-based sine-triangle PWM (SPWM) scheme and the space vector PWM (SVPWM) scheme. These modulation schemes have been extensively studied and compared for the performance parameters with two level inverters [1],[2]. The SPWM schemes are more flexible and simpler to implement, but the maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage [2]. In SVPWM schemes, a reference space vector is sampled at regular intervals to determine the inverter switching vectors and their time durations, in a sampling time interval. The SVPWM scheme gives a more fundamental voltage and better harmonic performance compared to the SPWM schemes [3-5]. The maximum peak of the fundamental component in the output voltage obtained with SVPWM is 15% greater than with the SPWM scheme [2],[3]. But the conventional SVPWM scheme requires sector identification and look-up tables to determine the timings for various switching vectors of the inverter, in all the sectors [3],[4]. This makes the implementation of the SVPWM scheme quite complicated. It has been shown that, for two-level inverters, a SVPWM like performance can be obtained with a SPWM scheme by adding a common mode voltage of suitable magnitude, to the sinusoidal reference signals [4],[5]. A simplified method, to determine the correct offset times for centering the time durations of the middle space vectors, in a sampling time interval, is presented [8], for the two-level inverter. The inverter leg switching times are calculated directly from the sampled amplitudes of the sinusoidal reference signals with considerable reduction in the computation time [8].

The SPWM scheme, when applied to multilevel inverters, uses a number of level-shifted carrier signals to compare with the sinusoidal reference signals [9]. The SVPWM for multilevel inverters [10],[11] involves mapping of the outer sectors to an inner subhexagon sector, to determine the switching time interval, for various space vectors. Then the switching space vectors corresponding to the actual sector are switched, for the time durations calculated from the mapped inner sectors. It is obvious that such a scheme, in multilevel inverters, will be very complex, as a large number of sectors and inverter vectors are involved. This will also considerably increase the computation time.

A modulation scheme is presented in [12], where a fixed common mode voltage is added to the reference signal throughout the modulation range. It has been shown [13] that this common mode addition will not result in a SVPWM-like performance, as it will not centre the middle space vectors in a sampling interval. The common mode voltage to be added in the reference phase voltages, to achieve SVPWM-like performance, is a function of the modulation index for multilevel inverters [13]. A SVPWM scheme based on the above principle has been presented [14], where the switching time for the inverter legs is directly determined from sampled sinusoidal reference signal amplitudes. This technique reduces the computation time considerably more than the conventional SVPWM techniques do, but it involves region identifications based on modulation indices. While this SVPWM scheme works well for a three-level PWM generation, it cannot be extended to multilevel inverters of levels higher than three, as the region identification becomes more complicated. A carrier-based PWM scheme has been presented [15], where sinusoidal references are added with a proper offset voltage before being compared with carriers, to achieve the performance of a SVPWM. The offset voltage computation is based on a modulus function depending on the DC link voltage, number of levels and the sinusoidal reference signal amplitudes. A SVPWM scheme is presented [18], where the switching time for the inverter legs is directly determined from sampled sinusoidal reference signal amplitudes for five-level inverter. A carrier based SPWM scheme is presented [19],[20], for five-level and seven-level inverter.

The objective of this paper is to present an implementation scheme for PWM signal generation for seven-level inverter system for dual-fed induction motor, similar to the

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SVPWM scheme. In the proposed scheme, the dual-fed induction motor is fed with two symmetrical three-level inverters from both ends. The PWM switching times for the inverter legs are directly derived from the sampled amplitudes of the sinusoidal reference signals. A simple way of adding an offset voltage to the sinusoidal reference signals, to generate the SVPWM pattern, from only the sampled amplitudes of sinusoidal reference signals, is explained. The proposed SVPWM signal generation does not involve checks for region identification, as in the SVPWM scheme presented in [14]. Also, the algorithm does not require either sector identification or look-up tables for switching vector determination as are required in the conventional multilevel SVPWM schemes [10],[11]. Thus the scheme is computationally efficient when compared to conventional multilevel SVPWM schemes, making it superior for real-time implementation.

II. Seven-Level Inverter Scheme for the Dual-Fed Induction Motor

The power circuit of the proposed drive is shown in Fig. 1. Two symmetrical three-level inverters, Inverter-A and Inverter-B feed the dual-fed induction motor. The inverter-A is composed of two conventional two-level inverters INV-1 and INV-2 in cascade. The Inverter-B is composed of two conventional two-level inverters INV-3 and INV-4 in cascade. The DC link voltages of INV-1, INV-2, INV-3 and INV-4 are $(2/6)E_{dc}$, $(2/6)E_{dc}$, $(1/6)E_{dc}$ and $(1/6)E_{dc}$ respectively, where E_{dc} is the DC link voltage of an equivalent conventional single two-level inverter drive.

The leg voltage E_{A2n} of phase-A attains a voltage of $(2/6)E_{dc}$ if the switches S_{21} and S_{14} are turned on. The leg voltage E_{A2n} of phase-A attains a voltage of $(4/6)E_{dc}$ if the switches S_{21} and S_{11} are turned on. The leg voltage E_{A2n} of phase-A attains a voltage of zero volts if the switch S_{24} is turned on. Thus the leg voltage E_{A2n} attains three voltages of 0, $(2/6)E_{dc}$ and $(4/6)E_{dc}$, which is basic characteristic of a 3-level inverter.

The leg voltage $E_{A4n'}$ of phase-A attains a voltage of $(1/6)E_{dc}$ if the switches S_{41} and S_{34} are turned on . The leg voltage $E_{A4n'}$ of phase-A attains a voltage of $(2/6)E_{dc}$ if the switches S_{41} and S_{31} are turned on . The leg voltage $E_{A4n'}$ of phase-A attains a voltage of zero volts if the switch S_{44} is turned on. Thus the leg voltage $E_{A4n'}$ attains three voltages of 0, $(1/6)E_{dc}$ and $(2/6)E_{dc}$, which is basic characteristic of a 3-level inverter.

Thus, one end of dual-fed induction motor may be connected to a DC link voltage of either zero or $(2/6)E_{dc}$ or $(4/6)E_{dc}$ and other end may be connected to a DC link voltage of either zero or $(1/6)E_{dc}$ or $(2/6)E_{dc}$ .When both the inverters Inverter-A and Inverter-B drive the induction motor from both ends, seven different levels are attained by each phase of the induction motor. If we assume that the points n and n' are connected, the seven levels generated for phase-A are shown in Table1.

III. Voltage Space Vectors of Proposed Inverter

At any instant, the combined effect of 120^0 phase shifted three voltages in the three windings of the induction motor could be represented by an equivalent space vector. This space vector Es, for the proposed scheme is given by

$$Es = E_{A2A4} + E_{B2B4}.e^{j(2\pi/3)} + E_{C2C4}.e^{j(4\pi/3)} \quad (1)$$

By substituting expressions for the equivalent phase voltages in (1),

$$Es = (E_{A2n} - E_{A4n'}) + (E_{B2n} - E_{B4n'}).e^{j(2\pi/3)} + (E_{C2n} - E_{C4n'}).e^{j(4\pi/3)} \quad (2)$$

This equivalent space vector Es can be determined by resolving the three phase voltages along mutually perpendicular axes, d-q axes of which d-axis is along the A-phase (Fig. 2). Then the space vector is given by

$$Es = Es(d) + jEs(q) \quad (3)$$

Where Es(d) is the sum of all voltage components of E_{A2A4}, E_{B2B4} and E_{C2C4} along the d-axis and Es(q) is the sum of the voltage components of E_{A2A4}, E_{B2B4} and E_{C2C4} along the q-axis. The voltage components Es(d) and Es(q) can be thus expressed by the following transformation,

$$Es(d) = E_{A2A4}(d) + E_{B2B4}(d) + E_{C2C4}(d) \quad (4)$$

$$Es(q) = E_{B2B4}(q) + E_{C2C4}(q) \quad (5)$$

$$\begin{bmatrix} Es(d) \\ Es(q) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} E_{A2A4} \\ E_{B2B4} \\ E_{C2C4} \end{bmatrix} \quad (6)$$

By substituting expressions for the equivalent phase voltages in (6),

$$\begin{bmatrix} Es(d) \\ Es(q) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} E_{A2n} - E_{A4n'} \\ E_{B2n} - E_{B4n'} \\ E_{C2n} - E_{C4n'} \end{bmatrix} \quad (7)$$

The inverters can generate different levels of voltage vectors in the three phases of induction motor depending upon the condition of the switchings of inverter and for each of the different combinations of leg voltages, E_{A2n}, E_{B2n} and E_{C2n} for the inverter-A and $E_{A4n'}$, $E_{B4n'}$ and $E_{C4n'}$ for the inverter-B. The different equivalent voltage space vectors can be determined using (3) and (7). The possible combinations of space vectors will occupy different locations as shown in Fig. 3. There are in total 127 locations forming 216 sectors in the space vector point of view. The resultant hexagon (Fig. 3) can be divided into six layers: layer-1(innermost layer); layer-2(next outer layer); layer-3(layer outside layer-2); layer-4 (layer outside layer-3); layer-5 (layer outside layer-4) and layer-6 (outermost layer).

Table1: The seven levels realized in the phase-A winding

Leg-voltage of phase A (E_{A2n})	Leg-voltage of phase A ($E_{A4n'}$)	Motor phase voltage $E_{A2A4} = E_{A2n} - E_{A4n'}$	Level
0	$(2/6)E_{dc}$	$-(2/6)E_{dc}$	Level 1
0	$(1/6)E_{dc}$	$-(1/6)E_{dc}$	Level 2
0	0	0	Level 3
$(2/6)E_{dc}$	$(1/6)E_{dc}$	$(1/6)E_{dc}$	Level 4
$(2/6)E_{dc}$	0	$(2/6)E_{dc}$	Level 5
$(4/6)E_{dc}$	$(1/6)E_{dc}$	$(3/6)E_{dc}$	Level 6
$(4/6)E_{dc}$	0	$(4/6)E_{dc}$	Level 7

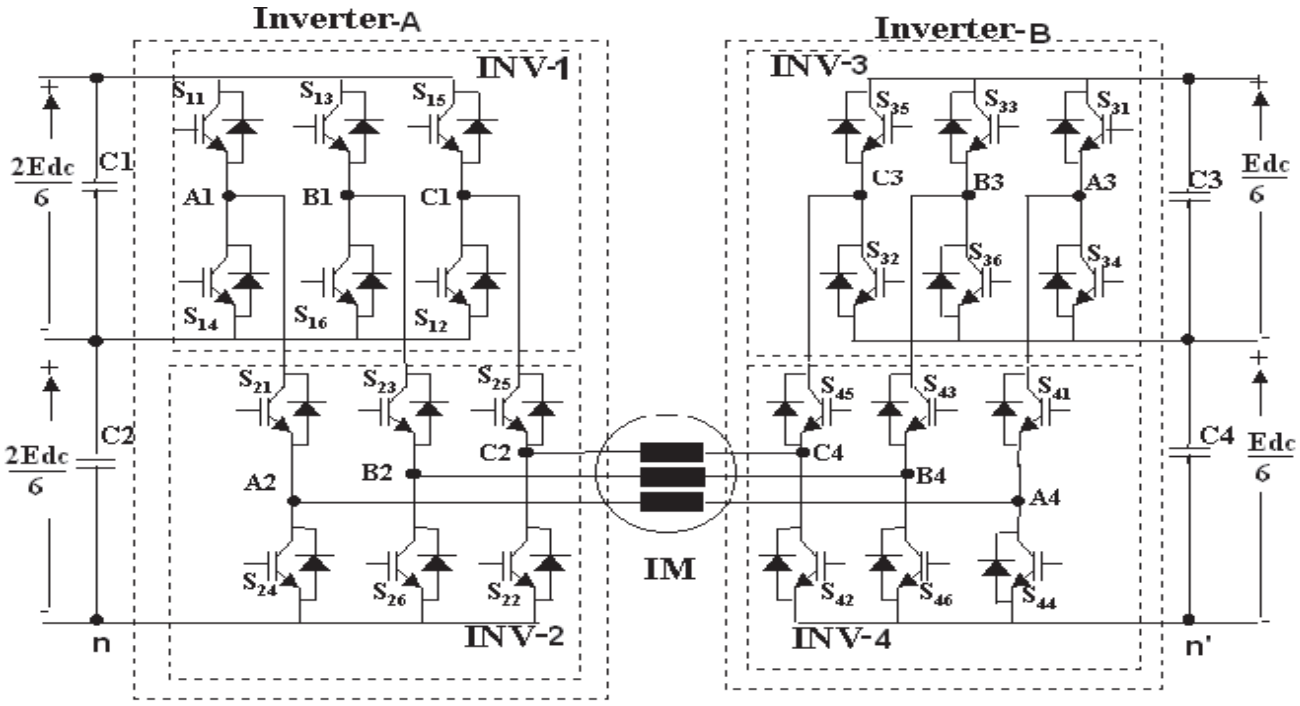

Fig. 1: Schematic circuit diagram of the proposed 7- level inverter drive scheme.

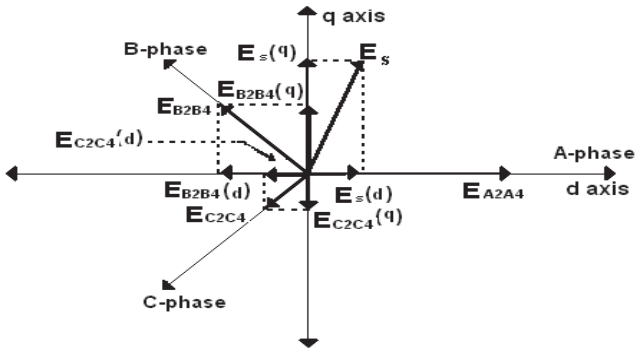

Fig. 2: Determination of equivalent space vector from phase voltages

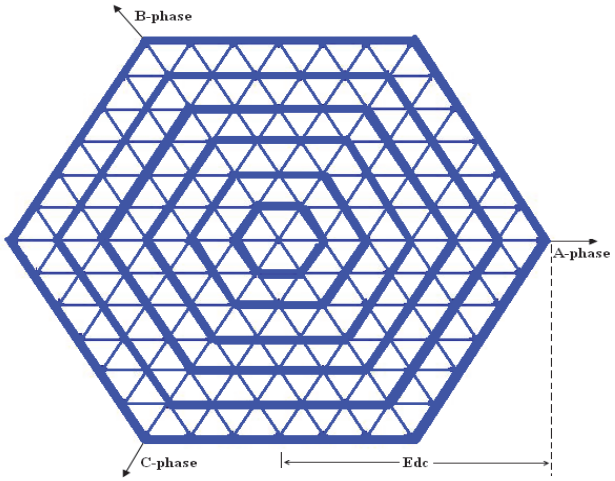

Fig. 3: The voltage space vector locations and layers for the proposed drive

IV. Effect of Common-Mode Voltage in Space Vector Locations

In the above analysis to generate the different levels and the space vector locations, the points n and n' are assumed to be connected. When the points n and n' are not connected (as in the proposed topology, Fig. 1), the actual motor phase voltages are

$$E_{A2A4} = E_{A2n} - E_{A4n'} - E_{n'n} \quad (8)$$

$$E_{B2B4} = E_{B2n} - E_{B4n'} - E_{n'n} \quad (9)$$

$$E_{C2C4} = E_{C2n} - E_{C4n'} - E_{n'n} \quad (10)$$

$E_{n'n}$ is the common-mode voltage and is given by

$$E_{n'n} = \frac{1}{3}(E_{A2n} + E_{B2n} + E_{C2n}) - \frac{1}{3}(E_{A4n'} + E_{B4n'} + E_{C4n'}) \quad (11)$$

Substituting these expressions in (1)

$$Es = (E_{A2n} - E_{A4n'} - E_{n'n}) + (E_{B2n} - E_{B4n'} - E_{n'n}).e^{j(2\pi/3)} + (E_{C2n} - E_{C4n'} - E_{n'n}).e^{j(4\pi/3)} = (E_{A2n} - E_{A4n'}) + (E_{B2n} - E_{B4n'}).e^{j(2\pi/3)} + (E_{C2n} - E_{C4n'}).e^{j(4\pi/3)} - (E_{n'n} + E_{n'n}.e^{j(2\pi/3)} + E_{n'n}.e^{j(4\pi/3)})$$

In this equation

$$(E_{n'n} + E_{n'n}.e^{j(2\pi/3)} + E_{n'n}.e^{j(4\pi/3)}) =$$

$$E_{n'n} - \frac{1}{2}E_{n'n} - \frac{1}{2}E_{n'n} = 0$$

and the equation then reduces to

$$Es = (E_{A2n} - E_{A4n'}) + (E_{B2n} - E_{B4n'}).e^{j(2\pi/3)} + (E_{C2n} - E_{C4n'}).e^{j(4\pi/3)}$$

This expression of Es is the same as (2), where the points n and n' are assumed to be connected. The above analysis depicts that the common-mode voltage present between the points n and n' does not effect the space vector locations. This common-mode voltage will effect only in the diversity of space vectors in different locations.

V. Proposed SVPWM in Linear Modulation Range

For two-level inverters, in the SPWM scheme, each sinusoidal reference signal is compared with the triangular carrier signal and the individual phase voltages are generated [1]. To attain the maximum possible peak amplitude of the fundamental phase voltage, a common offset voltage, Eoffset1 is added to the sinusoidal reference signals [5],[12], where the magnitude of Eoffset1 is given by

$$Eoffset1 = -(E\max + E\min)/2 \qquad (12)$$

Where Emax and Emin are the maximum and minimum magnitudes of the three sampled sinusoidal reference signals respectively, in a sampling time interval. The addition of this common offset voltage, Eoffset1, results in the active space vectors being centered in a sampling time interval, making the SPWM scheme equivalent to the SVPWM scheme [3]. In a sampling time interval, the sinusoidal reference signal which has lowest magnitude crosses the triangular carrier signal first, and causes the first transition in the inverter switching state. While the sinusoidal reference signal, which has the maximum magnitude, crosses the triangular carrier signal last and causes the last switching transition in the inverter switching states in a two-level SVPWM scheme [5],[13]. Thus the switching times of the active space vectors can be determined from the sampled sinusoidal reference signal amplitudes in a two-level inverter system [8].

The SPWM scheme, for seven-level inverter, sinusoidal reference signals are compared with symmetrical level shifted six triangular carrier signals for PWM generation [9]. After addition of offset voltage Eoffset1 to the sinusoidal reference signals, the modified sinusoidal reference signals are shown in fig. 4 along with six triangular carrier signals. The sinusoidal reference signals cross the triangular carrier signals at different instants in a sampling time interval Ts (Fig. 4). Each time a sinusoidal reference signal crosses the triangular carrier signal, it causes a change in the inverter switching state. The changes in phase voltage and their time intervals are shown in Fig. 5 in a sampling time interval Ts. The sampling time interval Ts can be split into four time intervals t_{01}, t_1, t_2 and t_{02}. The time intervals $t_{01}$and t_{02} are the time durations for the start and end inverter space vectors respectively, in a sampling time interval Ts. The time intervals t_1 and t_2 are the time durations for the middle inverter space vectors (active space vectors), in a sampling time interval Ts. It should be observed from Fig. 5 that the middle space vectors are not centered in a sampling time interval Ts. Because of the level-shifted six triangular carrier signals (Fig. 4), the first crossing (termed as first_cross) of the sinusoidal reference signal cannot always be the minimum magnitude of the three sampled sinusoidal reference signals, in a sampling time interval. Similarly, the last crossing (termed as third_cross) of the sinusoidal reference signal cannot always be the maximum magnitude of the three sampled sinusoidal reference signals, in a sampling time interval. Thus the offset voltage, Eoffset1 is not sufficient to center the middle inverter space vectors, in a multilevel PWM system during a sampling time interval Ts (Fig. 5). Hence an additional offset (offset2) has to be added to the sinusoidal reference signals of Fig. 4, so that the middle inverter space vectors can be centered in a sampling time interval, same as a two-level SVPWM system [3]. In this paper, a simple procedure to find out the offset voltage (to be added to the sinusoidal reference signals for PWM generation) is presented, based only on the sampled amplitudes of the sinusoidal reference signals. In the proposed scheme, the sinusoidal reference signal, from the three sampled sinusoidal reference signals, which crosses the triangular carrier signal first (first_cross) and the sinusoidal reference signal which crosses the triangular carrier signal last (third_cross) are found. Once the first_cross signal and third_cross signal are known, the theory of offset calculation of (12), for the 2-level inverter, can easily be adapted for the 7-level SVPWM generation scheme.

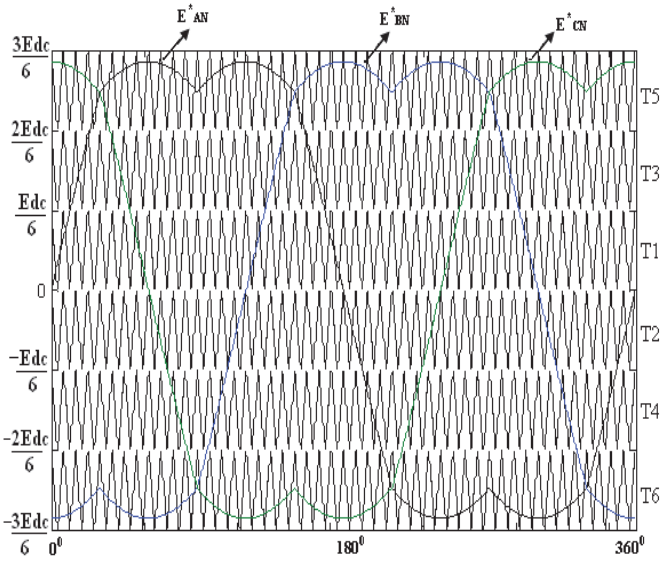

Fig. 4: Modified sinusoidal reference signals and triangular carrier signals for a seven-level PWM scheme

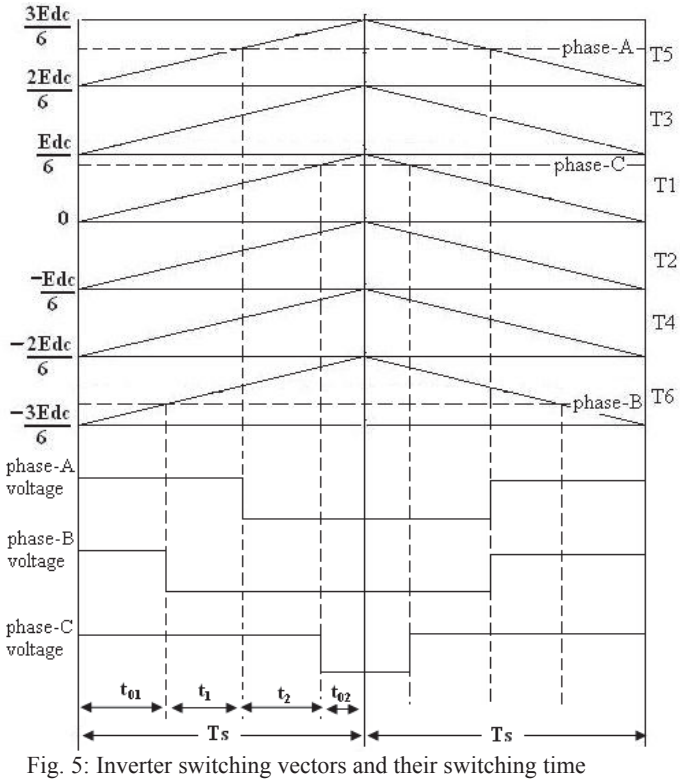

Fig. 5: Inverter switching vectors and their switching time durations during sampling time interval Ts

VI. Determination of the Offset Voltage for a Seven-Level Inverter

Fig. 4 shows modified sinusoidal reference signals and six triangular Carrier signals used for PWM generation for seven-level inverter. The modified sinusoidal reference signals are given by

$$\begin{aligned} E^*_{AN} &= E_{AN} + Eoffset1 \\ E^*_{BN} &= E_{BN} + Eoffset1 \\ E^*_{CN} &= E_{CN} + Eoffset1 \end{aligned} \quad (13)$$

where E_{AN}, E_{BN} and E_{CN} are the sampled amplitudes of sinusoidal reference signals during the current sampling time interval and Eoffset1 is calculated from (12). The time interval, at which the A-phase sinusoidal reference signal, E^*_{AN} crosses the triangular carrier signal, is termed as Ta-cross (Fig. 6). Similarly, the time intervals, when the B-phase and C-phase sinusoidal reference signals, E^*_{BN} and E^*_{CN} cross the triangular carrier signals, are termed as Tb-cross and Tc-cross respectively. Fig. 6 shows a sampling time interval when the A-phase sinusoidal reference signal is in the triangular carrier region T5 while the B-phase sinusoidal reference signal and C-phase sinusoidal reference signal are in carrier region T6 and T1 respectively. As shown in Fig. 6, the time interval, Ta-cross, at which the A-phase sinusoidal reference signal crosses the triangular carrier signal is directly proportional to the phase voltage amplitude, ($E^*_{AN} - 2E_{dc}/6$). The time interval, Tb-cross, at which the B-phase sinusoidal reference signal crosses the triangular carrier signal, is proportional to ($E^*_{BN} + 3E_{dc}/6$) and the time interval, Tc-cross, at which the C-phase sinusoidal reference signal crosses the triangular carrier signal, is proportional to (E^*_{CN}). Therefore

$$\begin{aligned} Ta-cross &= (E^*_{AN} - 2Edc/6)\left(\frac{Ts}{Edc/6}\right) = T^*as - 2Ts \\ Tb-cross &= (E^*_{BN} + 3Edc/6)\left(\frac{Ts}{Edc/6}\right) = T^*bs + 3Ts \\ Tc-cross &= (E^*_{CN})\left(\frac{Ts}{Edc/6}\right) = T^*cs \end{aligned} \quad (14)$$

where T^*as, T^*bs and T^*cs are the time equivalents of the voltage magnitudes. The proportionality between the time equivalents and corresponding voltage magnitudes is defined as follows [8]:

$$\begin{aligned} (Edc/6)/Ts &= E^*_{AN}/T^*as \\ (Edc/6)/Ts &= E^*_{BN}/T^*bs \\ (Edc/6)/Ts &= E^*_{CN}/T^*cs \\ (Edc/6)/Ts &= Eoffset1/Toffset1 \end{aligned} \quad (15)$$

The time interval, at which the sinusoidal reference signals cross the triangular carrier signals for the first time, is termed as Tfirst_cross. Similarly, the time intervals, at which the sinusoidal reference signals cross the triangular carrier signals for the second and third time, are termed as, Tsecond_cross and Tthird_cross respectively, in a sampling time interval Ts.

$$\begin{aligned} Tfirst\_cross &= \min(Ta-cross, Tb-cross, Tc-cross) \\ Tsecond\_cross &= mid(Ta-cross, Tb-cross, Tc-cross) \\ Tthird\_cross &= \max(Ta-cross, Tb-cross, Tc-cross) \end{aligned} \quad (16)$$

The time intervals, Tfirst_cross, Tsecond_cross and Tthird_cross, directly decide the switching times for the different inverter voltage vectors, forming a triangular sector, during one sampling time interval Ts. The time intervals for the start and end space vectors, are t_{01}= Tfirst_cross, t_{02}= (Ts − Tthird_cross), respectively (Fig. 5). The middle space vectors are centered by adding a time offset, Toffset2 to Tfirst_cross, Tsecond_cross and Tthird_cross. The time offset, Toffset2 is determined as follows. The time interval for the middle inverter space vectors, Tmiddle, is given by:

$$Tmiddle = Tthird\_cross - Tfirst\_cross \quad (17)$$

The time interval of the start and end space vector is

$$T_0 = Ts - Tmiddle \quad (18)$$

Thus the time interval of the start space vector is given by

$$T_0/2 = Tfirst\_cross + Toffset2$$

Therefore

$$Toffset2 = T_0/2 - Tfirst\_cross \quad (19)$$

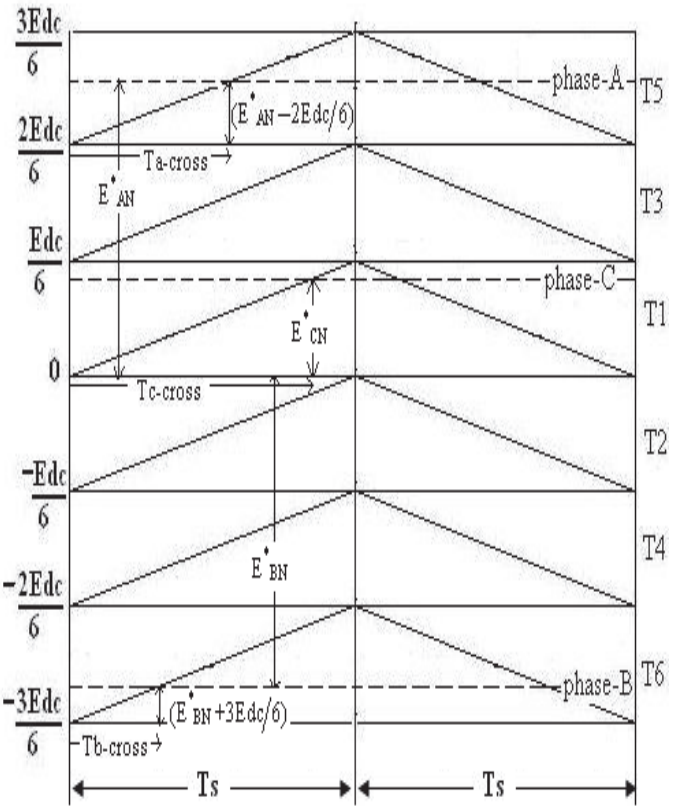

Fig. 6: Determination of the Ta-cross, Tb-cross and Tc-cross during sampling interval Ts

In this way, we can obtain offset voltages to be added for remaining samples during the time period of sinusoidal reference signal. For 7-level inverter maximum modulation index in the linear modulation range is 0.866 (the modulation index, M, is defined as the ratio of magnitude of the equivalent reference voltage space vector, generated by the three sinusoidal reference signals, to the DC link voltage).The proposed scheme can be adapted for modulation indices lesser than 0.866 .The addition of the time offset, Toffset2 to Ta-cross, Tb-cross and Tc-cross gives the inverter leg switching times Tga, Tgb and Tgc for phases A, B and C, respectively.

$$Tga = Ta - cross + Toffset2$$
$$Tgb = Tb - cross + Toffset2 \quad (20)$$
$$Tgc = Tc - cross + Toffset2$$

VII. Simulation Results and Discussion

The proposed SVPWM scheme is simulated using MATLAB environment with open loop E/f control for different modulation indices. The respective DC link voltages are $(2/6)E_{dc}$, $(2/6)E_{dc}$, $(1/6)E_{dc}$ and $(1/6)E_{dc}$ for the INV-1, INV-2, INV-3 and INV-4, where E_{dc} is the DC link voltage of an equivalent conventional single two-level inverter drive. The speed reference is translated to the frequency and voltage commands maintaining E/f. The modified three reference sinusoidal signals which are added by the total offset voltage to make SPWM scheme equivalent to the SVPWM scheme, are simultaneously compared with the triangular carrier set. A DC link voltage (E_{dc}) of 600 volts is assumed for simulation studies. Fig. 7a shows the motor phase voltage (E_{A2A4}) in the lowest speed range which corresponds to layer-1 operation (two-level mode) when modulation index is 0.13. Fig. 7b shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM and fig. 7c shows the A-phase sinusoidal reference signal after offset voltage is added. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig. 7d and Fig. 7e respectively. Fig. 8a shows the motor phase voltage (E_{A2A4}) in the next speed range which corresponds to layer-2 operation (three-level mode) when modulation index is 0.25. Fig. 8b shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM and fig. 8c shows the A-phase sinusoidal reference signal after offset voltage is added. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig. 8d and Fig. 8e respectively. Fig. 9a shows the motor phase voltage (E_{A2A4}) in the next speed range which corresponds to layer-3 operation (four-level mode) when modulation index is 0.425. Fig. 9b shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM and fig. 9c shows the A-phase sinusoidal reference signal after offset voltage is added. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig. 9d and Fig. 9e respectively. Fig. 10a shows the motor phase voltage (E_{A2A4}) in the next speed range which corresponds to layer-4 operation (five-level mode) when modulation index is 0.55. Fig. 10b shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM and fig. 10c shows the A-phase sinusoidal reference signal after offset voltage is added. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig. 10d and Fig. 10e respectively. Fig. 11a shows the motor phase voltage (E_{A2A4}) in the next speed range which corresponds to layer-5 operation (six-level mode) when modulation index is 0.7. Fig. 11b shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM and fig. 11c shows the A-phase sinusoidal reference signal after offset voltage is added. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig. 11d and Fig. 11e respectively. Fig. 12a shows the motor phase voltage (E_{A2A4}) in the next speed range which corresponds to layer-6 operation (seven-level mode) when modulation index is 0.85. Fig. 12b shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM and fig. 12c shows the A-phase sinusoidal reference signal after offset voltage is added. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig. 12d and Fig. 12e respectively. The ratio of triangular carrier signal frequency to reference sinusoidal signal frequency is 48 for all ranges of operation. It can be observed that the motor phase voltage and motor phase current during 7-level operation are very smooth and close to the sinusoid with lower harmonics.

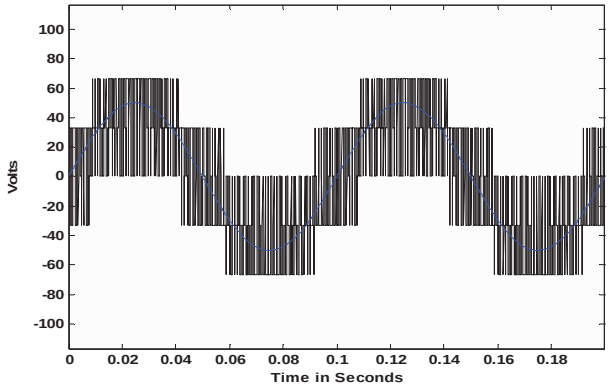

Fig. 7a: Motor phase voltage when M=0.13 (layer-1, 2-level operation)

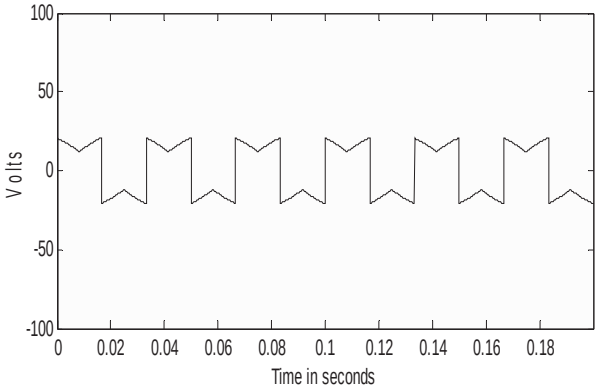

Fig. 7b: The offset voltage to be added to sinusoidal reference signals when M=0.13 (layer-1, 2-level operation)

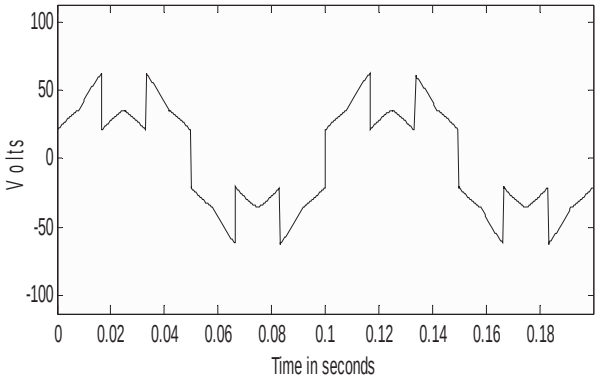

Fig. 7c: The A-phase sinusoidal reference signal after offset voltage is added when M=0.13 (layer-1, 2-level operation)

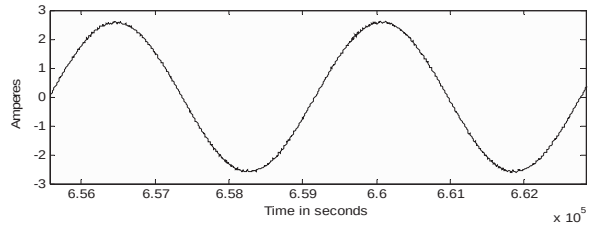

Fig. 7d: Motor phase current when M=0.13 (layer-1, 2-level operation)

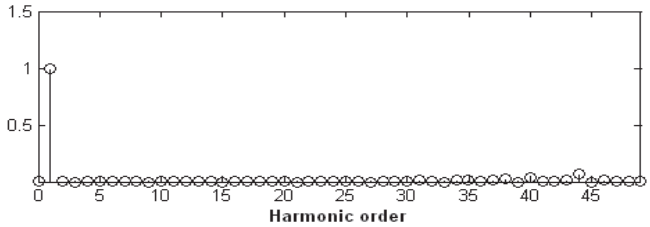

Fig. 7e: Normalized harmonic spectrum of the motor phase voltage when M=0.13 (layer-1, 2-level operation)

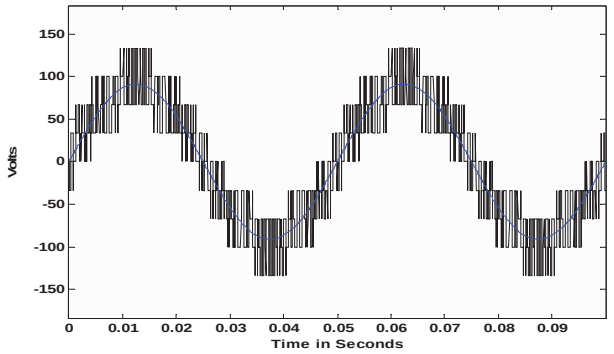

Fig. 8a: Motor phase voltage when M=0.25 (layer-2, 3-level operation)

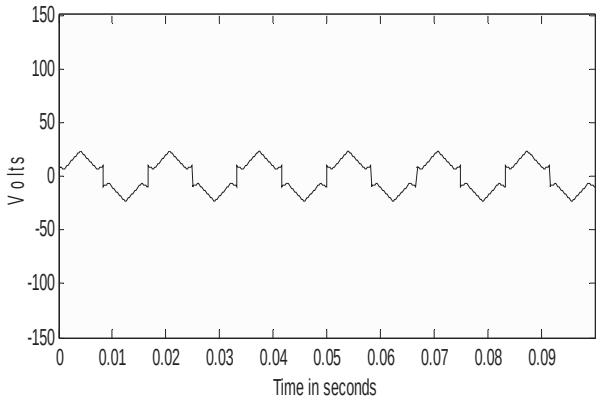

Fig. 8b: The offset voltage to be added to sinusoidal reference signals when M=0.25 (layer-2, 3-level operation)

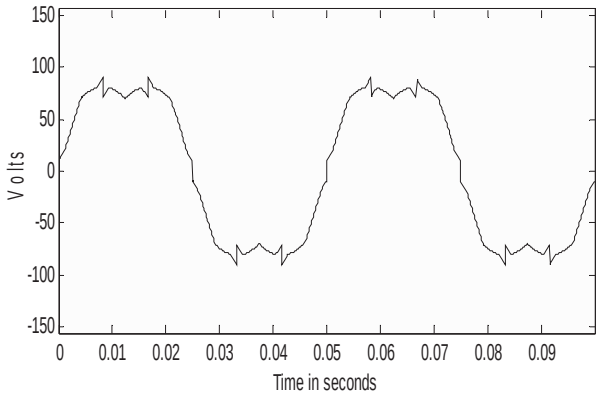

Fig. 8c: The A-phase sinusoidal reference signal after offset voltage is added when M=0.25 (layer-2, 3-level operation)

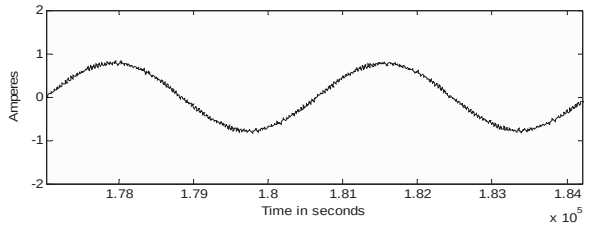

Fig. 8d: Motor phase current when M=0.25 (layer-2, 3-level operation)

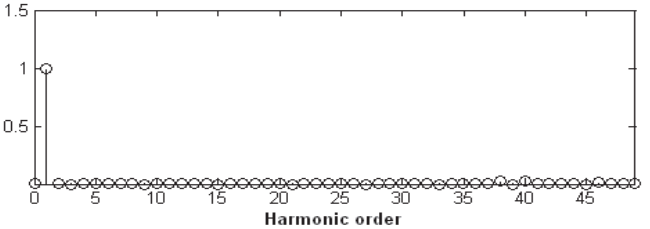

Fig. 8e: Normalized harmonic spectrum of the motor phase voltage when M=0.25 (layer-2, 3-level operation)

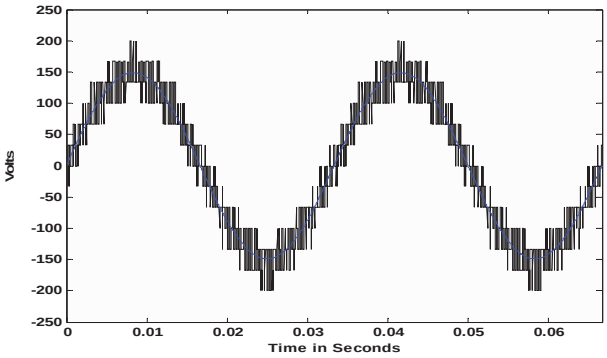

Fig. 9a: Motor phase voltage when M=0.425 (layer-3, 4-level operation)

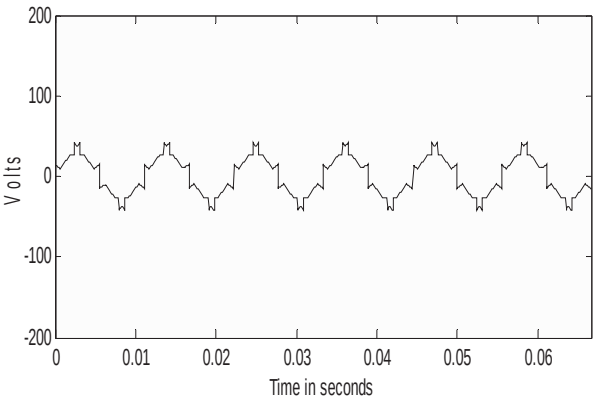

Fig. 9b: The offset voltage to be added to sinusoidal reference signals when M=0.425 (layer-3, 4-level operation)

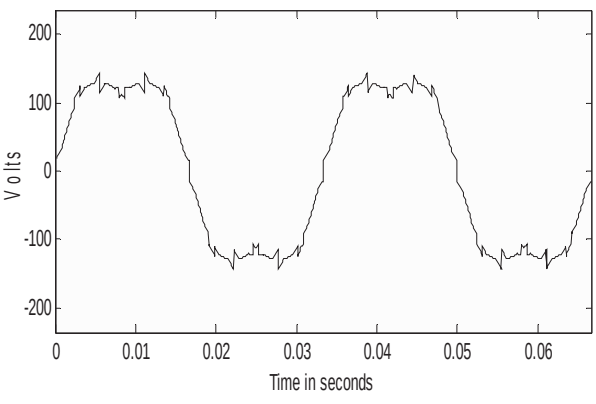

Fig. 9c: The A-phase sinusoidal reference signal after offset voltage is added when M=0.425 (layer-3, 4-level operation)

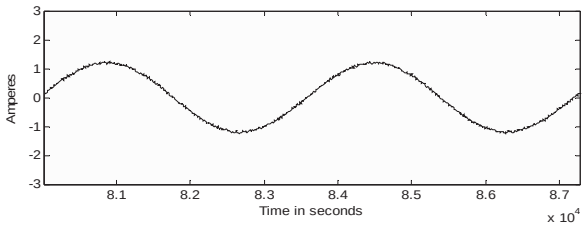

Fig. 9d: Motor phase current when M=0.425 (layer-3, 4-level operation)

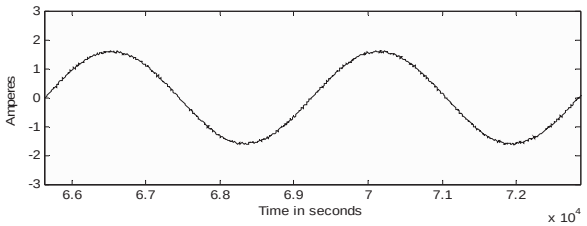

Fig. 10d: Motor phase current when M=0.55 (layer-4, 5-level operation)

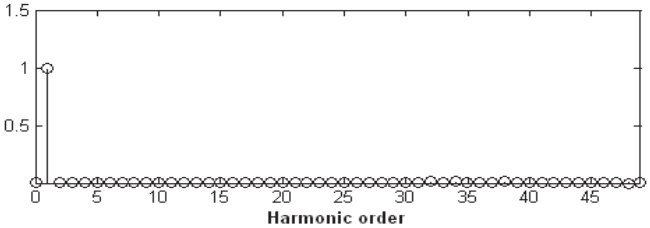

Fig. 9e: Normalized harmonic spectrum of the motor phase voltage when M=0.425 (layer-3, 4-level operation)

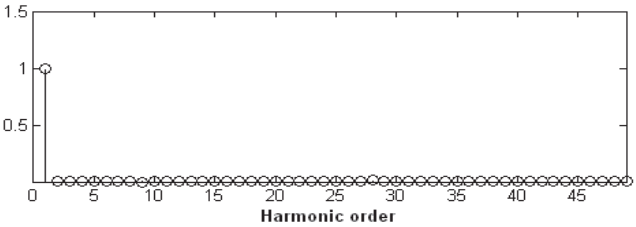

Fig. 10e: Normalized harmonic spectrum of the motor phase voltage when M=0.55 (layer-4, 5-level operation)

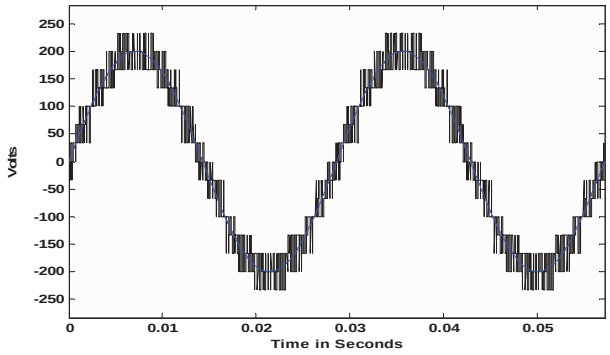

Fig. 10a: Motor phase voltage when M=0.55 (layer-4, 5-level operation)

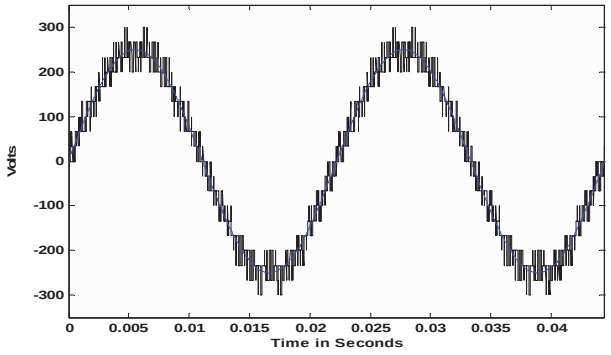

Fig. 11a: Motor phase voltage when M=0.7 (layer-5, 6-level operation)

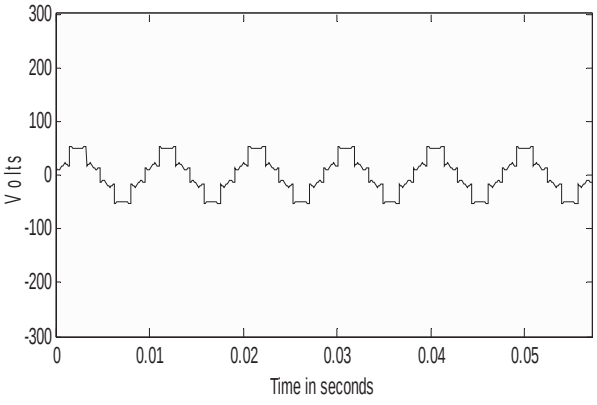

Fig. 10b: The offset voltage to be added to sinusoidal reference signals when M=0.55 (layer-4, 5-level operation)

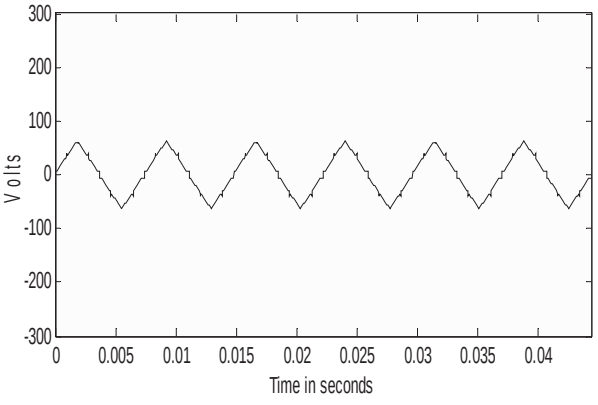

Fig. 11b: The offset voltage to be added to sinusoidal reference signals when M=0.7 (layer-5, 6-level operation)

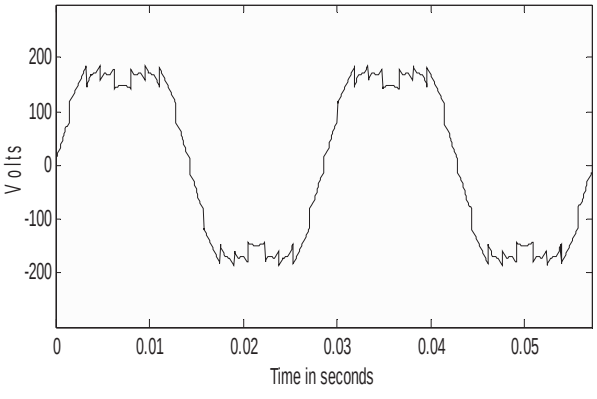

Fig. 10c: The A-phase sinusoidal reference signal after offset voltage is added when M=0.55 (layer-4, 5-level operation)

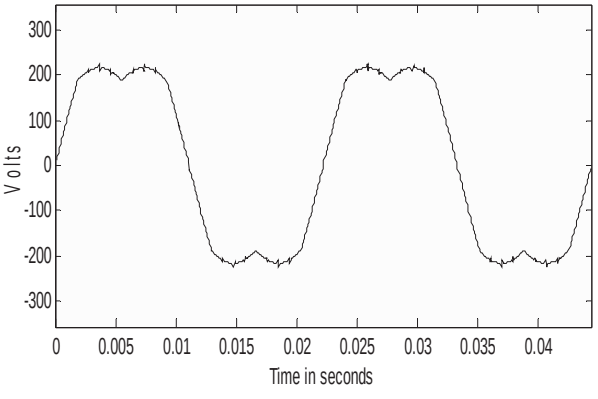

Fig. 11c: The A-phase sinusoidal reference signal after offset voltage is added when M=0.7 (layer-5, 6-level operation)

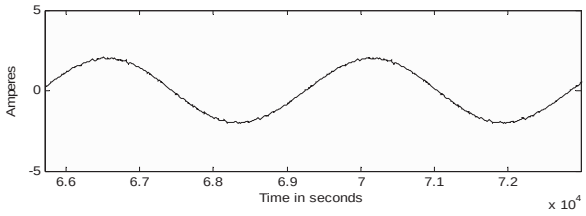

Fig. 11d: Motor phase current when M=0.7 (layer-5, 6-level operation)

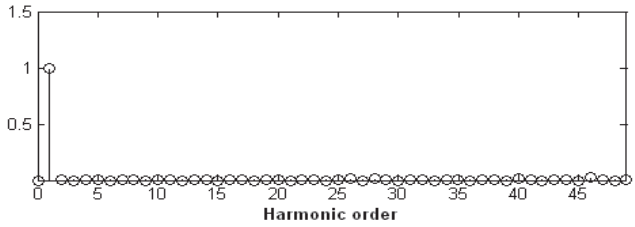

Fig. 11e: Normalized harmonic spectrum of the motor phase voltage when M=0.7 (layer-5, 6-level operation)

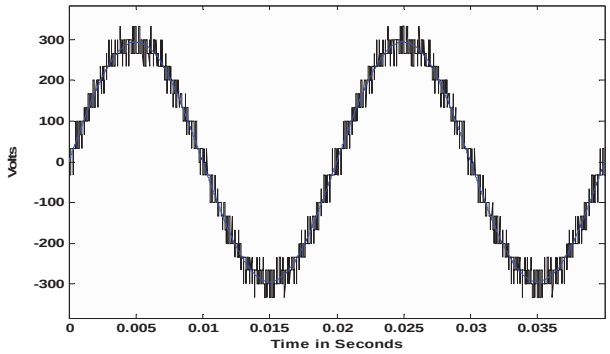

Fig. 12a: Motor phase voltage when M=0.85 (layer-6, 7-level operation)

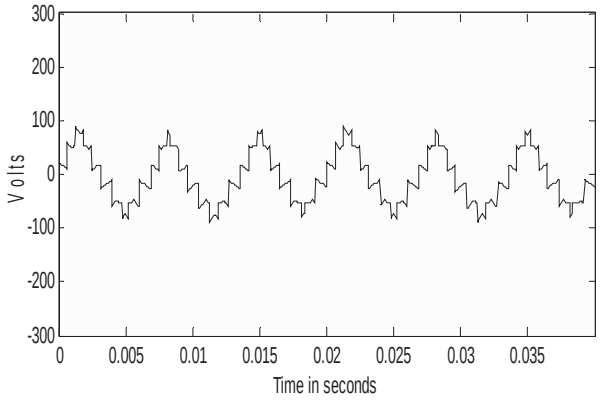

Fig. 12b: The offset voltage to be added to sinusoidal reference signals when M=0.85 (layer-6, 7-level operation)

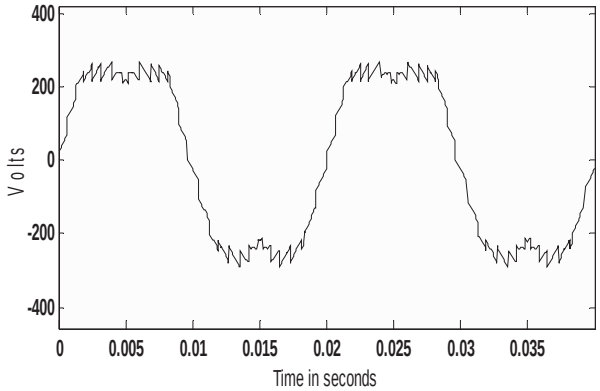

Fig. 12c: The A-phase sinusoidal reference signal after offset voltage is added when M=0.85 (layer-6, 7-level operation)

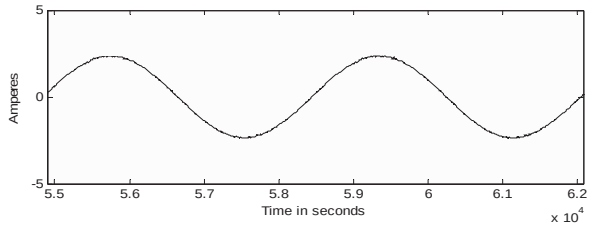

Fig. 12d: Motor phase current when M=0.85 (layer-6, 7-level operation)

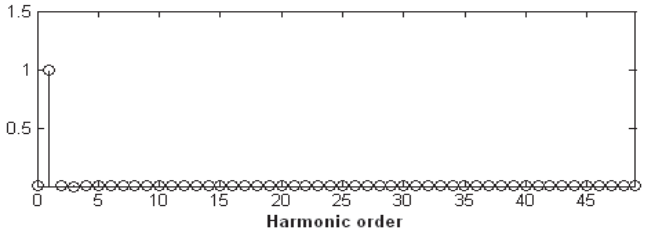

Fig. 12e: Normalized harmonic spectrum of the motor phase voltage when M=0.85 (layer-6, 7-level operation)

VIII. Conclusion

A modulation scheme of SVPWM for seven-level inverter system for dual-fed induction motor drive, where the induction motor is fed by two symmetrical three-level inverters from both ends is presented. The symmetrical three-level inverter used is composed of two conventional two-level inverters with equal DC link voltage in cascade. The centering of the middle inverter space vectors of the SVPWM is accomplished by the addition of an offset voltage signal to the sinusoidal reference signals, derived from the sampled amplitudes of the sinusoidal reference signals. The SVPWM technique, presented in this paper does not require any sector identification, as is required in conventional SVPWM schemes. The proposed scheme eliminates the use of look-up table approach to switch the appropriate space vector combination as in conventional SVPWM schemes. This reduces the computation time required to determine the switching times for inverter legs, making the algorithm suitable for real-time implementation.

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space vector PWM inverters", *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1144–1151, 1998.

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