A Six-level SPWM Inverter for an Open-end Winding Induction Motor

K.Chandra Sekhar[1] and G.Tulasi Ram Das[2]

Abstract –A six-level inverter system for an open-end winding induction motor drive is presented in this paper. Multilevel inversion is achieved by feeding an open-end winding induction motor with a 3-level inverter from one end and a 2-level inverter from the other end of the motor. The 3-level inverter used in the proposed drive, is realized by cascading two 2-level inverters. The combined inverter system with open-end winding induction motor produces voltage space phasor levels identical to a conventional 6-level inverter. In the multilevel carrier based sinusoidal pulse width modulation (spwm), used for the proposed drive, a progressive discrete DC bias depending upon the speed range is given to the reference wave so that the drive can operate in the k-level modes (k = 2, 3, … 6) depending on the speed range. The inverter with the higher DC-link voltage is switching less frequently, compared to the inverter with the lower DC-link voltage.

Keywords - Multilevel inverter, open-end winding induction motor, multilevel carrier based sinusoidal pulse width modulation

I. INTRODUCTION

Multilevel inverters have found increased relevance in the area of high power high voltage applications in the recent years since they were proposed in 1981[1][2][3]. The Multilevel inverters investigated for large induction motor drives fall under four general categories: the neutral-point clamped inverters, flying capacitor multilevel inverters, cascaded H-bridge inverters and open-end winding induction motor fed by dual inverters.

The neutral point clamped inverters experience neutral point fluctuations, as the DC-link capacitors have to carry the load current [4][5]. Flying capacitor topology is another scheme proposed for the multilevel inverters [6]. This structure does not require the neutral clamping diodes but needs as many capacitors as floating DC voltage sources. Higher number of levels is obtainable with series connected hybrid topology are more complex [7][8].

Dual inverter fed open-end winding induction motor drives also results in multilevel inverter structure [9][10]. A Dual inverter scheme with asymmetrical DC link voltages for the open-end winding induction motor is capable of producing a 4-level PWM waveform with reduced switching ripple for the motor phase voltage [11].

Digital ref: A070101080
[1]Dept. of Electrical & Electronics Engineering, R.V.R & J.C College of Engineering, Chowdavaram, Guntur, -520 019(India).
[2]Dept. of Electrical Engineering, J.N.T.U College of Engineering, Kukatpally, Hyderabad–500 072 (India).
email: cskoritala@hotmail.com , das_tulasiram@yahoo.co.in
The paper first received on 18 Dec 2005 and in revised form 20 April 2007.

A multilevel system that is capable of realizing a PWM waveform ranging from 2-level to 5-level is described in [12]. In the topology described in [12], an asymmetrical 3-level inverter and a 2-level inverter feed an induction motor with open-end windings. The waveforms in [12] were obtained by switching the appropriate space vector combination using the look-up table. It is a formidable and cumbersome proposition to switch appropriate space vector combinations using look-up table approach. The three-level inverter in [13] is constituted by the cascade connection of two 2-level inverters with equal DC-link voltage.

In the present work, an inverter system to produce a multilevel PWM waveform ranging from 2-level to 6-level for the motor phase voltage for an open-end winding induction motor drive is proposed. In the proposed scheme, an open-end winding induction motor is fed with a symmetrical three-level inverter from one end and a two-level inverter from the other end. In the present work, symmetrical three-level inversion is obtained by connecting two 2-level inverters with equal DC-link voltage in cascade. The inverter scheme proposed in this paper produces voltage space phasor levels equivalent to a conventional 6-level inverter. This six-level inverter does not experience neutral point fluctuations and uses a lesser number of DC sources compared to the series H-bridge topology. A multilevel carrier based PWM is implemented for the drive where a progressive discrete DC bias is given to the reference wave depending upon the speed range. This results in a reduction of the switching ripple in the motor phase voltage waveform. This multilevel carrier based PWM eliminates the use of look-up approach to switch the appropriate space vector combination as in [12].

II. PROPOSED POWER CIRCUIT CONGIHURATION

The proposed power circuit topology to realize a multilevel phase voltage is shown in Fig.1. In this circuit configuration, an open-end winding induction motor is fed from a 3-level inverter (two 2-level inverters are connected in cascade-inverter-1 & inverter-2 of Fig.1) from one end and a two-level inverter (inverter-3 of Fig.1) from the other end of the motor. The DC-link voltages of inverter-1, inverter-2 and inverter-3 are $(2/6)V_{dc}$, $(2/6)V_{dc}$ and $(1/6)V_{dc}$ respectively, where V_{dc} is the DC-link voltage of an equivalent conventional single 2-level inverter drive. For inverter-2, let V_{A2o}, V_{B2o} and V_{C2o} represent the pole voltages of A, B and C phases respectively, referred to the point 'O' (Fig.1). The pole voltage, of any phase for inverter-2 for example V_{A2o} (Fig.1) attains a voltage of $(2/6)\ V_{dc}$, if the following conditions are satisfied:

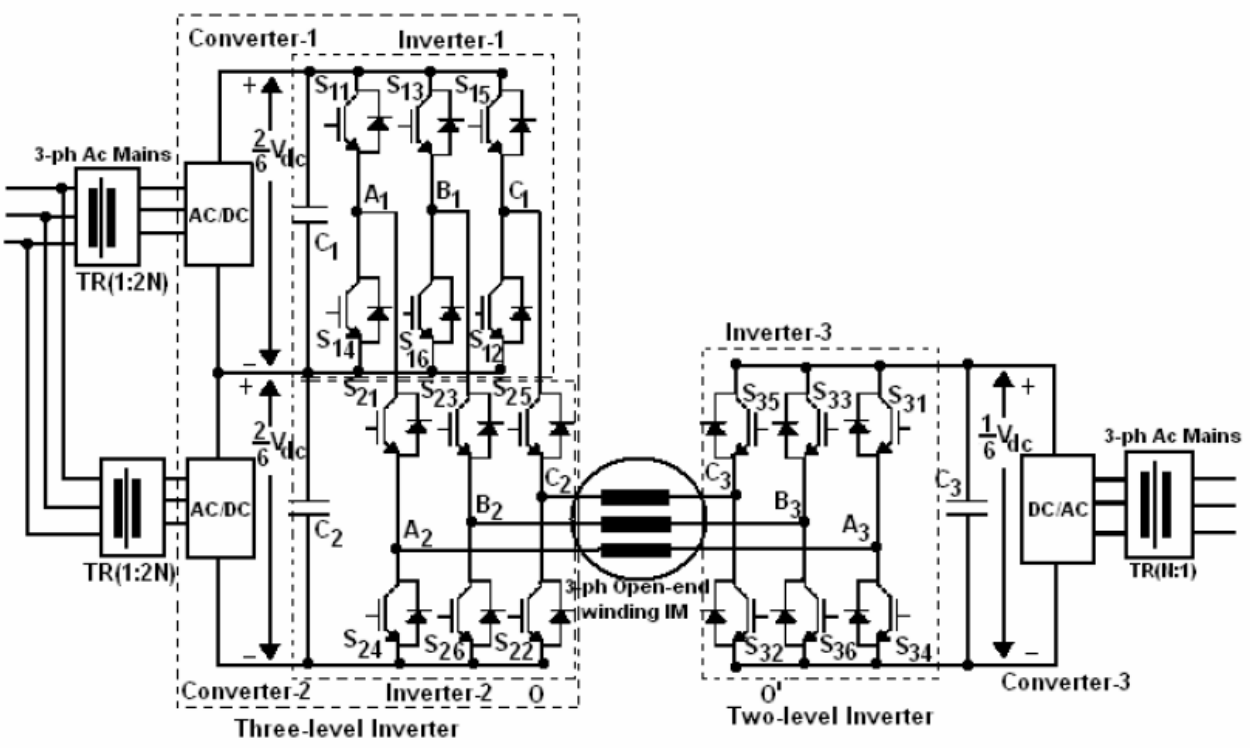

Fig. 1: Schematic circuit diagram of the proposed inverter drive scheme

- The top switch of that leg in inverter-2, in this case S_{21}, is turned on (Fig.1).
- The bottom switch of the corresponding leg in Inverter-1, in this case S_{14}, is turned on (Fig.1).

Similarly the pole voltage of any phase in inverter-2, for example V_{A2o} attains a voltage of $(4/6)V_{dc}$, if the following conditions are satisfied:

- The top switch of that leg in inverter-2, in this case S_{21}, is turned on (Fig.1).
- The top switch of the corresponding leg in inverter-1, in this case S_{11}, is turned on (Fig.1).

Thus, the DC-input points of individual phases of inverter-2 may be connected to a DC-link voltage of either (4/6) V_{dc} or (2/6) V_{dc} by turning on the top switch or the bottom switch of the corresponding phase leg in inverter-1. Additionally, the pole voltage of a given phase in inverter-2 attains a voltage of zero, if the bottom switch of the corresponding leg in inverter-2 is turned on. Thus, the pole voltage of a given phase for inverter-2 is capable of assuming one of the three possible values 0, $(2/6)V_{dc}$ and $(4/6)V_{dc}$, which is the characteristic of a three level inverter. This configuration of 3-level inverter eliminates the neutral point fluctuations associated with the conventional neutral clamped 3-level inverter [1] as the capacitors C_1 and C_2 do not carry the load current but only the ripple currents. Also, the fast recovery neutral clamping diodes are eliminated in this topology of 3-level inverter. This 3-level inverter can be synthesized by reconnecting two existing 2-level inverters as a retrofit.
The pole voltages of 2-level inverter 'inverter-3' ($V_{A3O,}$, $V_{B3O,}$, $V_{C3O,}$) assume one of the two values 0 or $(1/6)V_{dc}$ depending on whether the top switch or the bottom switch of a given phase leg is turned on. When these inverters drive the induction motor from both sides each phase of the induction motor can attain six different levels. To find the equivalent levels when Three level inverter and two level inverter are switched independently, the points O and O' are assumed to be connected. The different levels, generated for phase-A when Three level inverter and two level inverters are switched with different pole voltage levels are shown in Table-1.

It can be verified that all the other phases also can realize these six levels. It can be seen that the first two levels – (1/6) V_{dc} and 0 (L1, L2) are obtained when Three level inverter is clamped to zero while two level inverter is switched to (1/6) V_{dc} and 0. For the third and fourth levels (L3, L4) Three level inverter is clamped to its second level $(2/6)V_{dc}$, while two level inverter is switched to (1/6) V_{dc} and 0. For the fifth and sixth levels (L5, L6) Three level inverter can be clamped to third level $(4/6)V_{dc}$ while two level inverter is switched to (1/6) V_{dc} and 0. Hence the Three level inverter is switched less frequently as the inverter operates in all these levels.

It may be noted that when the bottom switch in a leg of the bottom inverters (inverter-2 or inverter-3) is ON, taking the machine winding end to O or O', the top switch of top inverter in the same leg could be ON or OFF. But if the top switch of the top inverter (inverter-1) is also made ON, the top switch of the bottom inverter would have to block twice DC link voltage [i.e.$(4/6)V_{dc}$]. So whenever the bottom switch in any leg of the bottom inverter is ON, the top switch in the same leg of the top inverter is kept OFF. The condition to be forced on the top switches of the inverters to realize these 6-levels in the A-phase is shown in the Table-2. The state of the bottom switch is complementary to the condition of the top switch in the same leg. The bottom switches of the bottom inverter of

Three level inverter (inverter-2) have to be rated for $(4/6)V_{dc}$, as they will have to block $(4/6)V_{dc}$ when the top switches of inverter-1 and inverter-2 are switched on. The bottom switches of the bottom of two level inverter (inverter-3), have to be rated for $(1/6)V_{dc}$, as they will have to block $(1/6)V_{dc}$.

This six-level topology does not need the clamping diodes as in the case of neutral-point clamped inverters. The DC-link capacitors do not carry the load current and hence the neutral-point fluctuations are absent. When compared with the series-connected H-bridge, it uses the less number of switching devices and DC-sources. The five-level inverter configuration has further been improvised to yield a six-level operation would results in a better waveform with lower THD.

Table 1: The levels realized in the A-phase winding when Three level inverter and Two level inverter are switched independently

Pole-voltage of Three level inverter (V_{A20})	Pole-voltage Of Two level Inverter (V_{A30})	Motor phase voltage V_{A2A3}= $V_{A20} - V_{A30}$)	Level
0	$(1/6)V_{dc}$	$-(1/6)V_{dc}$	L1
0	0	0	L2
$(2/6)V_{dc}$	$(1/6)V_{dc}$	$(1/6)V_{dc}$	L3
$(2/6)V_{dc}$	0	$(2/6)V_{dc}$	L4
$(4/6)V_{dc}$	$(1/6)V_{dc}$	$(3/6)V_{dc}$	L5
$(4/6)V_{dc}$	0	$(4/6)V_{dc}$	L6

Table 2: The Status of the switches in the inverters for each of six levels

Level in A-phase		Status of the top switches of the 2-level inverters (The bottom switches condition is complementary)		
	Voltage	Inverter1 S_{11}	Inverter1 S_{21}	Inverter1 S_{31}
L1	$-(1/6)V_{dc}$	OFF	OFF	ON
L2	0	OFF	OFF	OFF
L3	$(1/6)V_{dc}$	OFF	ON	ON
L4	$(2/6)V_{dc}$	OFF	ON	OFF
L5	$(3/6)V_{dc}$	ON	ON	ON
L6	$(4/6)V_{dc}$	ON	ON	OFF

III. VOLTAGE SPACE PHASORS OF PROPOSED SCHEME

The combined effect of three voltages in the three 120 degree separated phase winding of the induction motor at any instant, could be represented by an equivalent vector in space. This space vector V_s for the dual inverter scheme is given by

$$V_s = V_{A2A3} + V_{B2B3}.e^{j(2\pi/3)} + V_{C2C3}.e^{j(4\pi/3)}. \quad (1)$$

Substituting expressions for the phase voltages in the above equation gives

$$V_s = (V_{A2O} - V_{A3O}) + (V_{B2O} - V_{B3O}).e^{j(2\pi/3)} + (V_{C2O} - V_{C3O}).e^{j(4\pi/3)} \quad (2)$$

This equivalent vector can be determined by resolving the phase voltages along two mutually perpendicular axes, α-β axes of which α is along the A-phase(Fig.2). The space vector is then given by

$$V_s = V_s(\alpha) + jV_s(\beta) \quad (3)$$

Where $V_s(\alpha)$ is the sum of all components of V_{A2A3}, V_{B2B3} and V_{C2C3} along the α axis and $V_s(\beta)$ is the sum of the components V_{A2A3}, V_{B2B3} and V_{C2C3} along the β axis. The voltage components $V_s(\alpha)$ and $V_s(\beta)$ can be thus obtained by the following transformation

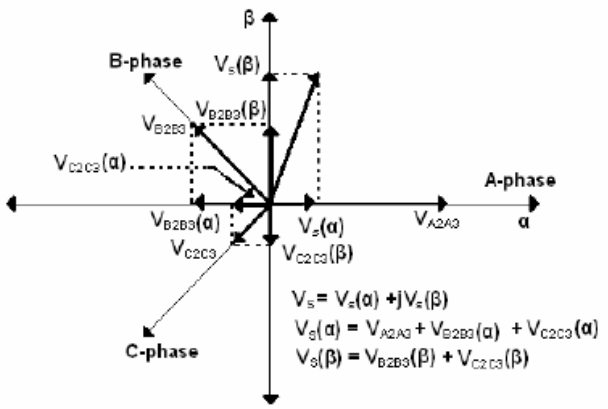

Fig. 2: Determination of equivalent space vector from phase voltages

$$V_S(\alpha) = V_{A2A3} + V_{B2B3}(\alpha) + V_{C2C3}(\alpha) \quad (4)$$

$$V_S(\beta) = V_{B2B3}(\beta) + V_{C2C3}(\beta) \quad (5)$$

$$\begin{bmatrix} V_s(\alpha) \\ V_s(\beta) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix} \quad (6)$$

Substituting expressions for the phase voltages in the above equation gives

$$\begin{bmatrix} V_s(\alpha) \\ V_S(\beta) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A20} - V_{A30'} \\ V_{B20} - V_{B30'} \\ V_{C20} - V_{C30'} \end{bmatrix} \quad (7)$$

The inverters can take different levels of pole voltages independently in the three phases depending upon the condition of the inverter switches and for each of the different combination of their pole voltages, V_{A2o}, V_{B2o} and V_{C2o} for the Three level inverter and V_{A3o},, V_{B3o}, and V_{C3o}, for the two level inverter. The equivalent voltage space phasor V_s, can be determined using equations (3) and (7). All the space phasors can be determined for all the possible combinations of the pole voltages of the two inverters. They will occupy different locations as shown in Fig.3, where the location marked '1' is the location of the zero amplitude space vector. When compared with five-level inverter the space phasor locations are enhanced to 91 from 61and the sectors are enhanced to 150 from 91 in the space vector point of view. The maximum amplitude of the space phasor generated can be verified to be V_{dc}.

A. Effect of Common-Mode Voltage in Space Phasor Locations

In the above analysis for deriving the different levels and the space phasor locations, the points O and O' were assumed to be connected. When these points are not connected (as in the proposed drive Fig.1), the actual phase voltages are

$$V_{A2A3} = V_{A2O} - V_{A3O'} - V_{O'O} \quad (8)$$

$$V_{B2B3} = V_{B2O} - V_{B3O'} - V_{O'O} \quad (9)$$

$$V_{C2C3} = V_{C2O} - V_{C3O'} - V_{O'O} \quad (10)$$

$V_{O'O}$ corresponds to the common-mode voltage present in this balanced three-phase system and is given by

$$V_{O'O} = \tfrac{1}{3}(V_{A2O} + V_{B2O} + V_{C2O}) - \tfrac{1}{3}(V_{A3O'} + V_{B3O'} + V_{C3O}) \quad (11)$$

Substituting these expressions for the phase voltages in (1)

$$V_S = (V_{A2O} - V_{A3O'} - V_{O'O}) + (V_{B2O} - V_{B3O'} - V_{O'O}).e^{j(2\pi/3)} + (V_{C2O} - V_{C3O'} - V_{O'O}).e^{j(4\pi/3)}$$

$$= (V_{A2O} - V_{A3O}) + (V_{B2O} - V_{B3O}).e^{j(2\pi/3)} + (V_{C2O} - V_{C3O}).e^{j(4\pi/3)} - (V_{O'O} + V_{O'O}.e^{j(2\pi/3)} + V_{O'O}.e^{j(4\pi/3)})$$

In this equation

$$(V_{O'O} + V_{O'O}.e^{j(2\pi/3)} + V_{O'O}.e^{j(4\pi/3)}) = V_{O'O} - \tfrac{1}{2}V_{O'O} - \tfrac{1}{2}V_{O'O} = 0$$

and the equation then reduces to

$$V_s = (V_{A2O} - V_{A3O}) + (V_{B2O} - V_{B3O}).e^{j(2\pi/3)} + (V_{C2O} - V_{C3O}).e^{j(4\pi/3)}$$

This equation is the same as that derived earlier (2), assuming that points O and O' were connected. Hence the above analysis shows that the common-mode present between points O and O' does not change the space phasor locations. This common-mode voltage will result only in the multiplicity of space phasors in different locations, and the system with isolated O and O' points generates the same voltage-space phasors.

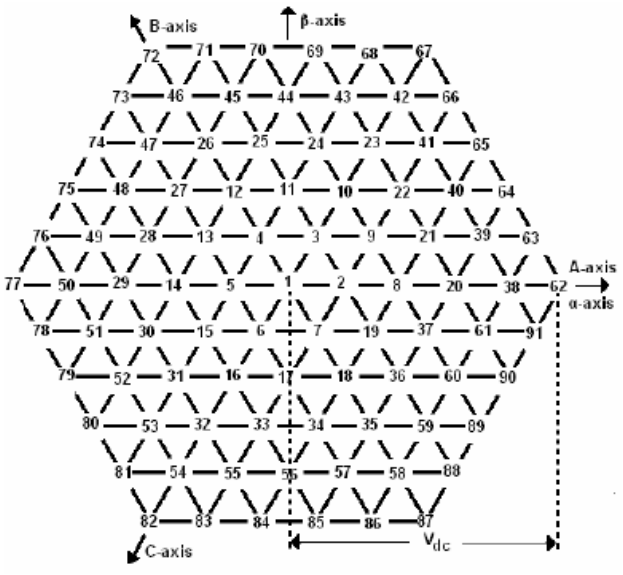

Fig. 3: The voltage space phasor locations for the proposed drive 91 locations forming 150 triangular sections equivalent to a 6-level Inverter.

IV. MODULATION SCHEME FOR THE PROPOSED INVERTER

Multilevel carrier based SPWM is used for the proposed inverter scheme. The multilevel carrier based PWM for an N-level inverter uses a set of N-1 adjacent level shifted triangular carrier waves with the amplitude and frequency [14]. If reference wave has peak amplitude V_m^* and frequency f_m, the modulation index is defined with reference to a triangular wave of peak-to –peak amplitude of V_C (N-1) as

$$M_a = 2V_m^* / V_C(N\text{-}1). \quad (12)$$

For the 6-level inverter drive structure, 5 triangular waves C1 to C5, with peak-to-peak amplitude of V_C are used, as shown in Fig.4a. The peak-to-peak amplitude of each carrier is $V_C = (1/6)V_{max}$, where V_{max} is the maximum value possible for the modulating signal. These five carriers divide the entire range of modulating signal to six regions R1 to R6, R1 being the region below the lowest carrier C1 and R6 the region above the highest carrier C5. The regions between these two carriers are referred as R2 to R5. When the modulating signal is in a particular region a corresponding voltage level is applied across the motor phase winding as assigned below:

$$R1 \Rightarrow -(1/6)V_{dc};\ R2 \Rightarrow 0;\ R3 \Rightarrow (1/6)V_{dc};$$
$$R4 \Rightarrow (2/6)V_{dc};\ R5 \Rightarrow (3/6)V_{dc};\ R6 \Rightarrow (4/6)V_{dc}; \quad (13)$$

Three 120 degree phase shifted sinusoids with 20% third harmonics content are used as the reference waves for the proposed carrier based SPWM. The addition of third harmonic content increases the maximum fundamental voltage amplitude that can be generated using the SPWM scheme [15].

These reference waves are continuously compared with

the carrier set to determine the region (R1, R2…R6) in which the instantaneous value of the reference wave exists. This comparison is performed simultaneously for all the three phases. Control signals for the two inverters then can be generated such that the appropriate devices are switched to realize the particular level in a particular phase depending upon the region. It may be noted that the proposed inverter can realize the even numbered levels also, and can start with the 2-level operation and progressively move to the 3-level, 4-level, 5-level and to the 6-level operation as the modulation index increases.

For low modulation index such that $V_m^* \leq V_C/2$ where V_m^* is the peak value of the modulating signal, in conventional SPWM the reference waves are placed at the center of the carrier set (Fig.4a). This will result in a 4-level operation as the modulating signal at different instants could be in one of the four regions R2, R3, R4 or R5. To realize the four levels associated with these regions (13), both inverters

Three level inverter and two level inverter would be switching (Table-2). Now if the reference wave is placed at the middle of the lowest carrier C1 as Fig.4b, the modulating signal exists only in two regions R1 or R2 and it will result in only two levels L1 (-1/6 V_{dc}) and L2 (0). In this case the switching losses are only due to two level inverter.

When the modulating index increases such that $V_C/2 \leq V_m^* \leq V_C$, an additional DC bias of $V_C/2$ is given to the reference wave such that it is at the middle of the two lower carriers C1 and C2 and results in 3-level operation (Fig.4c). A similar progressive DC shift in steps $V_C/2$ of is gives such that the inverter progressively moves through the 3-level, 4-level, 5-level and to 6-level operation (Fig.4d, Fig.4e &Fig.4f).

When the V/f control is used, these 5 ranges of voltage amplitudes correspond to 5 ranges in frequency. Therefore the range (denoted by n = 1, 2, …5) in which the frequency command falls can be used to determine the DC shift to be given to the reference waves and the reference waveforms can be represented by,

$$V_a^* = V_m \sin\omega t + 0.2\, V_m \sin 3\omega t + n\, V_c/2, \quad (14)$$

$$V_b^* = V_m \sin(\omega t - 2\pi/3) + 0.2\, V_m \sin 3\omega t + n\, V_c/2, \quad (15)$$

$$V_c^* = V_m \sin(\omega t - 4\pi/3) + 0.2\, V_m \sin 3\omega t + n\, V_c/2. \quad (16)$$

When this SPWM scheme is employed, Three level inverter is clamped to zero level and two level inverter is switched in two level mode to create the first two levels (L1, L2), then Three level inverter is clamped to second level (2/6)V_{dc}, and two level inverter is switched in 2-level mode to create the next two levels (L3, L4) and finally Three level inverter is clamped to its third level (4/6)V_{dc}, and two level inverter is switched in 2-level mode to create the last two levels (L5, L6). This results in the inverters, which has the higher DC bus voltage switching less frequently compared to two inverters.

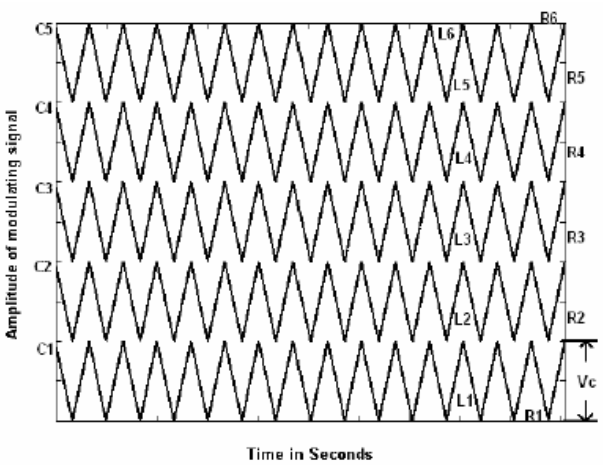

Fig. 4 (a): The carrier and the different regions in the multi-level carrier PWM

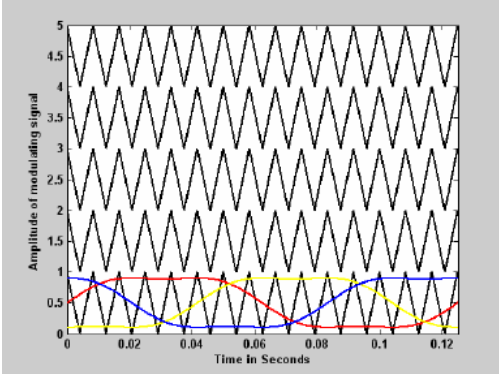

Fig. 4 (b): The reference wave set for 2-level operation in the proposed SPWM

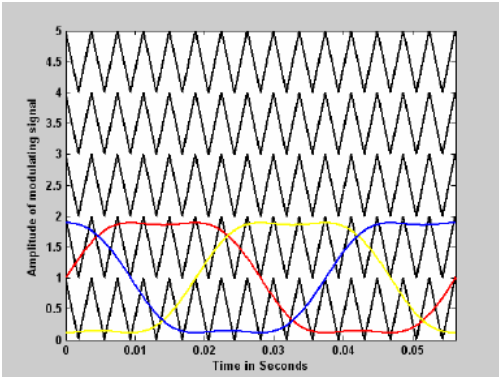

Fig. 4 (c): The reference wave set for 3-level operation in the proposed SPWM

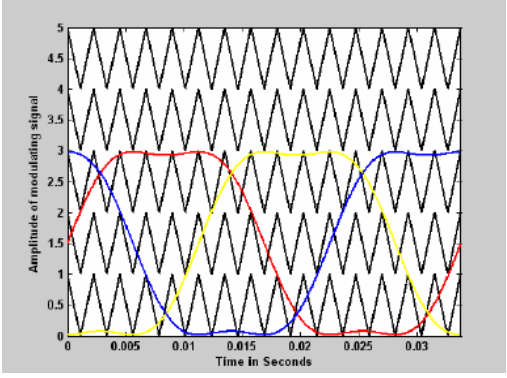

Fig. 4 (d): The reference wave set for 4-level operation in the proposed SPWM

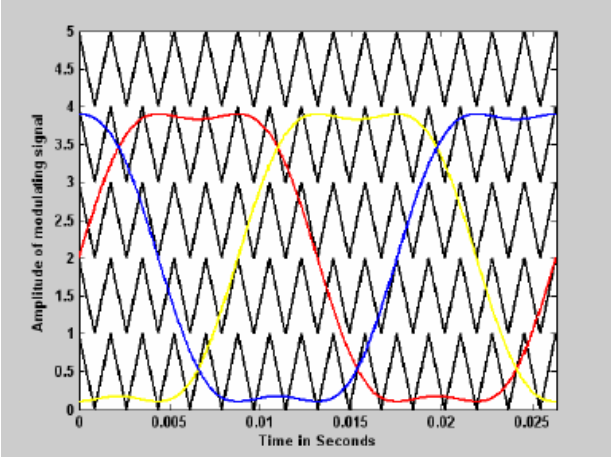

Fig. 4 (e): The reference wave set for 5-level operation in the proposed SPWM

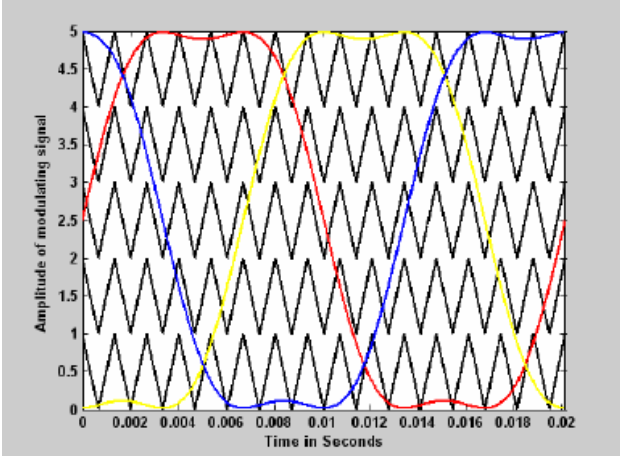

Fig. 4 (f): The reference wave set for 6-level operation in the proposed SPWM

V. Simulation Results and Discussion

Simulation studies have been carried out for the proposed inverter scheme in open-loop v/f control with multilevel carrier based SPWM using SIMULINK software in MATLAB environment. Figure 5 shows the block diagram of the proposed inverter scheme. The respective DC-bus voltages are $(2/6)V_{dc}$, $(2/6)V_{dc}$ and $(1/6)V_{dc}$ for the inverter-1, inverter-2 and inverter-3 respectively. This means that the DC-bus voltage of an equivalent conventional 2-level inverter is V_{dc}. The speed reference is translated to the frequency and voltage commands maintaining V/f. Depending upon the range in which the frequency command falls the reference waves are generated according to Eqn. (14), (15) and (16). The three reference waves are simultaneously compared with the carrier set and the level at which the instantaneous value of the reference wave is determined.

A DC-bus voltage (V_{dc}) of 600 volts is assumed for simulation studies. A load torque of 10 N-m is applied at 0.5sec. Fig.6 shows the motor phase voltage in the lowest speed range and it may be noted that the inverter is operating in the 2-level mode. In this case, inverter-3, being a two level inverter is switched between $(1/6)V_{dc}$ and 0 while the three level inverter (constituted by the cascade connection of inverter-1 and inverter-2) is clamped to zero. Fig.7 shows the motor phase voltageV_{A2A3}, in the next speed range in 3-level operation with the three level inverter is now in the 2-level mode, switching between zero and $(2/6)V_{dc}$ while two level inverter (i.e. inverter-3) switches. Fig.8 shows the motor phase voltage in the next speed range in the 4-level operation, where three level inverter switching in the 2-level mode between zero and $(2/6)V_{dc}$ and two level inverter switched between $(1/6)V_{dc}$ and 0. Fig.9 shows the motor phase voltage for the 5-level operation, in which the three level inverter enters into the three level operation switching between 0, $(2/6)V_{dc}$ and $(4/6)V_{dc}$ while the two level inverter switched. Fig.10 shows the motor phase voltage in the 6-level operation in which the Three level inverter switching in the 3-level mode between zero and $(4/6)V_{dc}$ and the two level inverter switched in the 2-level mode.

It can be seen that the motor phase voltage during 6-level operation is very smooth and close to the sinusoid with lower THD. Fig.11a to Fig.11e show the phase voltage, transient phase current, steady state phase current, torque and speed of the motor during six-level operation. Fig.12a to Fig.12e show the normalized harmonic spectrum of the motor phase voltage at different levels of operation. Fig.13 shows the decrease of total harmonic distortion (%THD) in the motor phase voltage as the number of levels increased.

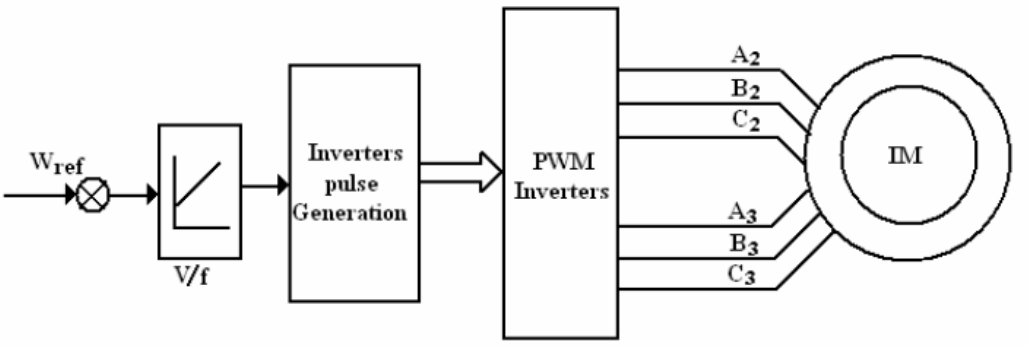

Fig. 5: Block diagram of the proposed SPWM-Inverter

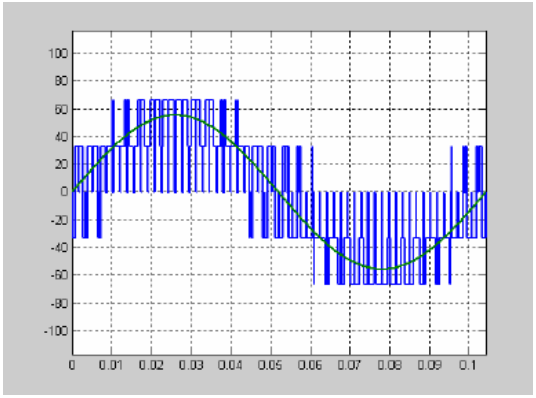

Fig. 6: Motor phase voltage and its fundamental waveform during 2-level operation

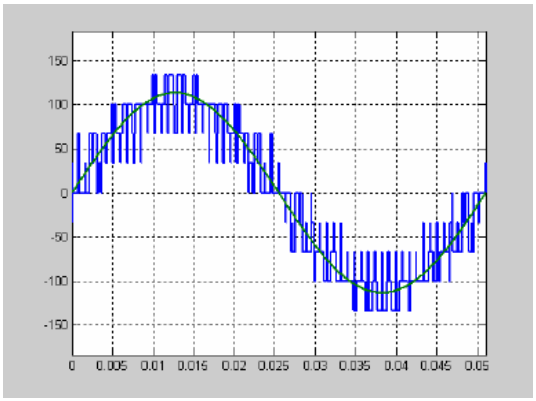

Fig. 7: Motor phase voltage and its fundamental waveform during 3-level operation

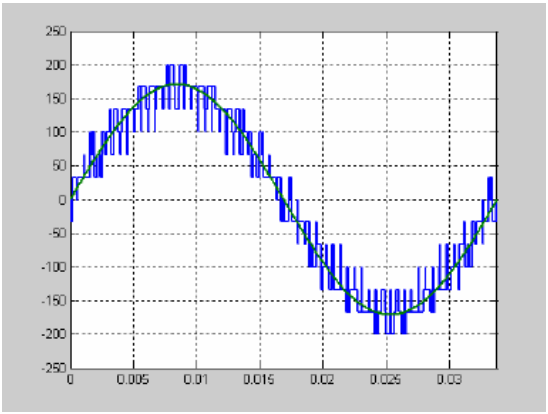

Fig. 8: Motor phase voltage and its fundamental waveform during 4-level operation

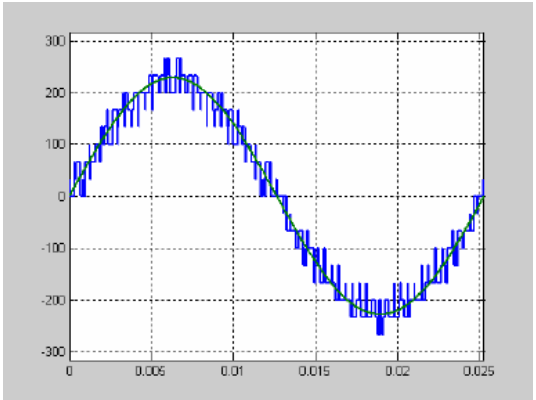

Fig. 9: Motor phase voltage and its fundamental waveform during 5-level operation

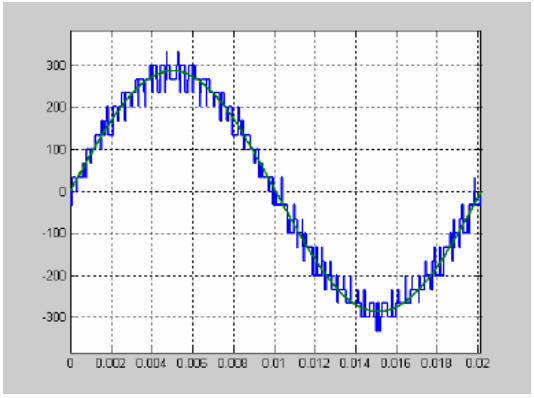

Fig. 10: Motor phase voltage and its fundamental waveform during 6-level operation

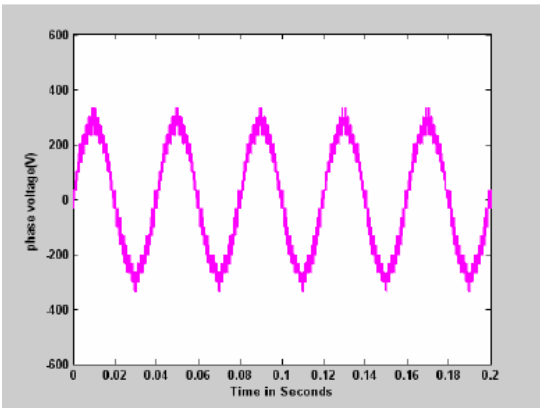

Fig. 11a: Motor phase voltage during 6-level operation (with more number of cycles)

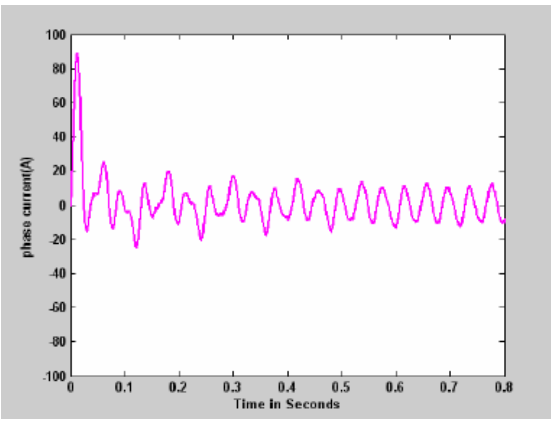

Fig. 11b: Transient motor phase current during 6-level operation

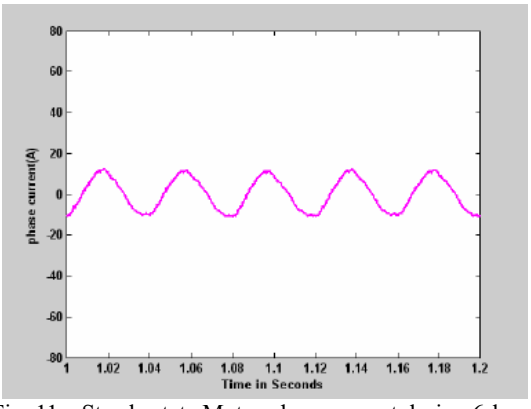

Fig. 11c: Steady state Motor phase current during 6-level operation

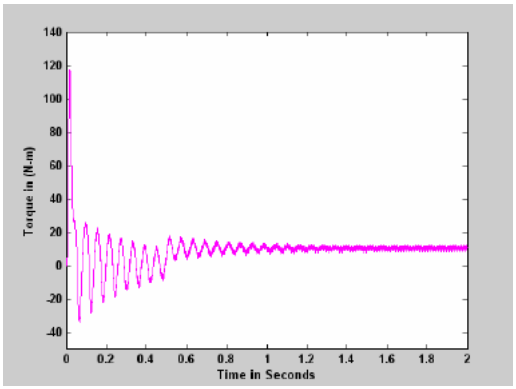

Fig. 11d: Motor torque during 6-level operation

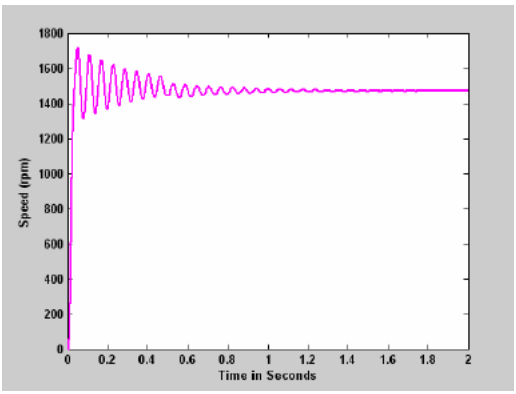

Fig. 11e: Motor speed during 6-level operation

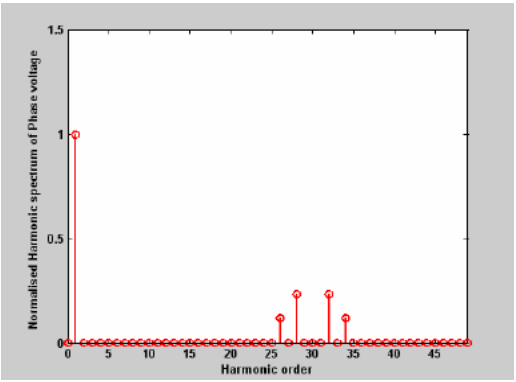

Fig. 12 (a): Normalized harmonic spectrum for the motor phase voltage during 2-level operation

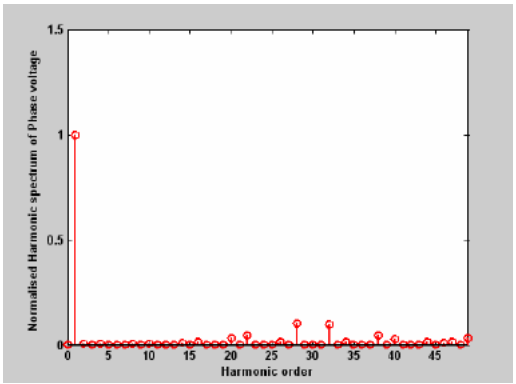

Fig. 12 (b): Normalized harmonic spectrum for the motor phase voltage during 3-level operation

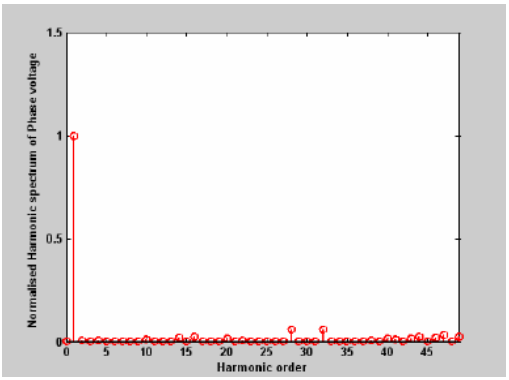

Fig. 12 (c): Normalized harmonic spectrum for the motor phase voltage during 4-level operation

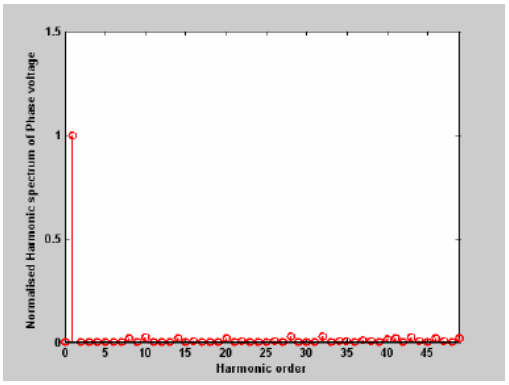

Fig. 12 (d): Normalized harmonic spectrum for the motor phase voltage during 5-level operation

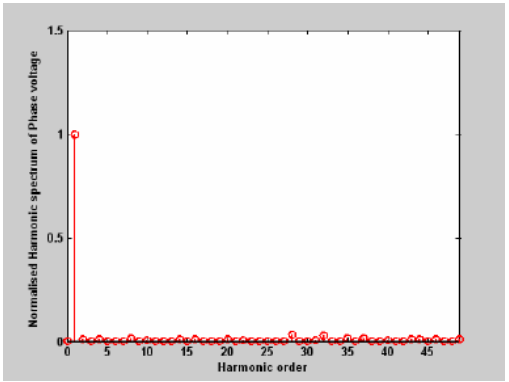

Fig. 12 (e): Normalized harmonic spectrum for the motor phase voltage during 6-level operation

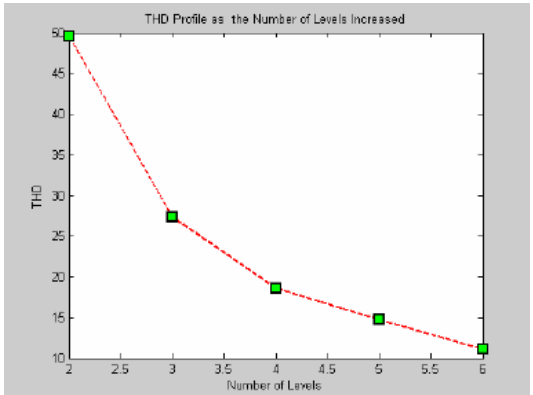

Fig. 13: Total harmonic distortion (%THD) of the motor phase voltage as the number of levels increased

VI. CONCLUSION

An open-end winding induction motor fed by a 3-level inverter from one end and a 2-level inverter from the other end of the motor results in voltage space phasor locations identical to a conventional 6-level inverter. The Three level inverter used is realized by cascading two 2-level inverters. When compared with the cascaded H-bridge topology the present scheme employs a lower number of power supplies and switching devices. The proposed inverter does not experience neutral-point fluctuations and the DC-link capacitors carry only the ripple current as isolated DC supplies are used for all the DC links. When compared with the five-level inverter the switching ripple and THD in the motor phase voltage of proposed inverter is reduced. Multilevel carrier based SPWM, where a progressive discrete DC shift is added to reference wave depending on the speed range, allowing operation in all levels (2-level to 6-level) is employed for the proposed work.

The phase current is also near to sinusoidal and contains low THD. The motor torque reached steady state and responded for a change of load at 0.5 sec. The corresponding speed response is also presented and the speed reached the steady state. The motor exhibits good dynamic response. The phase voltage of six-level operation contains lowest harmonics when compared to that of two-level to five-level operation. As the number of levels increased the %THD in the motor phase voltage decreased.

REFERENCES

[1] A. Nabae, I. Takahashi, and H. Agaki, "A New Neutral-Point-Clamped PWM Inverter", IEEE Transactions on Industry Applications, Vol. IA-17, September-October 1981, pp. 518-523.

[2] P.M. Bhagawat and V.R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter", IEEE Transactions on Industry Applications, 1983, 19(6), pp. 1057-1069.

[3] S.J. Lai and F.Z. Peng, "Multilevel Converter – A New Breed of Power Converter", IEEE Transactions Industry Applications, Vol. 32, No. 3, May-June 1996, pp. 509-517.

[4] R.W. Menzies, P. Steimer and J.K. Steinke, "Five-Level GTO Inverters for Large Inductor Motor Drives", Proceedings of the IEEE Ind. Appl. Soc. Annual Meeting, Toronto, 2-8 October 1993, pp. 595-601.

[5] G, Sinha and T.A. Lipo, "A Four-Level Inverter Based Drive with a Passive Front End", IEEE Transactions Power Electronics, Vol. 15, No. 2, March 2000, pp. 285-294.

[6] T. Meynard and H. Foch, "Imbricated Cells Multilevel Voltage Source Inverters for High Power Applications", EPE Journal, Vol. 3, No. 2, 1993, pp. 99-106.

[7] M.D. Manjrekar and T.A. Lipo, "A Hybrid Multilevel Inverter Topology for Drive Applications", Proceedings of 1998 IEEE – APEC Conference, pp. 523-529.

[8] A. Rufer, M. Veenstra and K. Gopakumar, "Asymmetric Multilevel Converter for High Resolution Voltage Phasor Generation", Proceedings of the 1999 EPE Conference, pp. 1-10.

[9] H. Stemmler and P. Guggenbach, "Configurations of High Power Voltage Source Inverter Drives", Proceedings of the 1993 EPE Conference, pp. 7-12.

[10] E.G. Shivakumar, K. Gopakumar and V.T. Ranganathan, "Space Vector PWM Control of Dual Inverter Fed Open-End Winding Induction Motor Drive", Proceedings of the 2001 IEEE – APEC Conference, pp. 394-404.

[11] E.G. Shivakumar, V.T. Somasekhar, K.K. Mohapatra, K. Gopakumar and L. Umanand, "A Multilevel Space-Phasor Based PWM Strategy for an Open-End Winding Induction Motor Drive Using Two Inverters with Different DC Link Voltage", Proceedings of the 2001 IEEE – EDS Conference, pp. 169-175.

[12] V.T. Somasekhar, K. Chandra sekhar and Gopajumar, "A New Five-Level Inverter System for an Induction Motor with Open-End Winding", Proceedings of the 2003 IEEE – PEDS Conference, pp. 199-204.

[13] V.T. Somasekhar and K. Gopakumar, "Three-Level Inverter Configuration Cascading Two-Level Inverter", IEE Proc.Electr.Power Appl. Vol. 150, No. 3, May 2003, pp.245-254.

[14] G. Carrara, S. Garedella, M. Marchesoni, R. Salutari and G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis", IEEE Transactions Power Electronics, Vol. 7, No. 3, July 1992, pp. 497-505.

[15] D.G. Holmes, "The Significance of Zero Space Vector Placement for Carrier-Based PWM Schemes", IEEE Transactions on Industry Applications, 1996, 32 (5), pp. 1122-1129.

BIOGRAPHIES

K.Chandra Sekhar received his B.Tech degree in Electrical & Electronics Engineering from V.R.Siddartha Engineering College, Vijayawada, India in 1991 and M.Tech with Electrical Machines & Industrial Drives from Regional Engineering College, Warangal, India in 1994. From 1994 to 1995, he was the Design & Testing Engineer in Maitreya Electricals (P) Ltd. Vijayawada. From 1995 to 2000, he worked with Koneru Lakshmaiah College of Engineering as a Lecturer, since 2000, he has been with R.V.R & J.C.College of engineering as Assistant Professor. Presently he is a part-time research student at J.N.T.U College of Engineering, Hyderabad- 500072, India, working towards his doctoral degree.

G.Tulasi Ram Das received his B.Tech degree in Electrical & Electronics Engineering from J.N.T.U college of Engineering, Hyderabad, India in 1983 and M.E with Industrial Drives & Control from O.U College of Engineering, Hyderabad, India in 1986. He Received the PhD, degree from the Indian Institute of Technology, Madras, India in 1996. He is having 20 years of teaching and research experience. He is currently Principal J.N.T.U College of Engineering, Hyderabad- 500 072, India. His Research interests are Power Electronics, Industrial Drives & FACTS Devices.