

# Unity-Power-Factor Operation of Two-Stage Electronic Ballast

V. B. Borghate<sup>1</sup> and H. M. Suryawanshi<sup>2</sup>

**Abstract** – This paper presents the zero-voltage switched power-factor-correction (PFC) circuit. The proposed PFC circuit along with the half bridge asymmetrical series connected parallel loaded resonant inverter is used in the electronic ballast. The current is injected to the dc-bus capacitor at higher frequency as compared to the switching frequency of the inverter circuit. The high frequency (HF) modulated voltage source is generated in series between the input ac source and the dc-bus capacitor by simply using coupling inductor. This helps to boost the dc-bus voltage above the peak of ac input voltage. These lead to the unity-power-factor (UPF) operation of electronic ballast. The HF operation of PFC circuit reduces the switch current, limits the THD below 4.0%, increases the efficiency and reduces the component sizes. The circuit maintains UPF and low THD even under lamp power and input voltage variations. The prototype of the electronic ballast is built-up with inverter circuit to operate at 50 kHz and PFC circuit at 150 kHz. The simulation and experimental results of proposed circuit are presented for 40W fluorescent lamp with 230 V, 50 Hz input.

**Keywords** - Current injection, modulated voltage source, zero voltage switching, unity power factor.

## I. INTRODUCTION

With continuous growth of population in the world, the demand for the power is ever increasing. The lighting is one of the major power-consuming loads. Therefore the electronic ballast operating at high efficiency and high power factor with low total harmonic distortion (THD) has become one of the important areas for the researchers. The continuous research has evolved two-stage [1]-[3] and single-stage electronic ballasts (EB) [4]-[10] operating at high efficiency, high power factor and low THD as compared electromagnetic ballast.

In [6], the HF voltage is derived from the transformer at the output of the inverter and connected in series with the boost inductor after the input diode rectifier to operate the EB at high power-factor and low THD. This HF voltage is of constant magnitude and depends on the dc-bus voltage. The EB in [7] uses the coupling inductor with buck-boost topology and the dc-bus voltage is to be maintained at value above the twice of peak of ac input voltage. This results in high voltage stress on the switches, if EB operates at 230 V, 50 Hz supply input. The topology used for EB in [8] employs the coupling inductor with very

high value of leakage and magnetizing inductances. The leakage inductances are used as the boost inductor. This results in freewheeling of flat-top current at its peak value for the longer time, which may results in saturation of magnetic component of its PFC circuit. In these topologies, the commonly shared switches carry the both PFC as well as inverter currents, which results in increase in their current stresses.

In this paper, independent HF switched PFC circuit is proposed for the EB. The PFC circuit with its magnetic components is switched independently than inverter circuit. The proposed PFC circuit serves three functions as; feedbacks the current from the output of diode-bridge rectifier to the input of the ballast circuit at HF, injects the stored energy to the dc-bus capacitor at HF and generates the HF modulated voltage at the input of the diode-bridge rectifier. Therefore, it maintains unity power factor and low THD at the ac source even under wide change in input voltage condition. HF operation (150 kHz) reduces the sizes of PFC circuit components, filtering requirements, magnitude of current to be injected, and flat-top current time period as compared to other topologies. The dc-bus voltage is required to maintain just above the peak of input ac voltage for operation of PFC circuit in discontinuous conduction mode (DCM). This topology reduces the current stress, voltage stress and power loss of the switches as they handle the PFC and inverter currents separately. Therefore, the proposed circuit operates at high efficiency, unity power factor and low THD. This circuit requires two additional switches as compared to single-stage EB. It is most suitable for high power lamp applications with high reliability, since the separate switches handle the PFC circuit current. The small values of leakage inductances of the coupling inductor (of PFC circuit) are sufficient to filter out the ripples of the input current, therefore, no separate EMI filter is required.

The operation and analysis of the proposed circuit are presented in the next section. The simulation is carried out to get insight of the circuit operation. The experimental results are obtained from the laboratory prototype fabricated for 40W fluorescent lamp at 230V, 50Hz.

## II. OPERATION AND ANALYSIS OF THE PROPOSED PFC CIRCUIT

The circuit diagram of the proposed EB is shown in Fig. 1. The PFC circuit consists of inductor  $L_j$ , capacitors  $C_1$ - $C_2$ , MOSFETS  $M_1$ - $M_2$ , and coupling inductor  $L_c$ . The  $L_j$  injects the current and transfers its stored energy to the dc-bus capacitor and also re-stores energy in every half switching cycle. The  $C_1$  and  $C_2$  act as the filter for the

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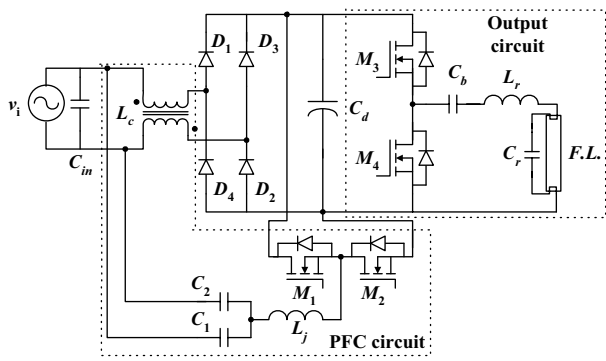


Fig. 1. Circuit diagram of proposed electronic ballast.

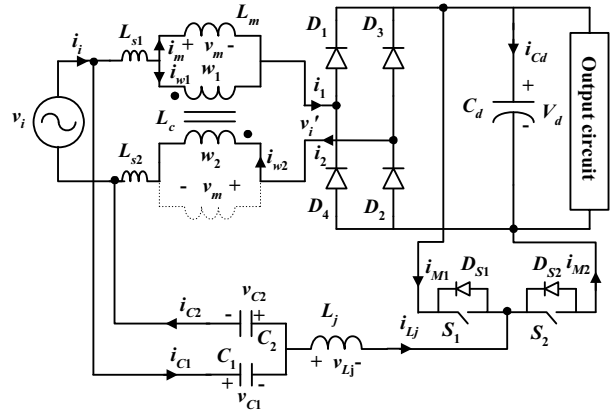


Fig. 2. Equivalent diagram of proposed PFC circuit.

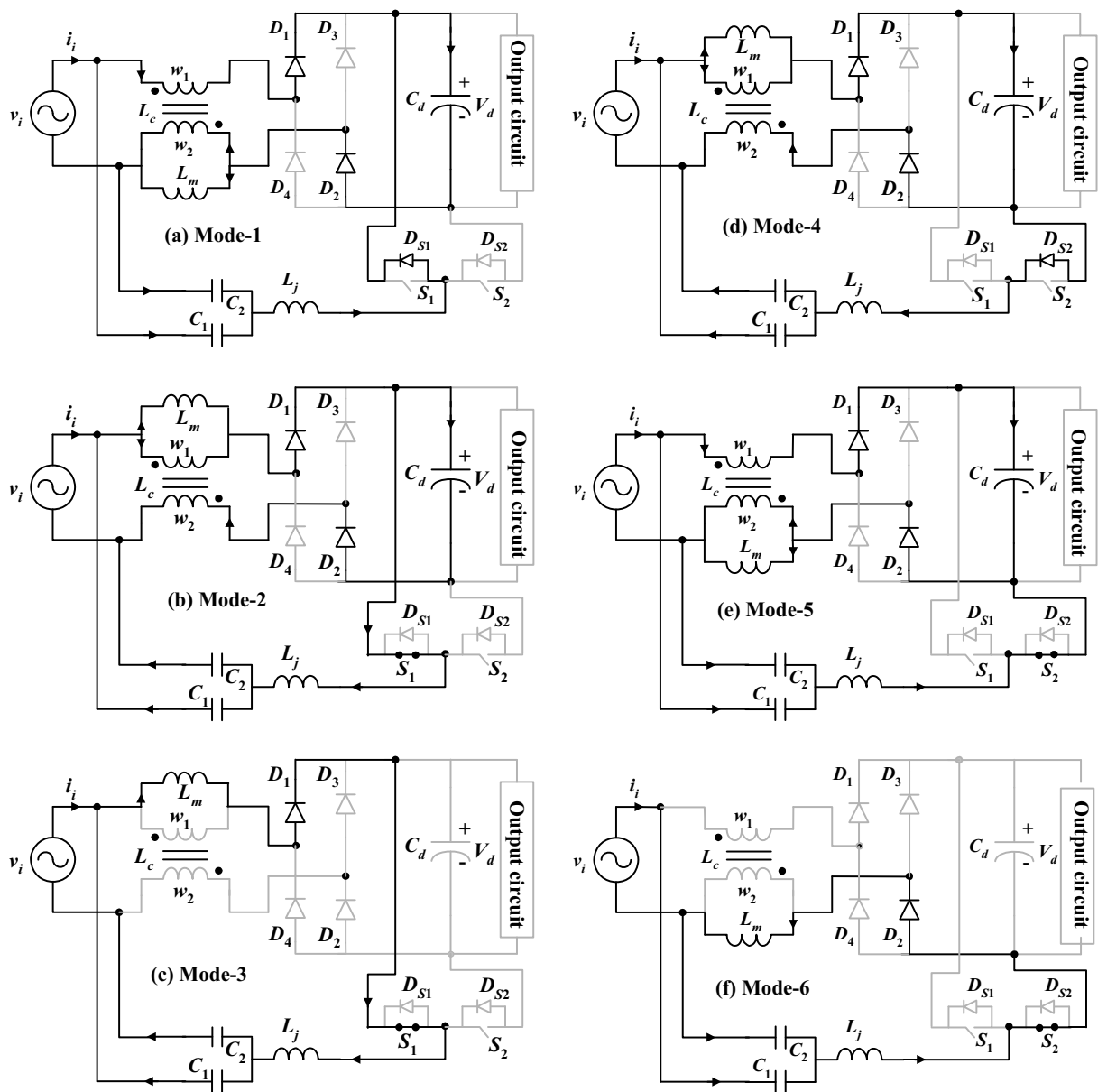


Fig. 3. Operating modes of PFC circuit.

current of  $L_j$ . These capacitors are sufficiently large enough so that the voltage across them remains constant during the switching cycle. The  $L_c$  has two identical coils wound on the common core. These coils carry the current in opposite directions and the cause of induced emf ( $v_m$ ) in the coils is differential current component. Therefore, the  $L_c$  is represented as a transformer with two ideal windings  $w_1$ - $w_2$  and magnetizing inductance  $L_m$  as shown in Fig. 2 of equivalent circuit diagram. The  $w_1$  and  $w_2$  carry the same current, whereas the  $L_m$  carries the differential current of two coils. The  $L_m$  is reflected on the side of  $L_c$ , which carries the larger current. The frequency of the induced emf is double of switching frequency of the PFC circuit and its magnitude decreases with increase in instantaneous value of input ac voltage and vice-versa. This induced emf acts as a HF modulated voltage source connected in series between ac input voltage and dc-bus voltage sources and always boosts the dc-bus voltage above the peak value of ac input voltage over the input 50 Hz cycle to obtain the discontinuous conduction mode (DCM) operation. The PFC and inverter circuits are switched at frequencies  $f_p$  and  $f_i$  respectively.

The following assumptions are made in the analysis.

- All the semiconductor devices and magnetic components are ideal.
- The dc-link capacitor  $C_d$  is large enough to be considered as a ripple free constant voltage source of magnitude  $V_d$ .
- The  $V_d$  is always greater than the peak value  $V_{ip}$  of the ac input line voltage  $v_i$ .
- The input voltage  $v_i$  is constant during a switching cycle, since the switching frequency  $f_p$  of the PFC circuit is much higher than the input supply frequency  $f$ .
- The MOSFETs  $M_1$ - $M_2$  are switched symmetrically with duty ratio ( $d = 0.5$ ).
- The fluorescent lamp operating at HF (50 kHz) is considered as a resistive load [2] of value  $R_{FL}$ .

For clarity, operation and analysis of PFC circuit only are given in this section, since the inverter circuit is well presented in [1]-[10]. It is explained with the help of six modes of operation shown in Fig. 3, and the simulated waveforms of Fig. 4 over one switching time period  $T_s$ . Since the switch capacitances are of small values, the transition of MOSFETs is assumed instantaneous, and therefore the corresponding modes are not included.

#### A. Operating modes

From the above discussion and Fig. 2,

$$i_{w1} = i_{w2}, \text{ and } i_{C1} = \frac{i_{Lj}}{2}, \quad i_{C2} = -\frac{i_{Lj}}{2} \quad (1)$$

$$v_{C1} + v_{C2} = v_i, \quad v_{C1} = v_{C2} = d \cdot v_i = 0.5v_i, \text{ and } V_d > V_{ip} \quad (2)$$

Before the beginning of mode 1, it is assumed that the switch  $S_2$  is in conduction and current  $i_{Lj}$  is circulating through  $S_2$ , and  $L_m$  at its positive peak value  $+I_{Lj}$ , therefore  $i_2 = +I_{Lj}$ , and  $i_1 = 0$ .

Mode-1 ( $t_0$ - $t_1$ ), Fig. 3(a): At  $t_0$ , the switch  $S_2$  is turned off. The diodes  $D_{S1}$  and  $D_1$  start conducting. In this mode, the

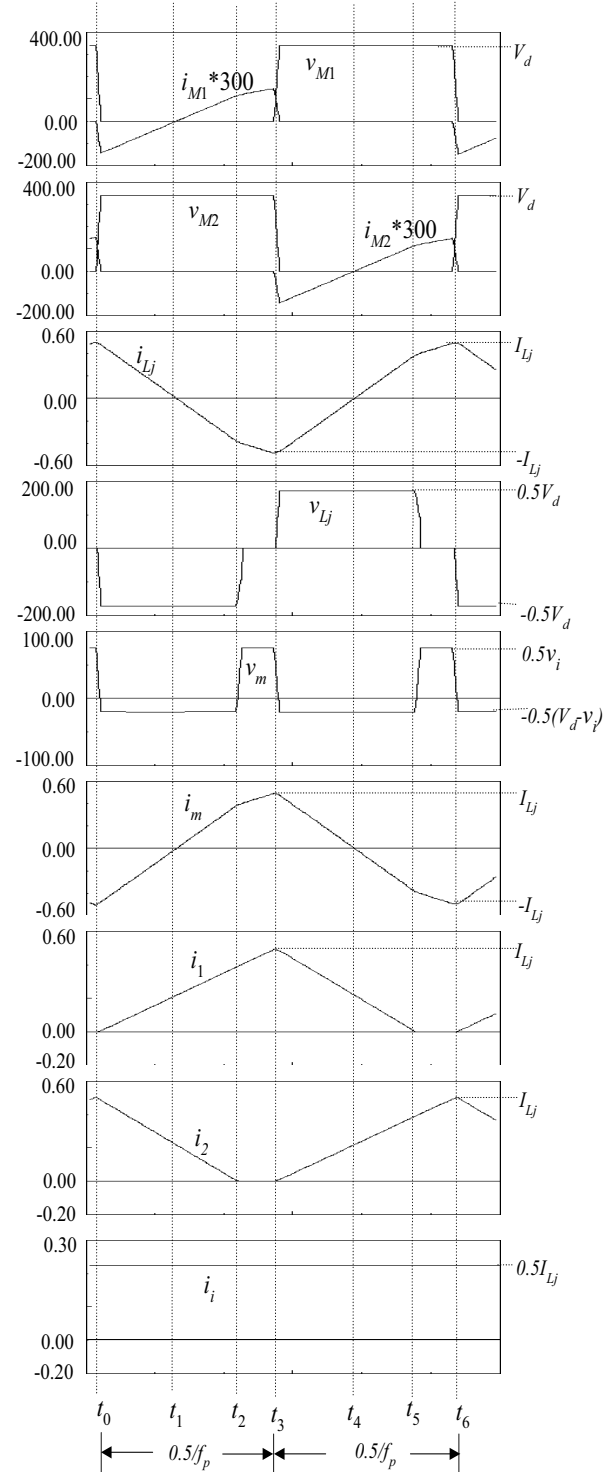


Fig. 4: Simulated waveforms of PFC circuit.

energy stored in  $L_j$  is transferred to  $C_d$ . Therefore, the inductor current  $i_{Lj}$  decreases linearly from its maximum positive value  $+I_{Lj}$  to zero at  $t_1$  as shown in Fig. 4. The energy is also supplied to  $L_m$  from the input source during this mode.

The expression of  $v_m$  &  $v_{Lj}$  with reference to Figs. 2 and 3(a) are,

$$v_i = 2v_m + V_d, \quad v_{Lj} = v_m - v_{C1} = v_{C2} - V_d - v_m \quad (3)$$

Therefore, from (1) to (3)

$$v_m = -\frac{V_d - v_i}{2} \quad (4)$$

$$v_{L_j} = -\frac{V_d - (1-2d)v_i}{2} \quad (5)$$

The inductor current  $i_{L_j}$  decreases linearly as,

$$\begin{aligned} i_{L_j}(t) &= I_{L_j} + \frac{v_{L_j}}{L_j}(t - t_0) \\ &= I_{L_j} - \frac{V_d - (1-2d)v_i}{2L_j}(t - t_0) \end{aligned} \quad (6)$$

As  $i_1 = i_{w1}$  and  $i_{w1} = i_{w2}$ , the MOSFET  $M_1$  current is,

$$i_{M1} = -(i_{DS1} = i_{L_j} = -i_m) \quad (7)$$

$$\text{The input current is, } i_i = i_1 + i_{C1} = i_1 + (i_{L_j}/2) \quad (8)$$

*Mode-2* ( $t_1$ - $t_2$ ), Fig. 3(b): At  $t_1$ ,  $i_{L_j}$  is decreased to zero, therefore the diode  $D_{S1}$  turns off naturally and upper switch  $S_1$  turns on. Thus, it achieved the zero-voltage-switching (ZVS). The energy stored in  $L_m$  is transferred to  $L_j$  through  $S_1$ ; therefore the current through  $L_j$  increases linearly in opposite direction at the same rate as that of last mode and reaches to maximum negative value  $-I_{L_j}$  at  $t_2$  as it stored energy to its full capacity. Therefore,

$$i_{M1} = i_{S1} = i_m = -i_{L_j} \text{ and } i_i = i_1 - (i_{L_j}/2) \quad (9)$$

*Mode-3* ( $t_2$ - $t_3$ ), Fig. 3(c): At  $t_2$ , the diode  $D_2$  turns off because the current  $i_2$  has become zero. During this mode, the current  $i_{L_j}$  is clamped at  $-I_{L_j}$  and the additional energy of  $L_m$  is returned to the input source. Therefore,

$$i_{L_j} = -I_{L_j} = -i_m, \quad i_1 = i_m = i_{S1} = I_{L_j} \quad (10)$$

$$v_{L_j} = 0, \quad v_m = v_{C1} = d \cdot v_i \quad (11)$$

$$\text{and the input current, } i_i = i_{C2} = \frac{I_{L_j}}{2} \quad (12)$$

*Mode-4* ( $t_3$ - $t_4$ ), Fig.3 (d): At  $t_3$ , the switch  $S_1$  is turned off and the diodes  $D_2$  and  $D_{S2}$  start conducting. The energy stored in  $L_j$  is transferred to  $C_d$ ; and the energy is supplied to  $L_m$  from the input source during this mode. The inductor current  $i_{L_j}$  increases linearly from its maximum negative value ( $-I_{L_j}$ ), and becomes zero at  $t_4$ . Therefore,

$$v_i = 2v_m + V_d, \quad v_{L_j} = v_{C2} - v_m = -v_{C1} + v_m + V_d \quad (13)$$

Therefore, using equations (1), (2) and (9),

$$v_m = -\frac{V_d - v_i}{2} \quad (14)$$

$$v_{L_j} = \frac{V_d - (1-2d)v_i}{2} \quad (15)$$

The inductor current  $i_{L_j}$  increases linearly from  $-I_{L_j}$  as;

$$\begin{aligned} i_{L_j}(t) &= -I_{L_j} + \frac{v_{L_j}}{L_j}(t - t_3) \\ &= -I_{L_j} + \frac{V_d - (1-2d)v_i}{2L_j}(t - t_3) \end{aligned} \quad (16)$$

As  $i_2 = i_{w2}$  and  $i_{w1} = i_{w2}$ , the MOSFET  $M_2$  and input currents are

$$i_{M2} = -(i_{DS2} = i_m = -i_{L_j}) \quad (17)$$

$$i_i = i_2 + (i_{L_j}/2) \quad (18)$$

*Mode-5* ( $t_4$ - $t_5$ ), Fig. 3(e): At  $t_4$ , the diode  $D_{S2}$  turns off, as the current through it ( $i_{L_j}$ ) is reached zero. The lower

switch  $S_2$  turns on, thus achieving its ZVS. During this mode, the energy stored in  $L_m$  is transferred to  $L_j$  through  $S_2$ . Therefore the current through  $L_j$  increases linearly at the same rate as that of last mode but in opposite direction and reaches to maximum positive value  $+I_{L_j}$  at  $t_5$  as it has stored energy to its full capacity. During this mode,

$$i_{M2} = i_{S2} = i_m = -i_{L_j} \quad (19)$$

$$i_i = i_2 - (i_{L_j}/2) \quad (20)$$

*Mode-6* ( $t_5$ - $t_6$ ), Fig. 3(f): At  $t_5$ , the diode  $D_1$  turns off as the current  $i_1$  is reached to zero. The inductor current  $i_{L_j}$  is clamped at  $+I_{L_j}$  and the additional energy is returned to the input source during this mode. Therefore,

$$i_2 = -i_m = i_{S2} = i_{L_j} = +I_{L_j}, \quad (21)$$

$$i_i = i_2 - i_{C2} = \frac{I_{L_j}}{2} \quad (22)$$

$$v_{L_j} = 0, \quad v_m = v_{C2} = d \cdot v_i \quad (23)$$

At  $t_6$ , the switch  $S_2$  is turned off and the mode 6 ends, completing one cycle of the switching frequency  $f_p$  of PFC circuit.

### B. Analysis of the PFC circuit

During the modes 1 and 2, the current  $i_1$  varies linearly as,

$$i_1(t) = 0 + \frac{I_{L_j}}{t_2 - t_0}(t - t_0)$$

The instantaneous mean value of  $i_i$  is the sum of the average value of  $i_1$  and  $i_{L_j}/2$  i.e.  $i_{iav} = i_{1av} + \left(\frac{i_{L_j}}{2}\right)_{av}$ .

The average value of  $i_{L_j}$  during  $t_0$  to  $t_2$  is zero. Therefore,

$$i_{iav} = \frac{I_{L_j}}{2} + 0 = \frac{I_{L_j}}{2} \quad (24)$$

During the modes 4 and 5, the current  $i_2$  varies linearly as,

$$i_2(t) = 0 + \frac{I_{L_j}}{t_5 - t_3}(t - t_3)$$

The instantaneous mean value of  $i_i$  is sum of the average value of  $i_2$  and  $i_{L_j}/2$  i.e.  $i_{iav} = i_{2av} + \left(\frac{i_{L_j}}{2}\right)_{av}$

The average value of  $i_{L_j}$  during  $t_3$  to  $t_5$  is zero. Therefore,

$$i_{iav} = \frac{I_{L_j}}{2} + 0 = \frac{I_{L_j}}{2} \quad (25)$$

During the modes 3 and 6, the input current is also  $I_{L_j}/2$ .

That is the instantaneous value of input current is constant and equal to  $I_{L_j}/2$ , and follows the input voltage over the complete switching cycle.

In references [7] and [8], the of leakage inductances of the coupling inductor are used as boost inductor and is given by,

$$L_b = 2L_l = 2 \frac{d^2 T_s V_{ip}^2}{4P_i} = 2 \frac{d^2 V_{ip}^2}{4f_s P_i} \quad (26)$$

And the maximum current through it is,

$$I_b = \frac{T_s V_{ip}}{4L_b} = \frac{V_{ip}}{4L_b f_s} \quad (27)$$

Where  $P_i$ ,  $V_{ip}$  and  $T_s (=1/f_s)$  are the input power, peak value of ac input voltage and the time period of switching cycle of the ballast circuit respectively.

In the proposed topology, the frequency of the inductor current is twice the operating frequency of the PFC circuit. Therefore, the required value of current injecting inductor and its maximum current are,

$$L_j = \frac{d^2 V_{ip}^2}{4(2f_p)P_i} = \frac{V_{ip}^2}{32f_p P_i} = \frac{\eta V_{ip}^2}{32f_p P_o} \quad (28)$$

$$I_{Lj} = \frac{V_{ip}}{8L_j f_p} \quad (29)$$

Therefore, the input current,  $i_i = \frac{V_{ip}}{16L_j f_p} \sin \omega t$  (30)

Where,  $P_o$  and  $\eta$  are output power and efficiency of the ballast circuit at rated input voltage respectively.

From (26) and (28), it is evident that the required values of the  $L_j$  of proposed EB is one-fourth of  $L_b$  in [7,8]. Equation (29) shows that the current  $i_{Lj}$  is half of the corresponding current in other single-stage topologies at the same switching frequency. Their values further reduce with increase in operating frequency of the separately switched PFC circuit.

The minimum value of  $L_m$  required for maintaining the  $V_d$  at  $V_{ip}$  is  $L_j/d$ , if PFC and output circuits are operated at the same frequency. In this topology, PFC circuit is operated at comparatively higher frequency. Therefore, the minimum  $L_m$  is,

$$L_{m \min} = \left( \frac{L_j}{d} \right) \left( \frac{V_d}{V_{ip}} \right) \left( \frac{f_i}{f_p} \right) \quad (31)$$

From above discussions and operating modes, it is evident that,

- The ZVS of MOSFETs  $M_1$ - $M_2$  is achieved inherently.
- The rate of current injection is twice the operating frequency of PFC circuit.
- The magnitude of induced emf  $v_m$  in coupling inductor  $L_c$  varies in inverse proportion of the instantaneous value of the input ac voltage.
- The frequency of  $v_m$  is twice of operating frequency of the separately switched PFC circuit  $f_p$ .
- The both coils  $w_1$ - $w_2$  of  $L_c$  carry the same current in opposite direction, whereas its  $L_m$  carries the equal and opposite current that of inductor  $L_j$ . Therefore, distortions in the input current because of HF injection current  $i_{Lj}$  are minimized.

The value of  $i_{Lj}$  varies from  $+I_{Lj}$  to  $-I_{Lj}$  or vice versa in an each half switching cycle. The rate of variation of  $i_{Lj}$  is double as that of the boost inductor current in single-stage ballast with unconventional PFC circuit [6] and four times as that of the ballast with the two-stage PFC circuit [2]. The input current  $i_i$  remains constant and equal to  $I_{Lj}/2$ ;

and follow the input voltage during the whole switching cycle.

Therefore, this circuit operates at unity power factor with low THD.

### III. DESIGN EXAMPLE

The Laboratory prototype of the proposed electronic ballast is built to drive the 40W fluorescent lamp at 230 V, 50 Hz input source with following circuit parameters and components.

#### A. PFC circuit

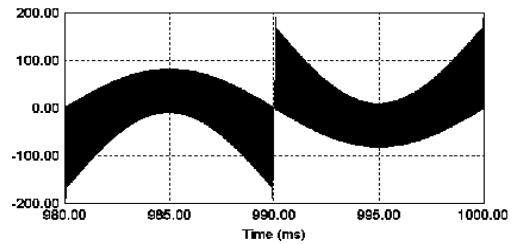
$f_p = 150$  kHz,  $d = 0.5$ ,  $\eta = 0.94$  (assumed),  $L_j = 0.5$  mH,  $L_m = 0.425$  mH,  $L_{s1} = L_{s2} = 5$   $\mu$ H,  $C_1$  and  $C_2 = 0.1$   $\mu$ F (polypropylene).

#### B. Resonant circuit

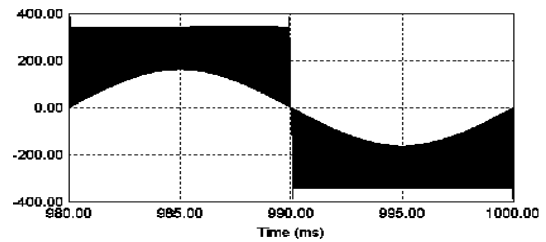
The resonant circuit parameters are finalized by adopting the method described in [7], as given below.

The ratio of dc-bus voltage to lamp voltage,  $(V_{dc}/V_{FL}) = 2$ ,  $Q = 0.9$ ,  $(f_i/f_r) = 1.12$ ,  $f_r = 45$  kHz,  $f_i = 50$  kHz,  $L_r = 1.3$  mH,  $C_r = 10$  nF (Polypropylene),  $C_b = 0.47$   $\mu$ F (Polypropylene)

MOSFETs  $M_1$ - $M_4$ : IRFPC 30 and Diodes:  $D_1$ - $D_4$ : UF408.



(a)



(b)

Fig. 5. Simulated waveform: (a) induced emf ( $v_m$ ) in the  $L_c$ , (b) voltage ( $v_i$ ) at the input of the diode-bridge rectifier

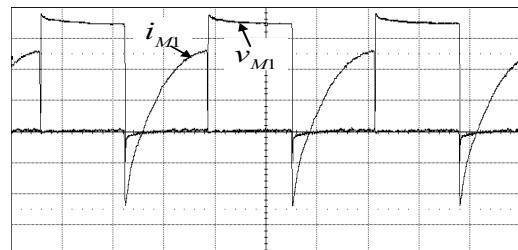


Fig. 6. Experimental ZVS of PFC MOSFET: (100 V/div, 0.2 A/div, 2  $\mu$ s/div).

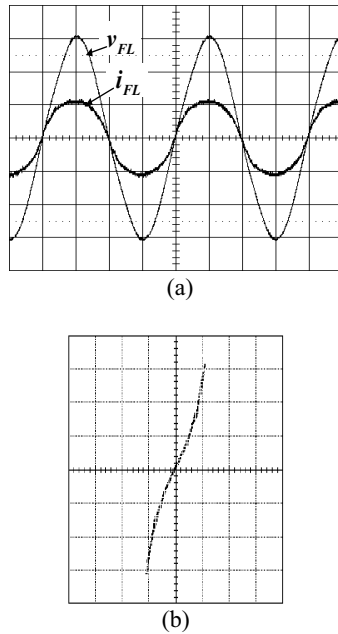


Fig. 7. Experimental lamp waveforms  
(a) voltage ( $v_{FL}$ ) and current ( $i_{FL}$ ) and (b) Measured V-I characteristic at 50kHz: (50 V/div, 0.5 A/div, 10 us/div).

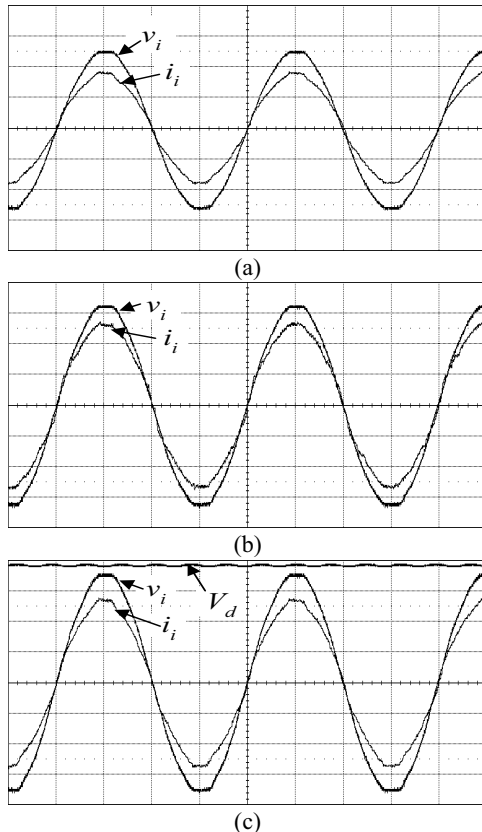


Fig. 8. Experimental waveforms of input voltage ( $v_i$ ), input current ( $i_i$ ) and dc-bus voltage ( $V_d$ ) at (a) 180 V, (b) 230 V and (c) 260 V: (100 V/div, 0.1 A/div, 5ms/div).

#### IV. SIMULATION AND EXPERIMENTAL RESULTS

The simulation and experimental results are obtained for the circuit shown in Fig. 1. From Fig. 5(a), it is evident that the magnitude of the induced HF voltage ( $v_m$ ) in the coupling inductor ( $L_c$ ) varies inversely with the instantaneous value of the input ac voltage. The voltage ( $v_i'$ ) available at the input terminals of the diode-bridge rectifier shown in Fig. 5(b) is modulated at frequency of

$v_m$ . Its magnitude is constant over the input cycle, and equal to sum of instantaneous input ac voltage ( $v_i$ ) and twice the induced voltage, which keeps the diodes in conduction at the valley of ac input line voltage. The frequency of the  $v_m$  and  $v_i'$  is twice the operating frequency of the PFC circuit, that is 300 kHz. The inverter output circuit is operating in lagging mode, since the inverter switches are operated above the resonant frequency (45 kHz). Therefore, the inverter switches  $M_3$  and  $M_4$  operate with ZVS [1]-[10]. Fig. 6 indicates the ZVS operation of the active power switches of PFC circuit. The lamp voltage and current waveforms ( $V_{FL}$  and  $i_{FL}$ ) shown in Fig. 7(b) are sinusoidal in nature. The current shape is sinusoidal and circular because of operation of inverter circuit at just above the resonant frequency, slightly nonlinear lamp behavior and non-ideal components. This is evident from V-I characteristic of the lamp shown in Fig. 7(a). The input ac voltage, current and dc-bus voltage waveforms shown in Fig. 8 substantiate the claim that the proposed circuit takes ripple-free input current at unity power factor even with variation in input voltage. The dc-bus voltage ( $V_d$ ) is marginally above the peak of ac input voltage as shown in Fig. 8(c). The measured efficiency of the circuit is 94.2 % and its THD at 3.9 % at the rated input voltage.

#### V. CONCLUSION

This paper has presented a new circuit for the electronic ballast based on the two-stage boost converter topology. It uses the separately switched PFC circuit, which serves three functions viz. current injection; current feedback and generating the HF modulated voltage of constant magnitude at the input of the diode bridge rectifier to keep them in conduction even at valley point of the input ac line voltage to obtain the unity power factor. The very small leakage inductances of the coupling inductor of PFC circuit filter out the HF ripples of the input current, and no additional EMI filter is required.

The operation and analysis of the proposed PFC circuit is given in detail. The experimental results are obtained of the laboratory prototype built for fluorescent lamp of 40 W at 230 V, 50 Hz. It maintains unity power factor, high efficiency and low THD (below 4.0 %) even under lamp power and input voltage variations. The proposed topology can also be used effectively with high reliability for high-power-lamp application at 230 V mains.

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