Reduced PWM Harmonic Distortion for a New Topology of Multilevel Inverters

Tamer H. Abdelhamid

Abstract—**Harmonic elimination problem using iterative methods produces only one solution, not necessarily the optimal solution. In contrast to using iterative methods, an approach based on solving polynomial equations using the theory of resultant, which produces all possible solutions, is used. The set of switching angles that produces the lowest THD is considered. This paper demonstrates how reduced harmonic distortion can be achieved for a new topology of multilevel inverters. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels. The modes of operation are outlined for 5-level inverter, as similar modes will be realized for higher levels. Simulation of different number of levels of the proposed inverter topology along with corroborative experimental results are presented.**

Keywords—**Multilevel inverter, harmonic elimination, programmed PWM.**

I. Introduction

The general concept of multilevel power conversion was introduced more than twenty years ago. However, most of the development in this area has occurred over the past five years. Multilevel converters have emerged as a very important alternative in the area of high-power medium-voltage applications [1]. Multilevel inverters have the ability to synthesize waveforms with a better harmonic spectrum. However, their increasing number of devices tends to reduce the overall reliability and efficiency of the power converter.

The principal function of multilevel inverters is to synthesize a desired ac voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells [2]. The desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. With an increasing number of dc sources, the inverter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme.

While many different multilevel inverter topologies have been proposed, the two most common topologies are the cascaded H-bridge inverter and its derivatives [3], and the diode-clamped inverter [4]. The main advantage of both topologies is that the rating of the switching devices is highly reduced to the rating of each cell. However, they have the drawback of the required large number of switching devices which equals 2(k-1) where k is the number of levels. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency.

Cascaded H-bridge inverter has a modularized layout and the problem of the dc link voltage unbalancing does not occur, thus easily expanded to multilevel. Due to these advantages, cascaded H-bridge inverter has been widely applied to such applications as HVDC, SVC, stabilizers, and high power motor drives.

Diode-clamped inverter needs only one dc-bus and the voltage levels are produced by several capacitors in series that divide the dc bus voltage into a set of capacitor voltages. Balancing of the capacitors is very complicated specially at large number of levels. Moreover, three-phase version of this topology is difficult to implement due to the neutral-point balancing problems.

The output waveforms of multilevel inverters are in a stepped form, therefore they have reduced harmonics compared to a square wave inverter. To reduce the harmonics further, carrier-based PWM methods are suggested in the literature [5]. Another approach to reduce the harmonics is to calculate the switching angles in order to eliminate certain low order harmonics. The harmonic elimination problem was formulated as a set of transcendental equations that must be solved to determine the angles in an electrical cycle for turning the switches on and off so as to produce a desired fundamental amplitude while eliminating specific low order harmonics. Available techniques to determine such angles include iterative techniques and resultant theory. Iterative numerical techniques, such as *Newton-Raphson* [6], method gives only one solution, while the theory of *Resultant* produces all possible solutions [7]. These sets of solutions have to be examined for its corresponding THD in order to select the set witch generate the lowest harmonic distortion.

This paper presents how reduced harmonic distortion is achieved for a new topology of multilevel inverters using programmed PWM technique. This new topology has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. It can also be extended to any number of levels. The modes of operation of a 5-level inverter is presented, where similar modes can be realized for higher levels. The inverter operation is controlled using switching angles based on programmed PWM method. These angles are obtained from solving the waveform equations using the theory of resultants. Simulation of higher levels of the proposed inverter topology is carried out using PSpice. The validity of the proposed topology and the harmonic elimination method are verified experimentally for 5 and 7 level inverters.

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II. Multilevel Inverter New Topology

In order to reduce the overall number of switching devices in conventional multilevel inverter topologies, a new topology has been proposed. The circuit configuration of the new 5-level inverter is shown in Fig.1. It has four main switches in H-bridge configuration Q_1~Q_4, and two auxiliary switches Q_5 and Q_6. The number of dc sources (*two*) is kept unchanged as in similar 5-level conventional cascaded H-bridge multilevel inverter. Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Fig.2. The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, and for the sake of simplicity, the modes of operation will be illustrated for 5-level inverter, these modes are:

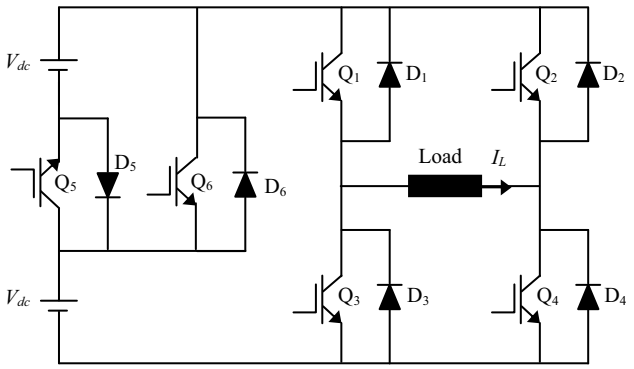

Fig. 1: The 5-level inverter of the new topology

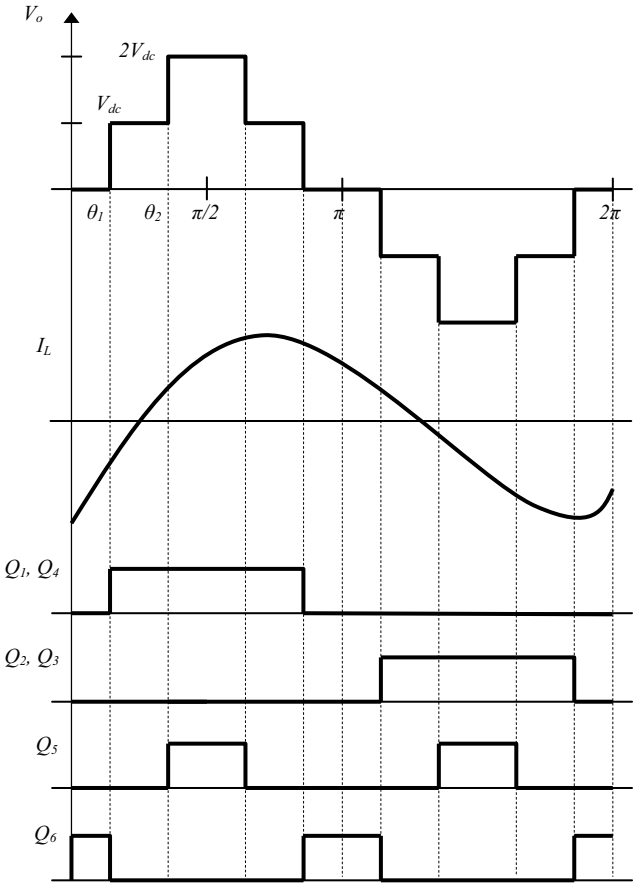

Fig. 2: Waveforms of the proposed 5-level inverter

Powering Mode

This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is V_{dc}, the current pass comprises; the lower supply, D_6, Q_1, load, Q_4, and back to the lower supply. When the output voltage is $2V_{dc}$, current pass is; the lower source, Q_5, the upper source, Q_1, load, Q_4, and back to the lower source. In the negative half cycle, Q_1 and Q_4 are replaced by Q_2 and Q_3 respectively.

Free-Wheeling Mode

Free-wheeling modes exist when one of the main witches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q_1, load, and D_2 or Q_4, load, and D_3, while in the negative half cycle the current pass includes Q_3, load, and D_4 or Q_2, load, and D_1.

Regenerating Mode

In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vise-versa, where the output voltage is zero. The positive current pass comprises; load, D_2, Q_6, the lower source, and D_3, while the negative current pass comprises; load, D_1, Q_6, the lower source, and D_4.

The 7-level version of the proposed topology is shown in Fig.3, where another dc supply, and two auxiliary switches, Q_7 and Q_8, are added while keeping the four main switches, Q_1~Q_4, unchanged. The corresponding output voltage waveform, load current, and gating signals are shown in Fig.4, where the abovementioned modes of operation can also be realized.

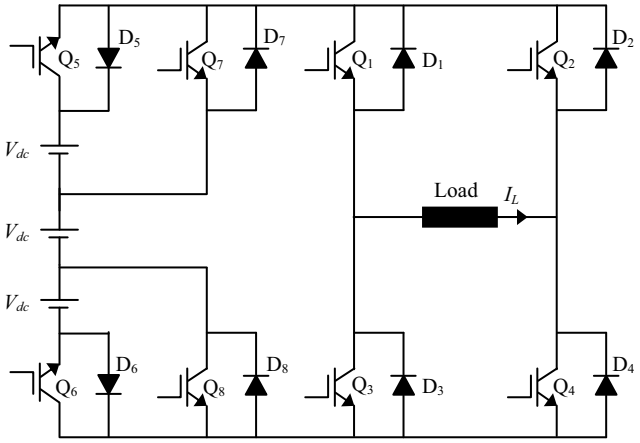

Fig. 3: The 7-level inverter of the new topology

A generalized circuit configuration of the new topology is shown in Fig.5. The proposed topology has the advantage of the reduced number of power switching devices, but on the expense of the high rating of the main four switches. Therefore, it is recommended for medium power applications.

The percentage reduction in the number of power switches compared to conventional H-bridge multilevel inverter is shown in Table 1.

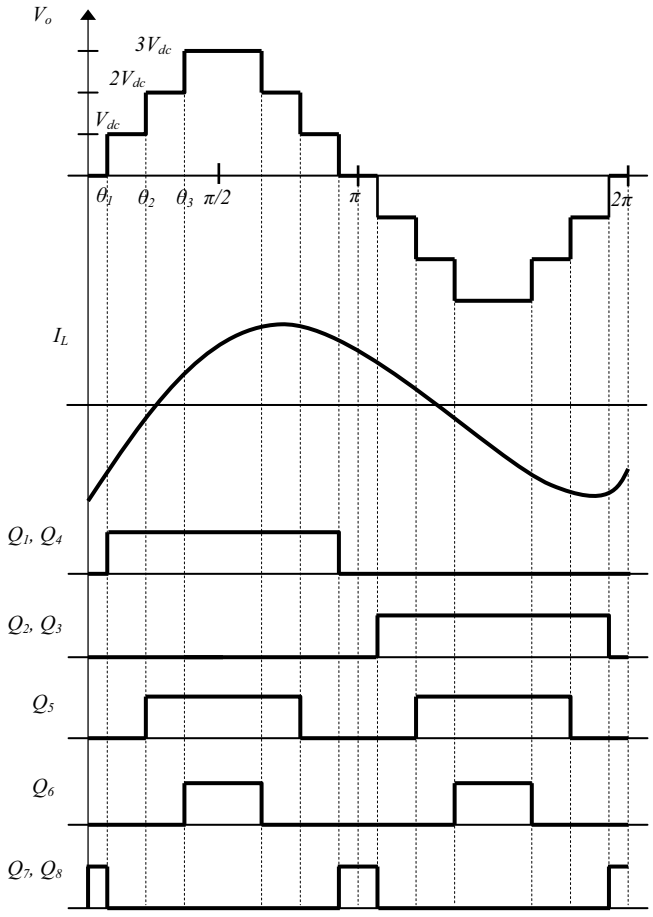

Fig. 4: Waveforms of the proposed 7-level inverter

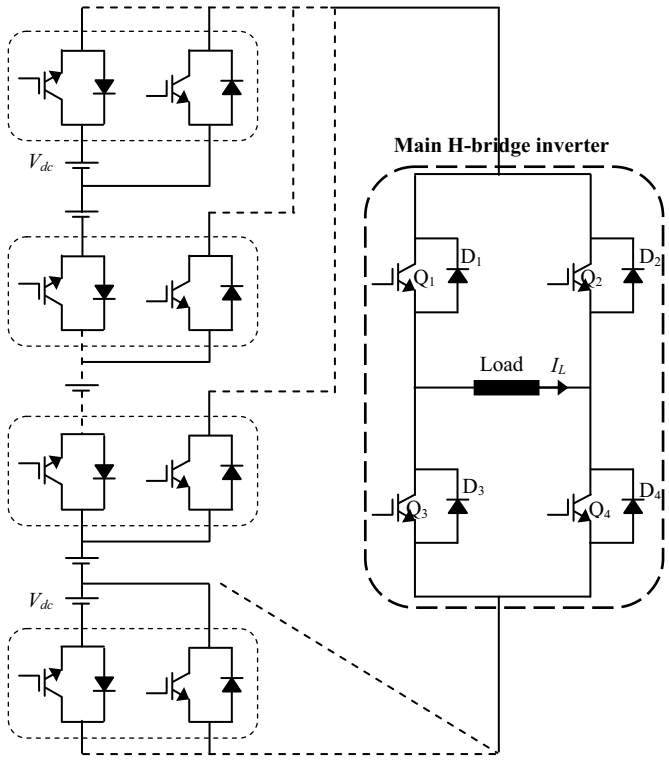

Fig. 5: Generalized multilevel inverter configuration of the new topology

Table 1: Percentage reduction in switching devices

	Number of switches			
Inverter type	5-level	7-level	9-level	11-level
Cascaded H-bridge	8	12	16	20
Proposed topology	6	8	10	12
% Reduction	25%	33.3%	37.5%	40%

III. Mathematical Method of Switching

In order to verify the ability of the proposed multilevel inverter topology to synthesize an output voltage with a desired amplitude and better harmonic spectrum, programmed PWM technique is applied to determine the required switching angles. It has been proved that in order to control the fundamental output voltage and eliminate n harmonics, therefore n+1 equations are needed. Therefore, 7-level inverter, for example, can provide the control of the fundamental component beside the ability to eliminate or control the amplitudes of two harmonics, not necessarily to be consecutive. The method of elimination will be presented for 7-level inverter such that the solution for three angles is achieved.

The Fourier series expansion of the output voltage waveform using fundamental frequency switching scheme shown in Fig.2 is as follows:

$$V_o(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi}\left(\cos(n\theta_1) + \cos(n\theta_2) + ... + \cos(n\theta_s)\right)\sin(n\omega t) \quad (1)$$

Where s is the number of dc sources in the multilevel inverter. Ideally, given a desired fundamental voltage V1, one wants to determine the switching angles θ_1, θ_2,…, θ_s so that $V_o(\omega t)=V_1\sin(\omega t)$, and a specific higher harmonics of $V_n(n\omega t)$ are equal to zero. The switching angles can be found by solving the following equations:

$$\left.\begin{aligned} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) &= m \\ \cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) &= 0 \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0 \end{aligned}\right\} \quad (2)$$

Where $m=V_1/(4V_{dc}/\pi)$, and the modulation index m_a is given by $m_a=m/s$, where $0 \le m_a \le 1$.

One approach to solving the set of nonlinear transcendental equations (2), is to use an iterative method such as the Newton-Raphson method [6]. In contrast to iterative methods, the approach here is based on solving polynomial equations using the theory of resultants which produces all possible solutions [7]. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Then the resultant method is employed to find the solutions when they exist. These sets of solutions have to be examined for its corresponding total harmonic distortion (THD) in order to select the set which generate the lowest harmonic distortion (mostly due to the 11th and 13th harmonics). The computed THD in percent is defined by:

$$\%THD = \sqrt{\frac{V_3^2 + V_5^2 + V_7^2 + \cdots\cdots + V_{19}^2}{V_1^2}} \times 100 \qquad (3)$$

Transforming the transcendental equations (2) into polynomial equations using the change of variables:

$$x_1 = \cos\theta_1\,,\ x_2 = \cos\theta_2\,,\ x_3 = \cos\theta_3 \qquad (4)$$

And the trigonometric identities:

$$\cos(3\theta) = -3\cos\theta + 4\cos^3\theta$$
$$\cos(5\theta) = 5\cos\theta - 20\cos^3\theta + 16\cos^5\theta \qquad (5)$$

To transfer (2) into the equivalent conditions:

$$\left.\begin{aligned} p_1(x) &= x_1 + x_2 + x_3 - m = 0 \\ p_3(x) &= \sum_{i=1}^{3}\left(-3x_i + 4x_i^3\right) = 0 \\ p_5(x) &= \sum_{i=1}^{3}\left(5x_i - 20x_i^3 + 16x_i^5\right) = 0 \end{aligned}\right\} \qquad (6)$$

System (6) is a set of three polynomial equations in three unknowns x_1, x_2, and x_3, where $x = (x_1, x_2, x_3)$, and the angles condition must satisfy $0 \le x_3 \le x_2 \le x_1 \le 1$. Polynomial systems were also considered to compute the solutions of the harmonic elimination equations by iterative numerical methods which give only one solution [9]. In contrast, this system of polynomial equations will be solved using resultant such that all possible solution of (2) can be found. A systematic procedure to do this is known as elimination theory and uses the notion of resultants. The details of this procedure can be found in [9].

IV. Computational Results

Using the abovementioned technique, the polynomial (6) are solved for all possible solutions (sets of switching angles) for any given value of m. The THD produced by output waveform using each of these sets of switching angles is then computed and the particular solution (set of switching angles) that produces the smallest THD is then chosen. That is, the particular waveform and switching angles are simply dictated by the process of solving the harmonic elimination equations for the solution that produces the lowest THD.

A considerable number of simulation results were obtained for different values of inverter levels. Simulation results for 5-level inverter at V_{dc}=50V, and m_a=0.8 (where s=2, and m=1.6) are shown in Figs. 6 and 7. To verify the harmonic elimination method, FFT of the inverter output voltage is shown in Fig. 8. Since only two angles are available in 5-level inverter, it is only possible to eliminate the 3rd harmonic and to control the fundamental component by ma. For ma=0.8, $V_1 = (4mV_{dc}/\pi)$ =101.8V.

The corresponding simulation results, at the same values of V_{dc} and m_a, for 7-level inverter are shown in Figs. 9, 10, and 11, where 3 angles are obtained such that the 3rd and 5th harmonics are eliminated and V_1=152.78V. Note also that the current waveform is improved as a result of the increased number of levels.

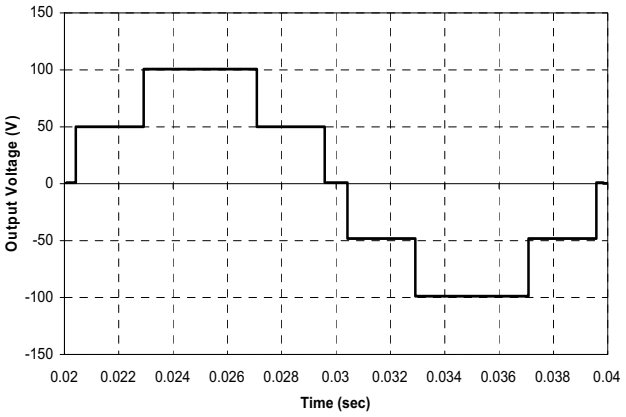

Fig. 6: Output voltage of 5-level inverter at V_{dc}=50V, and m_a=0.8

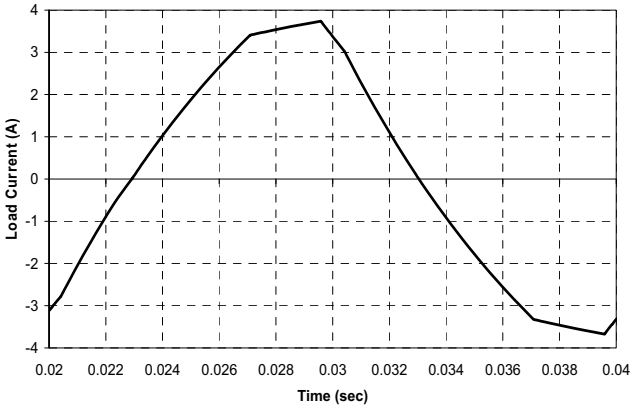

Fig. 7: Load current of 5-level inverter at V_{dc}=50V, and m_a=0.8

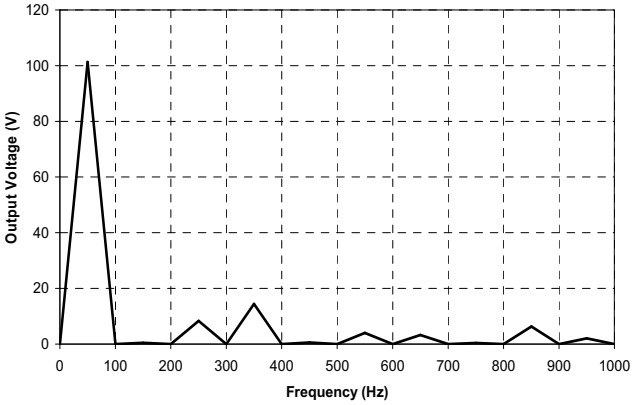

Fig. 8: Harmonic spectrum of output voltage of 5-level inverter at V_{dc}=50V, and m_a=0.8

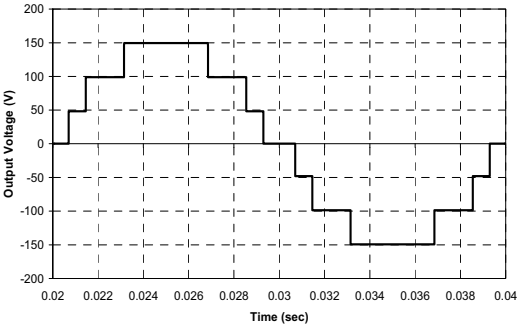

Fig. 9: Output voltage of 7-level inverter at V_{dc}=50V, and m_a=0.8

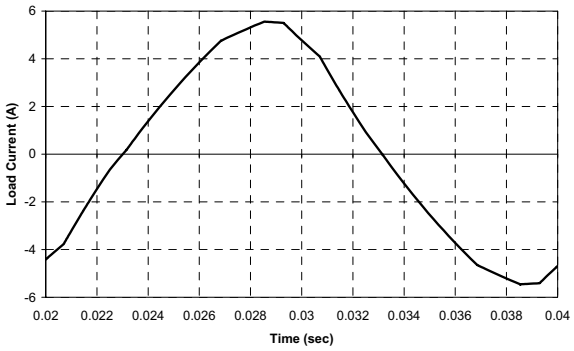

Fig. 10: Load current of 7-level inverter at V_{dc}=50V, and m_a=0.8

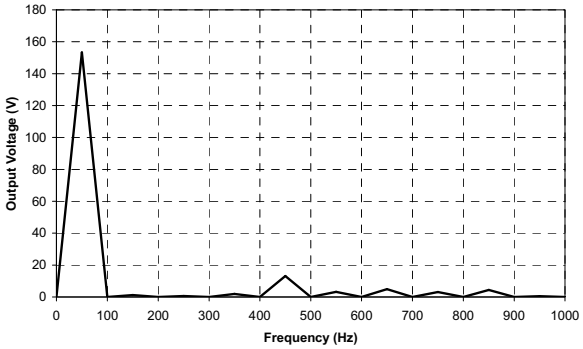

Fig. 11: Harmonic spectrum of output voltage of 7-level inverter at V_{dc}=50V, and m_a=0.8

Simulation results are extended to 9-level inverter which has four dc sources (s=4) as shown in Figs. 12 and 13, where the 3rd, 5th, and 7th harmonics are eliminated and an output voltage of 203.7V is obtained at V_{dc}=50V, and m_a=0.8.

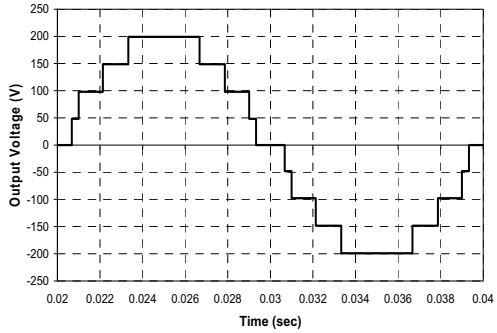

Fig. 12: Output voltage of 9-level inverter at V_{dc}=50V, and m_a=0.8

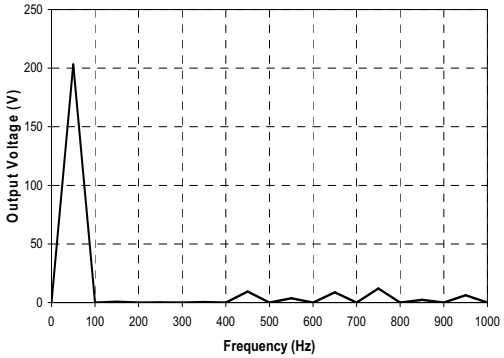

Fig. 13: Harmonic spectrum of output voltage of 9-level inverter at V_{dc}=50V, and m_a=0.8

V. Experimental Verification

The proposed multilevel inverter circuits with the described harmonic elimination method have been implemented. The prototype inverters have been built using IRF520 100V-10A MOSFETs as switching devices. A real-time controller based on the available MCB-1A Hampden microprocessor kit is used to implement the harmonic elimination PWM method. The switching angles obtained from solving the polynomial equations, using the theory of resultant, are stored in the form of look-up tables for different values of modulation indices. Then, these switching angles are converted into time-interval switching patterns using a down-counter and some logic operations, and then stored in an in-house EPROM. The switching patterns obtained from the controller are interfaced to the inverter power switches through optocoupler isolators.

In order to verify the presented idea, the hardware implementation is only developed for 5-level and 7-level inverters, where it can be extended to any number of levels with any desired harmonic profile. The gating signals of the proposed 5-level inverter are shown in Fig. 14, while those of the proposed 7-level inverter are shown in Fig. 15, where signals of Q_2 and Q_3 (not shown) are similar to those of 5-level inverter. A nominal dc link of 20V is used for dc sources. The 5-level inverter output voltage is shown in Fig. 16 at m_a=0.8 (m=1.6). The corresponding FFT is shown in Fig. 17, where a fundamental output voltage of 37V is obtained while the 3rd harmonic is eliminated. The corresponding set of curves for 7-level inverter at m_a=0.8 (m=2.4) are shown in Figs. 18, and 19, where a fundamental output voltage of 56V is obtained while both the 3rd and 5th harmonics are eliminated.

It can be seen that the experimental results are in close agreement with the simulation results. The THD on simulation and experiments are 1.8% and 2.4% respectively. The THD of the experiments is a little higher than that of the simulation because the control resolution is limited 8μs, and the switches are not ideal. The effective switching frequency of the main four switches is 50Hz, while it is 100Hz for the auxiliary switches.

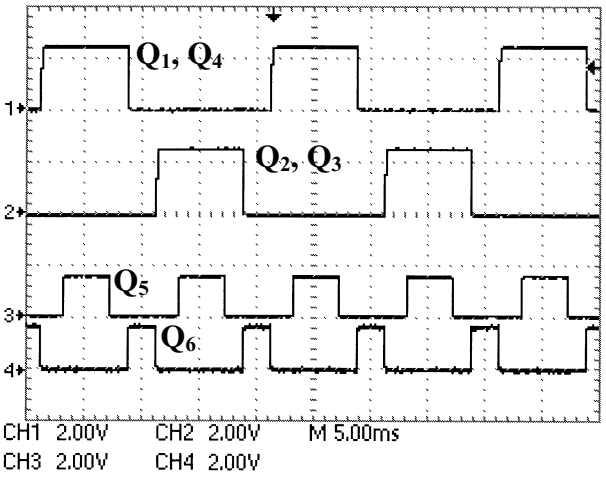

Fig. 14: Gating signals of the proposed 5-level inverter

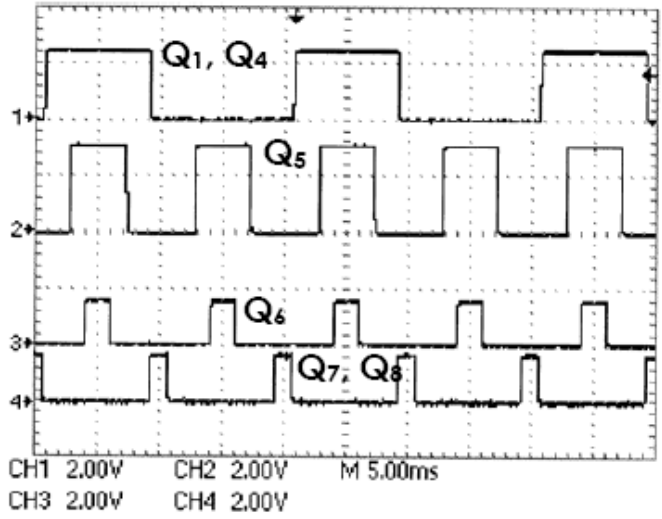

Fig. 15: Gating signals of the proposed 7-level inverter

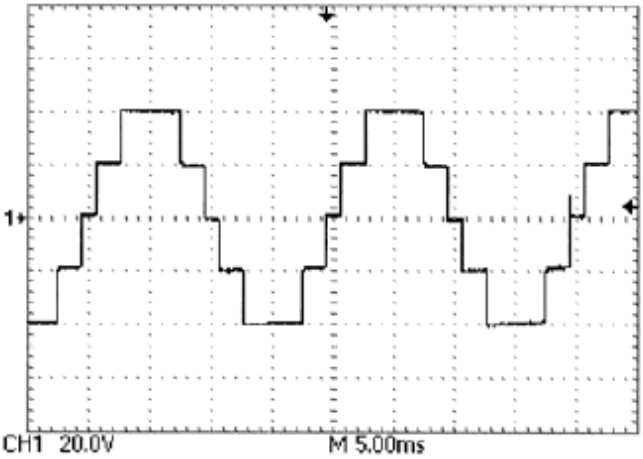

Fig. 16: Output voltage of the proposed 5-level inverter at V_{dc}=20V, and m_a=0.8

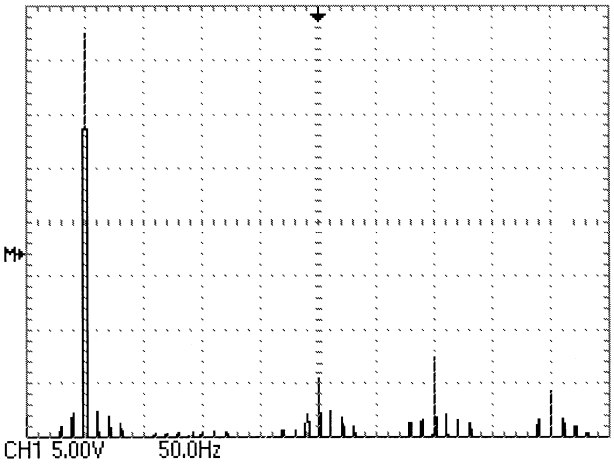

Fig. 17: FFT of 5-level inverter output voltage at V_{dc}=20V, and m_a=0.8

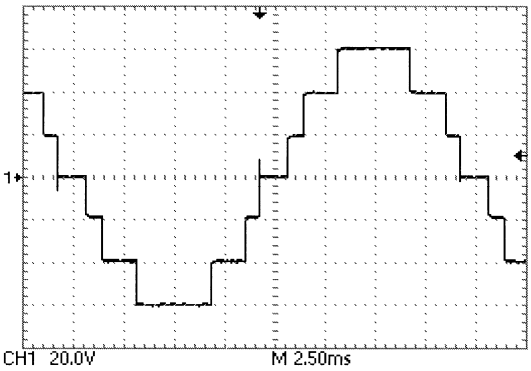

Fig. 18: Output voltage of the proposed 7-level inverter at V_{dc}=20V, and m_a=0.8

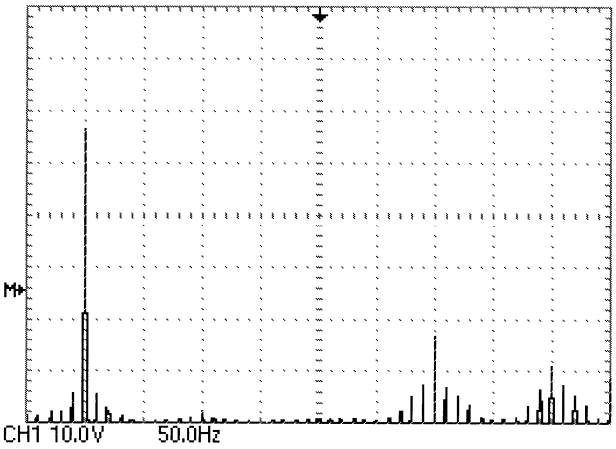

Fig. 19: FFT of 7-level inverter output voltage at V_{dc}=20V, and m_a=0.8

VI. Conclusions

A new family of multilevel inverters has been presented. It has the advantage of its reduced number of switching devices compared to conventional similar inverters. However, the high rating of its four main switches limits its usage to the medium voltage range. The modes of operation and switching strategy of the new topology are presented. A programmed PWM algorithm based on the theory of resultant has been applied for harmonic elimination of the new topology. Since the solution algorithm is based on solving polynomial equations, it has the advantage of finding all existed solutions, where the solution produces the lowest THD is selected. Other PWM methods and techniques are also expected to be successively applied to the proposed topology. The simulation results and experimental results show that the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD.

References

[1] J.S. Lai and F.Z. Peng, "Multileve Converters – A New Breed of Power Converters", IEEE Trans. Ind. Appl., Vol. 32, No.3, 1996, pp. 509-517.

[2] L.M. Tolbert and F.Z. Peng, "Multilevel Converters as a Utility Interface for Renewable Energy System", IEEE

Proceedings-Power Eng. Soc. Summer Meeting, Seattle, WA, 2000, pp. 1271-1274.

[3] K. Corzine and Y. Familiant, "A New Cascaded Multilevel H-Bridge Drive", IEEE Transactions Power Electron., Vol. 17, No.1, 2002, pp. 125-131.

[4] X. Yuan and I. Barbi, "Fundamentals of a New Diode Clamping multilevel Inverter", IEEE Transactions Power Electron., Vol. 15, No.4, 2000, pp. 711-718.

[5] L.M. Tolbert and T.G. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Methods", IEEE Trans. Ind. Appl., 35, 1999, pp. 1098-1107.

[6] H.S. Patel and R.G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I – Harmonic Elimination", IEEE Trans. Ind. Appl., 3, 1973, pp. 310-317.

[7] J.N. Chiasson, L.M. Tolbert, K.J. Mckenzie and Z. Du, "Control of a Multilevel Converter Using Resultant Theory", IEEE Transactions Control System Theory, Vol. 11, No.3, 2003, pp. 345-354.

[8] J. Sun and I. Grotstollen, "Pulsewidth Modulation Basedon Real-Time Solution of Algebraic Harmonic Elimination Equations", Proceedings 20th Int. Conf. Ind. Electron. Contr. Instrum. IECON, 1994, pp. 79-84.

[9] J.N. Chiasson, L.M. Tobert, K.J. McKenzie and Z. Du, "A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters", IEEE Trans. Power Electron., Vol.19, No.2, 2004, pp. 478-490.

BIOGRAPHY

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