IGBT Based Cyclo-Inverter

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Abstract - This paper proposes a novel, power electronics system, an IGBT based Cyclo-Inverter, capable of converting power at the main frequency to a higher frequency. It finds its application in induction heating, fluorescent lighting, ballast, high frequency power supplies and so many other applications where high frequency reduces the size of equipment. A methodology is developed to generate the trigger signals for various IGBTs used in the cyclo-inverter such that the circuit is not restricted to a particular value of output frequency but it can produce any output frequency that is an integer multiple of the input supply frequency. Hardware design is obtained using readily available ICs and other components. The trigger circuit has been tested qualitatively by observing various waveforms on CRO. The operation of proposed system has been found to be satisfactory.

Keywords - Cyclo-Inverter, IGBT, Triggering Pulses, Zero Crossing Detector (ZCD), Operational Amplifier (OPAMP)

I. INTRODUCTION

Developments in the field of DC to AC converter or inverter circuit are a subject of investigation. A wide variety of inverter circuits are possible depending upon the output frequency and voltage [1-4]. Simplest is the single-phase bridge inverter circuit. The output voltage waveform is fairly square and contains harmonics. [5]. Most applications of DC to AC converter prefer a sine wave rather than a square wave output [6]. Sine wave output may be obtained from resonant inverters or load commutated inverters [7- 8]. A unique advantage of this type of inverter is that device-switching loss is eliminated and therefore, the inverter can operate at high frequency (200 Hz to 100 kHz) with high efficiency. One of the main disadvantages with this circuit is that high rating is required for the commutating components because they carry the load current continuously.

In this paper an attempt has been made to design direct AC-to-AC converter or cyclo-inverter, which uses self commutated device IGBT and eliminates the need for external commutation circuit. The converter is suitable for heating and melting applications [9], active power filters, low EMI, high power density UPS and so on. Trigger requirements are obtained for single-phase centre tapped transformer configuration. Hardware design is obtained using readily available ICs and other components. Experiment results are presented for a resistive load.

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II. PROPOSED CONVERTER

Fig. 1 shows the detailed circuit of the proposed converter. It consists of two converters a positive converter PC and a negative converter NC connected in anti parallel. IGBTs 1 and 2 form positive converter whereas IGBTs 3 and 4 form negative converter, NC. Output is obtained through proper conduction of IGBTs in the two input cycles. For example, to generate an output frequency double to the input frequency a firing sequence of 14, 23, 14, …, and so on, is adopted whereas for an output frequency of three times that of input frequency, this firing sequence becomes 141, 323, 141, …, and so on. Thus, the output of converter will have a frequency, $f_o = f_i \times N_r$ where N_r is an integer and f_i is the source frequency.

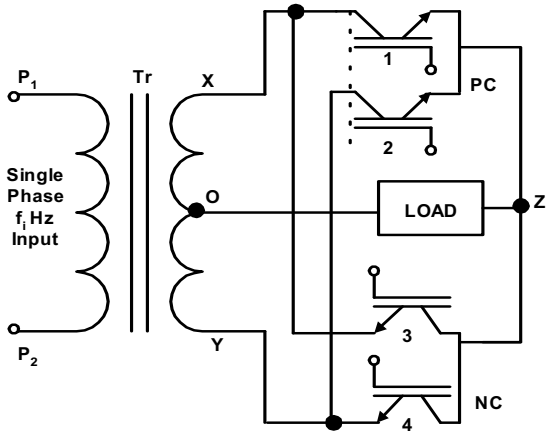

Fig. 1: IGBT Based Frequency Multiplier

Fig. 2 shows the idealized waveform with a firing sequence of 14, 23, and 14, for an output frequency double to the input frequency for a purely resistive load.

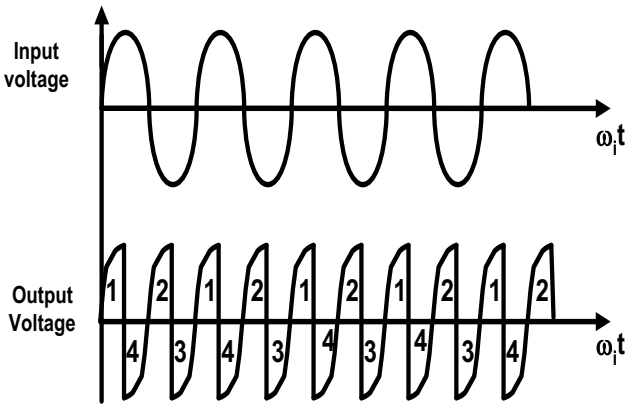

Fig. 2: Idealized Waveform of Converter for $f_o = f_i \times 2$

III. Principle Of Triggering Pulse Generation

There is a definite firing sequence for a given value of N_r to generate the high frequency output f_o. Fig. 3 shows the schematic details of the trigger scheme to generate the required high frequency output. The input signal having frequency f_i, which has to be converted into high frequency signal, is stepped down from a step down transformer in input stage. It is then converted into a square signal using Zero Crossing Detector (ZCD). Another reference signal, having frequency f_o is derived directly from a frequency multiplier using a Phase lock loop PLL and a divide by N_r counter. The two signals are then fed to a pulse generator block, which generates the required pulse for IGBT. The output of pulse-wave generator is fed to the driver circuit, which isolates and boosts the level of pulses.

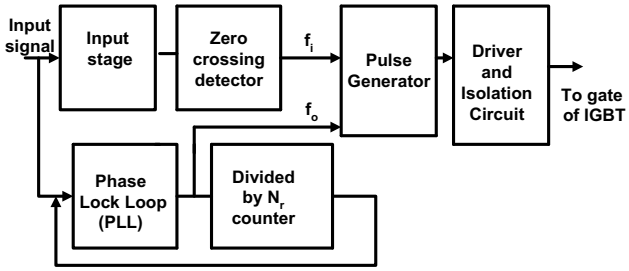

Fig. 3: Block Diagram for trigger pulse generation

The isolated pulses thus obtained, drive the gate of individual IGBTs. The next section illustrates the hardware implementation of this technique.

IV. Hardware Implementation

The trigger requirements are obtained for single phase to single phase centre tapped transformer configuration. Block diagram of Fig. 3 has been designed using following sub circuits.

A. Input Stage and Zero Crossing Detector

A step down transformer (220 V/6 V), connected to the main source is used in the input stage of the control circuit. Since the transformer operates at a frequency f_i it provides the desired input frequency reference to the control circuit. The polarity of secondary voltage V_r is matched with that of secondary of power transformer. The voltage V_r is fed to the zero crossing detector (ZCD) as shown in Fig. 4.

A zero crossing detector consists of a comparator, LM 741, suitable to give TTL - compatible output. It compares input voltage V_r with a reference voltage kept at zero. The output is driven into positive saturation when V_r passes zero in positive direction. When V_r changes its direction the output switches and becomes zero. Diodes *D1* and *D2* clamp the OPAMP inputs to ± 0.7 V and protect it from damage due to excessive input voltage. The resistance R is selected to limit the current through D_1 and D_2 to safer value of 1.2 mA.

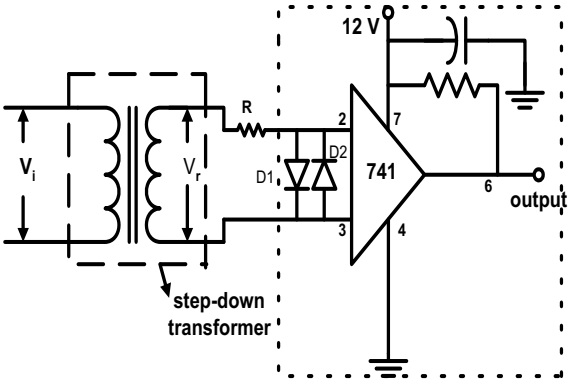

Fig. 4: Input Interfacing Circuit

B. Square Wave Generation at frequency f_o

A square wave output at frequency f_o is generated by using a PLL and a divide by N_r counter. Fig. 5 shows the block diagram for a frequency multiplier using PLL IC 565. It consists of phase comparator, amplifier, low pass filter and VCO. The phase comparator compares the input frequency f_i with the feed back frequency f_o and generates an output signal which is function of the difference between the phases of two input signals. The output signal of the phase comparator is a dc voltage. The output of phase comparator is applied to low pass filter to remove high frequency noise from the dc voltage. This output of the filter is known as error voltage or control voltage for VCO.

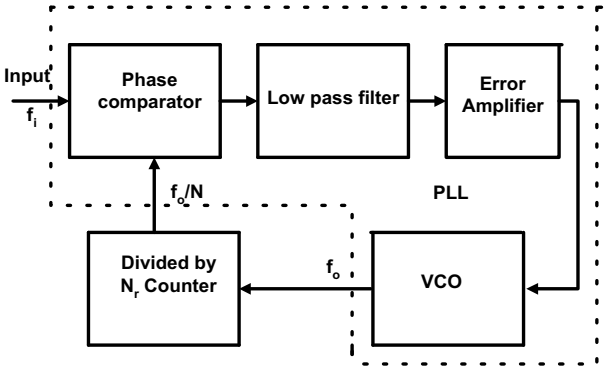

Fig. 5: Block diagram of frequency multiplier using PLL

When control voltage is zero VCO is in free running mode and its output frequency is called as center frequency f_o. The nonzero control voltage results in a shift in the VCO frequency from its free running frequency. f_o to a frequency $f = f_o + K_v V_C$, where K_v is the voltage to frequency transfer coefficient of the VCO. The control voltage applied as the input to VCO, forces the VCO to change its output frequency in the direction that reduces the difference between the input frequency and the output frequency of VCO. This action commonly known as capturing continues till the output frequency of VCO is same as the input frequency. Once the two frequencies are same the circuit is locked.

If a divide by N_r counter is inserted between the VCO output and the phase comparator input then the output of the counter will be locked to the input frequency f_i, and VCO will be actually running at a multiple of the input frequency. Therefore, in the locked state, the VCO output frequency f_o is given by

$$f_o = N \times f_i \quad (1)$$

By selecting proper divide by N_r network, desired multiplication is obtained.

Fig. 6 shows the detailed circuit diagram of IC 565 used as a frequency multiplier. The frequency, f_o, of VCO is given by (2)

$$f_o = 0.31/R_oC_o \quad (2)$$

Here R_o and C_o are external resistor and capacitor connected to pins 8 and 9, respectively. The values of R_o and C_o are adjusted such that free running frequency will be at the center of the input frequency range. The value of R_o is restricted from 2 kΩ to 20 kΩ, but a capacitor can have any value. A capacitor C_2 connected between pin 7 and positive supply (pin 10) forms a first order low pass filter with an internal resistance of 3.6 kΩ.

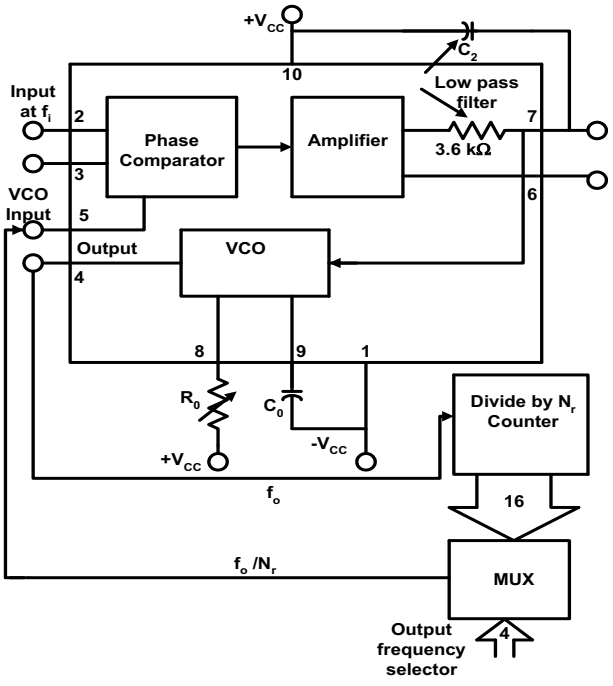

Fig. 6: Detailed circuit diagram of IC 565 used as used as a frequency multiplier

The output of PLL is fed to a divide by N_r counter. The counter counts the output of VCO for a predetermined period defined by the output frequency f_o, and thus toggles at N_r times the output frequency. The counter which has been implemented using a 4×16 decoder and 16 mod counters (mod 2, mod 3, ---- up to mod 17), has sixteen separate output channels, one for each N_r. Fig. 7 shows a divide by N_r counter implemented for N_r from 2 to 17. A particular mod counter and output channel is selected by taking a 4 bit word $U_1U_2U_3U_4$ from user and decoding it by a 4×16 decoder according to the truth table shown in Table 1.

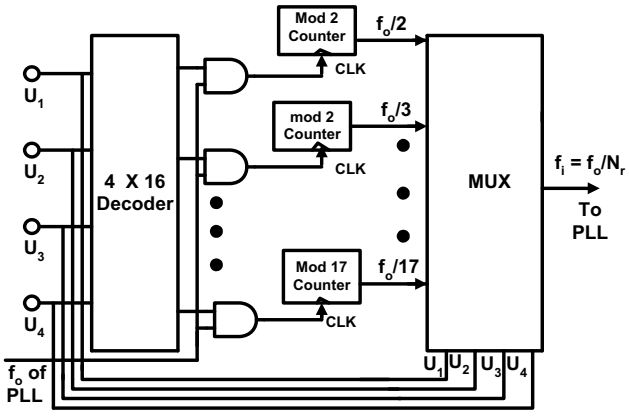

Fig. 7: Divide by N_r counter for N_r from 2 to 17

Table 1 Truth Table for Decoder

U1	U2	U3	U4	N_r
0	0	0	0	2
0	0	0	1	3
0	0	1	0	4
-				
-				
1	1	1	1	17

The maximum count N_r obtainable with the counter corresponds to the maximum output frequency to be generated.

The counter outputs are connected to a 16 to 1 multiplexer. Using four single pole double throw switches generates the four bit multiplexer address. Depending upon the desired output frequency the multiplexer address is selected. The output of MUX is thus at a frequency f_o /N_r which is well synchronized with f_i.

C. Pulse Wave Generation

The triggering pulses are different for the same IGBT for different values of N_r. For example for $N_r = 3$, the gating pulses are generated using two set of pulses having frequencies 50 Hz (input supply frequency) and 150 Hz (N_r times the input supply frequency that is desired output frequency) as shown in Fig. 8.

Let X1 represents the pulses at a frequency of 50 Hz and X2 of 150 Hz. Then ANDing of X1 and X2 will result the pulses required by the IGBT T1. Further if this X2 is inverted by a NOT gate, then the ANDing of X1 and X2' will result the pulses required by the IGBT T4. Similarly, ANDing of X1' and X2 result the pulses required by IGBT T2 and then ANDing the X1' and X2' finally generates the required pulses required for IGBT T3.

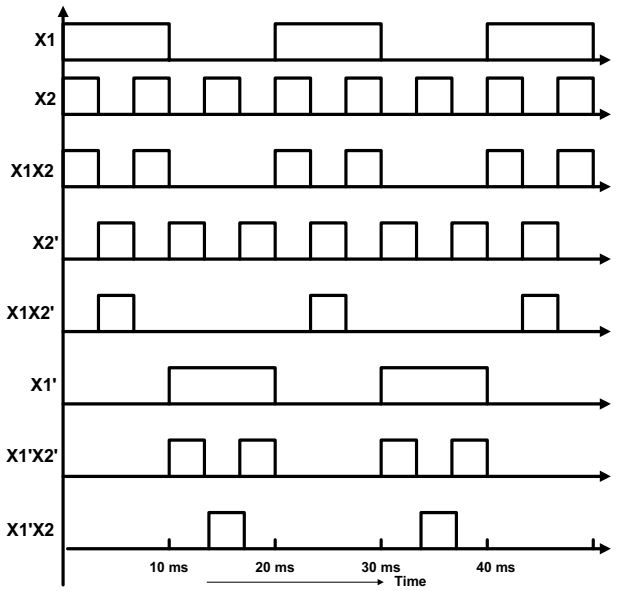

Fig. 8: Gate pulses for Different IGBTs

The circuit diagram to obtain the required pulses is shown in Fig. 9

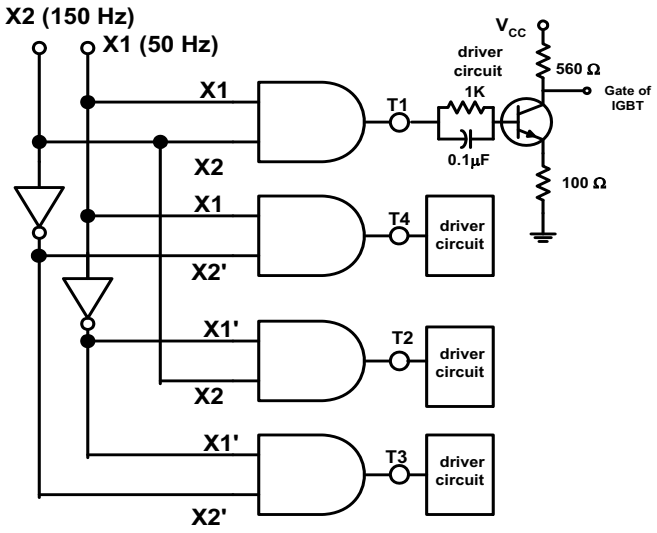

Fig. 9: Circuit Diagram to Generate Gate Pulses

The pulses produced by the pulse wave generator circuit are usually at low power level. They may not be able to trigger the devices into conduction if fed directly. These pulses are therefore boosted to high power level by a circuit known as *driver circuit*. A transistor, in the driver circuit operates in the active region. It is designed to operate in the voltage range of 5 - 20V. As the voltage is increased from 0V to 20Vthe same voltage will appear across the collector and emitter but the voltage across the collector resistance increase only up to 15V for 20V of input. The amplified pulses are isolated using opto-coupler 4N35 and fed to the gate of respective IGBT.

V. Experimental Results

Testing of trigger system and its hardware involves ascertaining that the trigger signals are produced at correct instants. Experimental results are obtained qualitatively by observing the waveforms on CRO at salient points of the control circuit. Fig. 10 shows the complete system diagram of IGBT based cyclo inverter. It consists of a center-tapped transformer, four IGBTs, IRG4PH40UD, with ultra fast soft recovery diode, trigger circuit board, driver circuit and opto couplers for isolation. A variable resistance is used as a load. The input center-tapped transformer rating is 3 kVA.

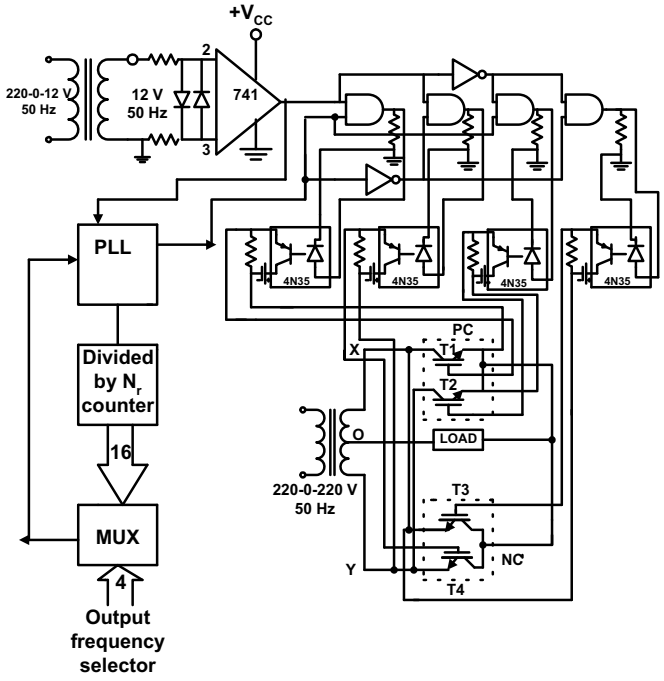

Fig. 10: System Diagram of complete set-up.

Assuming that the power factor to be 0.8, the output power of the transformer will be given as 3× 0.8 = 2.4 kW. Table 2 shows the input and output voltage and current of the module for N_r =3. The circuit has been tested for different loading conditions and average output efficiency thus obtained is approximately 90.1%.

Table 2 Input and Output voltage and current for N_r =3

$V_{in}(V)$	$I_{in}(A)$	$P_{in}(kW)$	$V_o(V)$	$I_o(A)$	$P_o(kW)$	η
220	5.5	1.21	210.7	5.2	1.0956	90%
220	10.96	2.411	210.7	10.7	2.225	92.0%
220	8.11	1.77	210.7	7.9	1.66.5	90.0%

Trigger signal for IGBTs T1 and T3 are shown in Fig. 11 for N_r = 3.

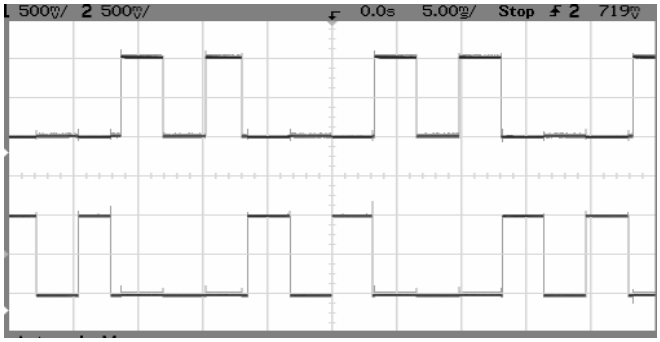

Fig. 11: Trigger signals for IGBTs T1 (upper trace: 2.5 V/div) and T3 (lower trace: 2.5 V/div) for N_r = 3

Figures 12, 13 and 14 show the trace of output voltage of proposed converter for N_r =2, N_r = 3 and N_r = 4 respectively. Fig. 15 shows the combined trace of input and output voltage waveforms of the module Due to some voltage drop in the circuit the output voltage level is somewhat less than the input supply voltage level. Though the output obtained through this converter is enriched with harmonics but this can be shaped to a sinusoidal waveform by incorporating some advanced modulation techniques. The converter is designed to work satisfactory in the output frequency range of 100 Hz to 850 Hz. The range may be extended by selecting the input address of multiplexer circuit more than four bits.

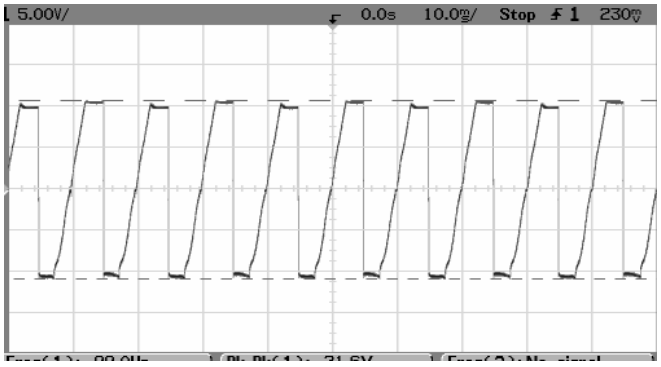

Fig. 12: Output voltage of Converter for N_r =2 (50 V/div)

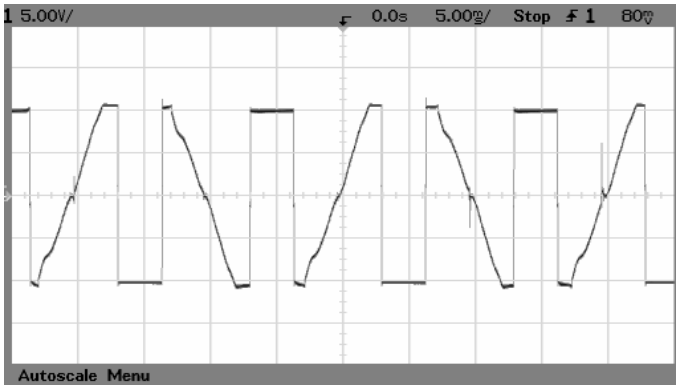

Fig. 13: Output Voltage of Converter for N_r = 3 (50 V/div)

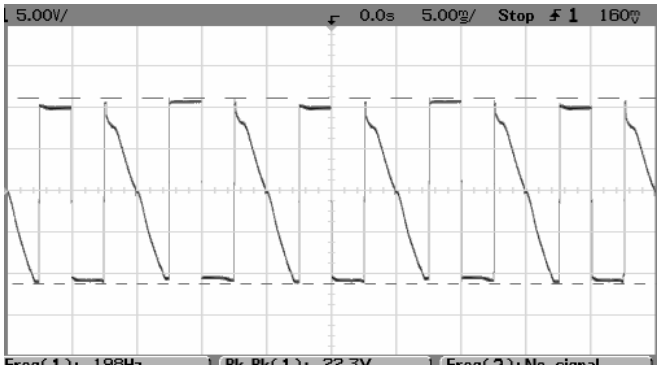

Fig. 14: Output Voltage of Converter for N_r = 4 (50 V/div)

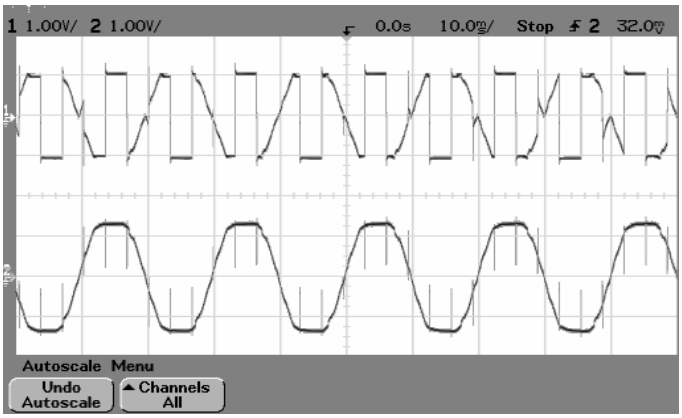

Fig. 15: Input (lower trace: *100* V/div) and output voltage (upper trace: 50 V/div) for N_r = 3

VI. Conclusions

A direct IGBT based AC-to-AC converter has been developed which generates an output at a frequency that is higher than the input frequency. A methodology is obtained for generating the required trigger signal for any integer multiple output frequency. Hardware realization of control circuit and power circuit has been done using readily available ICs and less expensive JK flip flops. Using the proposed design so that no new components are needed for changing the value of N_r from one value to another reduces the complexity of the control circuit. The trigger circuit has been tested qualitatively by observing the various waveforms on CRO. The operation of proposed system has been found satisfactory.

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BIOGRAPHY

Vineeta Agrawal has graduated from Allahabad University, India, in 1980, and received Master’s degree in Electrical Engineering in 1984, from the same university. She joined as lecturer in 1982 in Electrical Engineering Department in M. N. R. Engineering College and since then she has been teaching in the same college. During teaching, she did her Ph.D. course in Power Electronics.

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