Investigation of DC-DC Converter Topologies for Future Microprocessor

K. Rajambal [1] P. Sanjeevikumar [2] G. Balaji [3]

Abstract – Future generation microprocessors are expected to exhibit much heavier loads and much faster transient slew rates. Today's Voltage Regulator Module (VRM) will need a large amount of extra decoupling and output filter capacitors to meet future requirements, which basically makes the existing VRM topologies impractical. This paper is concerned with the investigation into topologies capable of meeting future VRM requirements. Three such topologies, the Interleaved Quasisquare-wave (QSW) topology, the Phase-shift buck (PSB) converter and the ZVS self-driven 12-V voltage regulator, are identified and the performance comparison of these three 12-V VRM topologies is presented. Based on simulation results, the optimum topology with high efficiency and fast transient response is identified.

Keywords – Buck, interleaved, phase shift, QSW, self-driven, voltage regulator module.

I. INTRODUCTION

Since the early 80s, computer industry has experienced rapid expansion. Processors are becoming faster and more powerful. Accordingly, their power consumption has increased dramatically. To decrease power consumption and increase the speed, the next generation of computer microprocessors will operate at significantly lower voltages and higher currents than today's generation. In order to provide the power as quickly as possible, the voltage regulator (VR), a dedicated DC/DC converter is placed in close proximity to power the processor. Moreover, the total voltage tolerance will become much tighter. Generally, the Voltage Regulator Module (VRM) is required to operate with a high efficiency. All these requirements pose very serious design challenges. Table 1 shows the specifications for current and future VRMs [1].

A typical structure of a microprocessor power system is shown in Fig. 1. The processor, which is represented by a current source i_L, is powered up from a power supply or voltage regulator module with regulated output voltage V_o. To reduce the effect of the interconnect inductance L_{interc} between the output of the power supply and the processor, decoupling capacitance C_{decoup} is placed right across the processor power supply pins. The most dramatic load transients occur in the processor transition from the sleep mode to the active mode and vice versa, as illustrated in Fig. 2. Moreover, the transition between the sleep and active modes occurs in a very short period of time, resulting in extremely high slew rates di_L/dt [2]. This paper presents the design procedure and simulation results of the three 12-V VRM topologies namely the Interleaved Quasisquare-wave (QSW) topology,

The paper first received 8 Apr 2008 and in revised form 19 Sep 2008.
Digital ref: AI70301193

[1] Department of Electrical and Electronics, Pondicherry Engineering College, Puducherry, India, E-mail: rajambalk@gmail.com
[2] SimulationSolutions,Chennai, India, E-mail: sanjeevi_12@yahoo.co.in
[3] Department of Electrical and Electronics, Pondicherry Engineering College, Puducherry, India, E-mail: rajambalk@yahoo.com

Table 1: Present and future VRM specifications

	Present	Future
Output Voltage	2.1~3.5V	1~3V
Input Voltage	5V	12V
Load Current	0.3~13A	1~50A
Output Voltage Tolerance	±5%	±2%

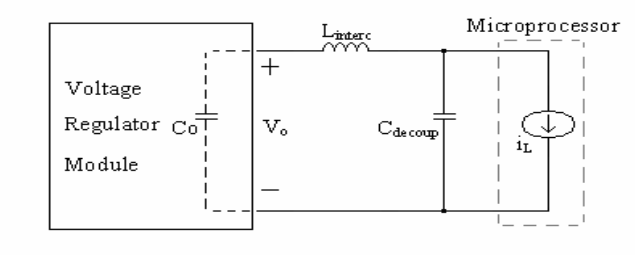


Fig. 1: Microprocessor power system structure

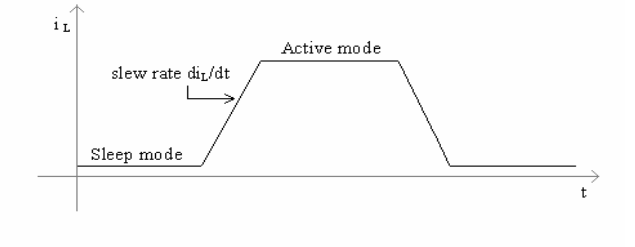


Fig. 2: Load waveform during transients

the Phase-shift Buck (PSB) converter and the ZVS self-driven 12-V voltage regulator along with their performance comparison. Section II, III and IV respectively discusses in detail the principle of operation of the three 12-V VRM topologies along with their simulation results. Finally, section V and VI respectively contains the comparison of these three 12V VRM topologies for future microprocessors and the conclusion. The best VRM topology with high efficiency and fast transient response is identified. The main aim is to maintain the output voltage of the VRM at desired constant voltage (1.5V) when the load varies from no-load (1A) to full-load (50A) and vice versa.

II. INTERLEAVED QUASI-SQUARE-WAVE TOPOLOGY

Fig. 3 shows the Quasi-Square-Wave (QSW) circuit and the operating principle of QSW topology is presented in Fig. 4 [1]. When Q1 turns on, the input voltage charges the inductor current from negative to positive. After Q1 turns off, and before Q2 turns on, the inductor current flows through Q2's body diode. Then Q2 can turn on at zero voltage. After Q2 turns on, the inductor current is discharged to negative. After Q2 turns off, and before Q1 turns on, the inductor current flows through the Q1 body diode. Then Q1 can turn on at zero voltage. In the QSW topology, both the top switch and bottom switch can turn on at zero voltage.

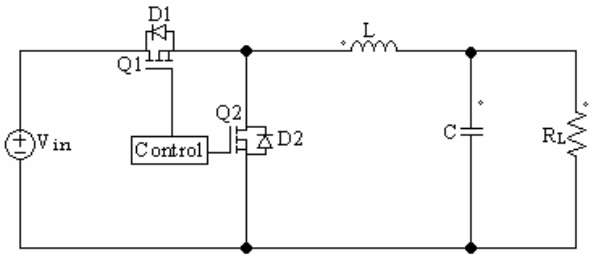


Fig. 3: Quasi-Square-Wave (QSW) topology

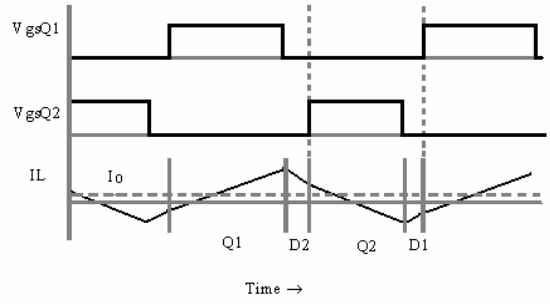


Fig. 4: Operating principle of QSW topology

The QSW topology keeps the VRM output inductor current peak to peak value is two times the full load current, which makes the inductor current go negative in all load ranges. Its inductor design is according to:

$$L = \frac{(V_{in} - V_o) \times D}{2 \times I_o \times f_s} \quad (1)$$

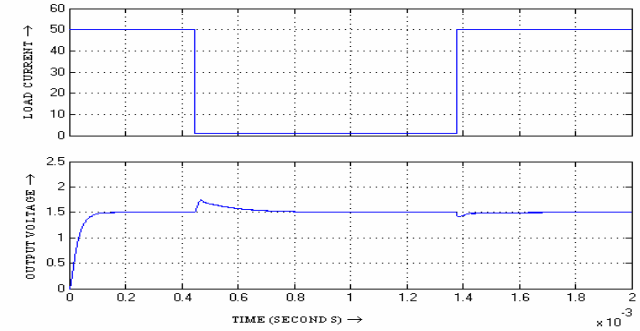


Fig. 5: Simulation results of QSW topology

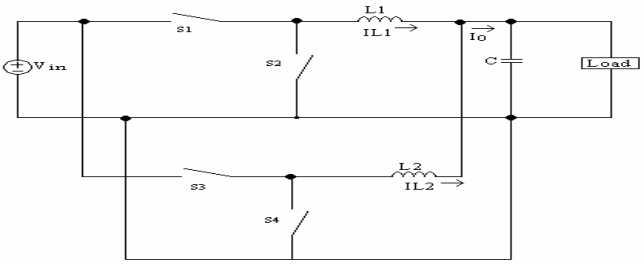


Fig. 6: Interleaved QSW topology

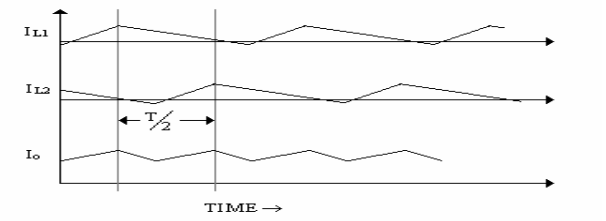


Fig. 7: Current ripple canceling effect of interleaved QSW

Fig. 5 shows the simulation results of the QSW topology at 50 A load and 1 MHz switching frequency using PSIM software. In order to meet both the steady state and transient requirements, interleaved QSW VRM topology is presented in Fig 6. The interleaved QSW topology naturally cancels the output current ripple and still maintains the fast transient response characteristics of the QSW topology as shown in Fig. 7. Generally, the interleaving technique is implemented by paralleling a number of converter cells (phases), and by phase-shifting (interleaving) their drive signals [3]. In this work 2 converter are parallel and interleaved in their driving pulses. The main benefit of interleaving is the decreased magnitude and the increased frequency of the output voltage ripple; the latter is equal to the product of the single-phase switching frequency and the number of the interleaved phases. Fig. 8 shows the simulation results of the interleaved QSW topology. From the simulation results, it is clear that the interleaved QSW topology gives the better performance than the QSW topology and the output voltage is maintained constant at 1.5V, for a variation in load current from no-load (1A) to full-load (50A).

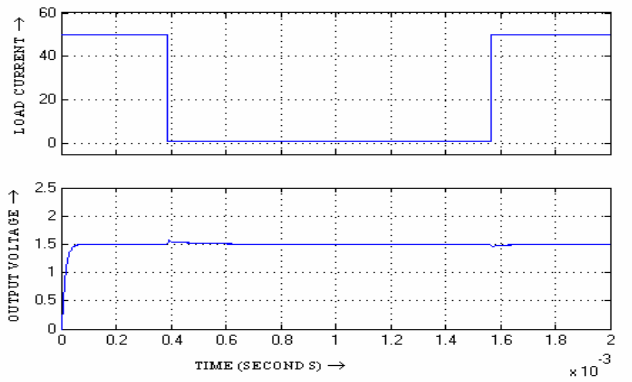


Fig. 8: Simulation results of the interleaved QSW topology

III. Phase-Shift Buck Converter Topology

Due to the very low output voltage, the duty cycle is very narrow, and is predicted to be smaller than 0.1 in the future. This extreme duty cycle impairs the VR's efficiency and imposes obstacles for the transient response. Also, control-wise, to generate the very narrow duty cycle, the control IC must incorporate a very fast comparator, which may cause some cost increase. The PSB converter applies the transformer concept to this non-isolated application; therefore, the extreme duty cycle is extended and many benefits are gained. PSB converters can also achieve ZVS turn-on of the top switch, which enables them to achieve high efficiency at high switching frequencies and high current [4]. The proposed phase-shift buck (PSB) converter is shown in Fig. 9. The PSB converter can be controlled in a traditional PWM fashion or a phase-shifted fashion. The traditional PWM control leads to hard switching of the top switches *Q1~Q4*, while phase-shift control allows soft switching of *Q1~Q4*, which is desirable at high switching frequency. The voltage conversion gain of the phase-shifted buck converter is given by equation 2 [4]

$$\frac{V_o}{V_{in}} = \frac{D}{(n+1)} \quad (2)$$

Through the choice of n, a more desirable duty cycle can be obtained. For example, V_{in}=12V and V_o=1.5V, D is 0.25 when n=1. This duty cycle is twice that of a buck converter. The operating principle of PSB converter is shown in Fig. 10.

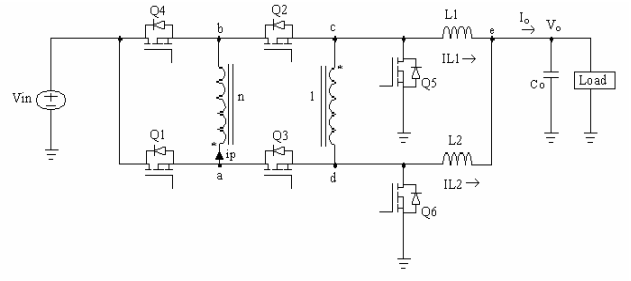


Fig. 9: The proposed phase-shift buck converter

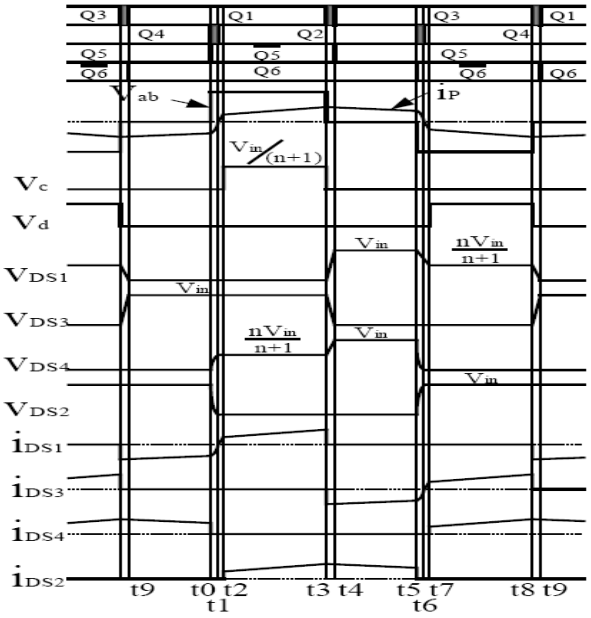
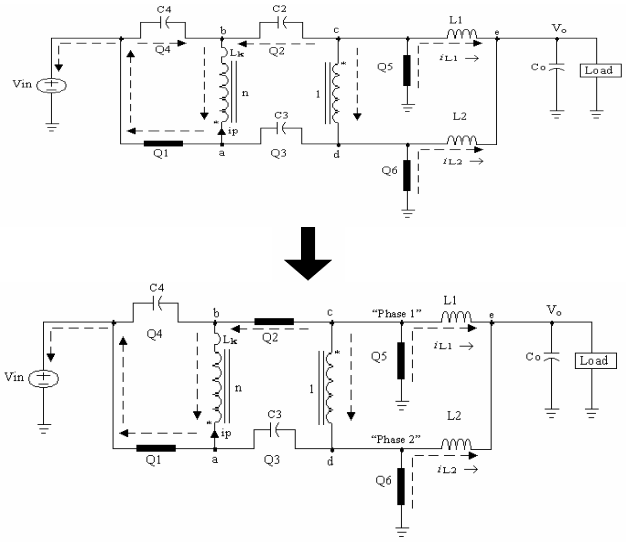
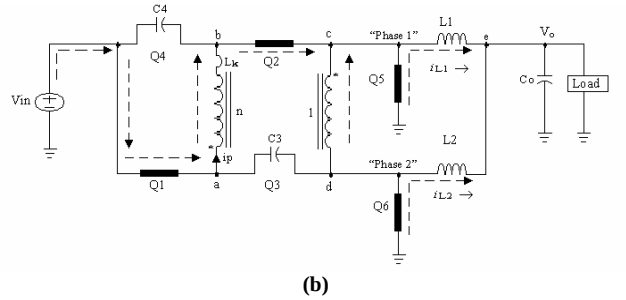


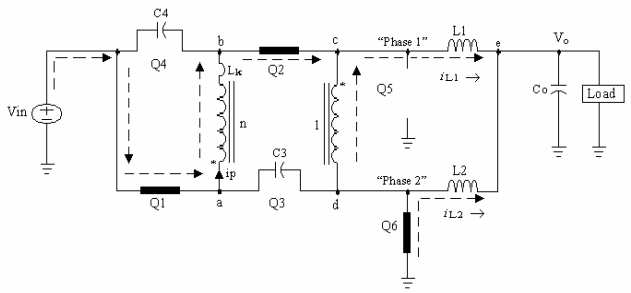
Fig. 10: The operating principle of PSB converter



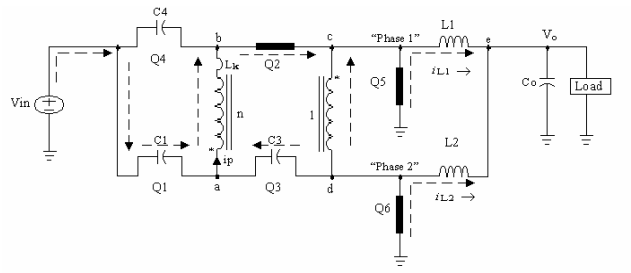
(a)



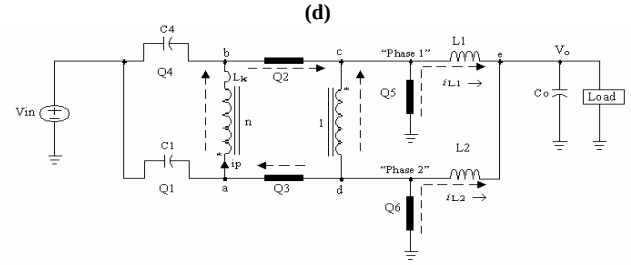
(b)



(c)



(d)



(e)

Fig. 11: Subintervals of the Circuit Operation: (a) t_0~t_1 (b) t_1~t_2 (c) t_2~t_3 (d) t_3~t_4 (e) t_4~t_5

Fig. 11(a) shows the subinterval t_0~t_1. Before t_0 the circuit is in the freewheeling mode and the transformer is shorted. The primary current i_p is flowing from node "b" to "a". At t_0, *Q4* is turned off. However, i_p continues flowing due to the existence of *Lk*, therefore *C2* is discharged and *C4* is charged in a fashion determined by the *L-C* resonance formed by *Lk* and the parallel of *C2* and *C4*. Given sufficient energy stored in *Lk*, *C2* can be fully discharged, after which i_p flows through the body diode of *Q2*. Fig. 11(b) shows the subinterval t_1~t_2. At t_1, *Q2* is turned on. Because i_p is flowing through the body diode of *Q2*, *Q2* is turned on at zero-voltage condition, which eliminates the turn-on loss. In the meantime, *Q5*and *Q6* are still carrying current for freewheeling, which means the transformer is still shorted. Thus the voltage across nodes "a" and "b" is applied to *Lk* and builds up i_p in the direction from "a" to "b". As a result, the current through *Q5* decreases until at t_2 it reaches zero. Fig. 11(c) shows the subinterval t_2~t_3. This is a power transfer mode. The transformer acts as an autotransformer and L_1 is being charged while L_2 is being discharged. The transformer primary current i_p is flowing from node "a" to "b". Fig. 11(d) shows the subinterval t_3~t_4. At t_3, *Q1* is turned off, but the transformer primary current i_p continues flowing from node "a" to "b". Because i_p is the reflected output inductor current, *C3* is discharged and *C1* is charged linearly until at t4 when *C3* is fully discharged so i_p flows through the body diode of *Q3*. Fig. 11(e) shows the subinterval t_4~t_5. This is a freewheeling mode. Switches *Q2*, *Q3*, *Q5* and *Q6* are on so the transformer is shorted. From t_5~t_0, another half-period starts, and the operation principle is the same except for polarity changes as shown in Fig. 11 and Fig. 12.

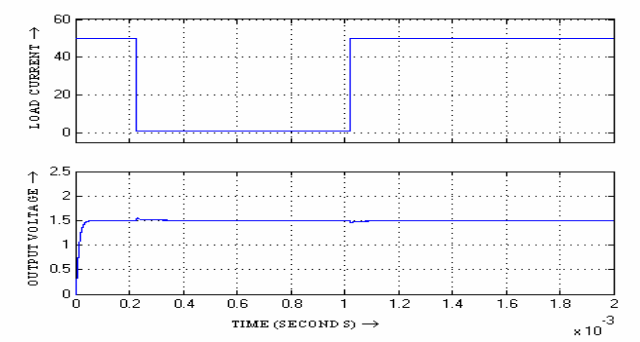


Fig. 12: Simulation results of the phase-shift buck converter

From the simulation results shown in Fig. 12, it is clear that the phase-shift buck converter topology gives better transient response than the interleaved QSW topology.

IV. ZVS SELF-DRIVEN 12-V VR TOPOLOGY

The concept of synchronous rectifier devices being self-driven was widely used in isolated topologies, where the voltage across the secondary winding can be used as the gate driving source for the rectifiers [5]-[10]. The main benefit of self-driven synchronous rectifier devices is that the driving circuitry is simplified, and partial driving energy can be recycled which results in a low-cost, high-efficiency solution. The self-driven topology is basically a buck-derived multiphase interleaving soft switching topology, which can use self-driven technology easily, save driving loss and achieve zero voltage switching (ZVS). The self-driven topology is shown in Fig. 13. In order to achieve ZVS and also to find suitable voltage waveforms in the power stage to drive the synchronous rectifier MOSFETs, a complementary control strategy for *Q1* ~ *Q4* is used. The switch timing diagram for the switches *Q1* ~ *Q4* and secondary synchronous rectifier switches *Q5* ~ *Q6* are shown in Fig. 14. The operation modes of the proposed circuit are shown in Fig. 15. The on time of *Q1* is complementary to that of *Q3*, with a fixed dead time to achieve ZVS as shown in Fig. 14. The same is true of the switches *Q2* and *Q4*. Here, the output voltage is regulated by control of the duty cycle of *Q2* and *Q3*. The larger the duty cycle is, the higher the output voltage will be.

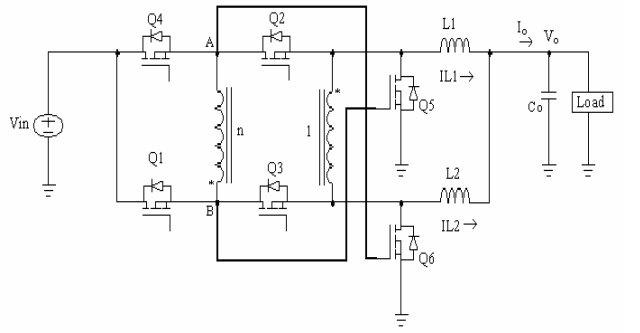


Fig. 13: ZVS self-driven 12-V Voltage Regulator

Based on the switch-timing diagram, there are eight operating modes during one switching cycle. Fig. 14 illustrates the equivalent circuits for Mode1 to Mode 4. During the other half of the switching cycle, the circuit operates in the same way as in Mode1 to Mode 4.

A. *Mode 1 [T_0 ~ T_1]*

Q1 and *Q2* are on. The voltage at point B is actually the input voltage, which is 12 V. Because point B is directly connected to the gate of *Q5*, *Q5* is self-driven to be on. On the other hand, since *Q2* and *Q5* are both on, point A is connected to the ground which automatically keeps *Q6* off during this operating mode. The energy is transferred from the input to the output through the transformer.

B. *Mode 2 [T_1 ~ T_2]*

Q2 turns off at T_1, and the reflected output current discharges and charges the output capacitor of *Q4* and *Q2*, respectively. Meanwhile, because *Q5* stays on during this interval, the drain-to-source voltage of *Q4* will drop to zero so that *Q4* can be turned on under ZVS. Where n_p is the transformer turn's ratio; C_{eq} is the sum of the output capacitance of *Q2* and *Q4* plus the gate-to-source capacitance of *Q6*; V_{in} is the input voltage; $I_{o\text{-}min}$ is the minimum load current at which the ZVS can still be achieved. The gate capacitor of *Q6* serves as a lossless snubber of *Q2*.

C. *Mode 3 [T_2 ~ T_3]*

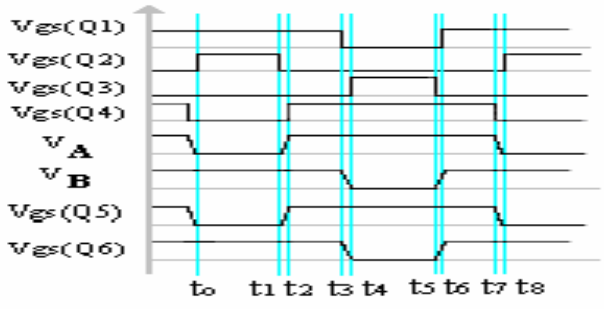
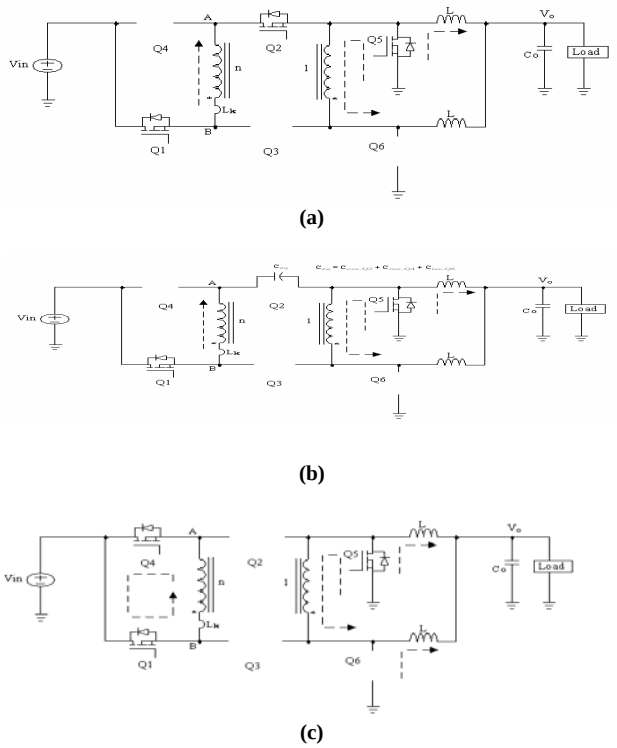
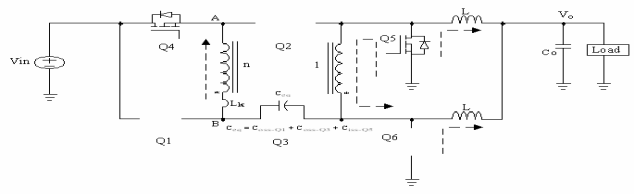


Fig. 14: Control strategy of ZVS self-driven 12-V VR





(d)

Fig. 15: Operation modes of the ZVS self driven 12-V VR: (a) Mode 1 [$T_0 \sim T_1$] (b) Mode 2 [$T_1 \sim T_2$] (c) Mode 3 [$T_2 \sim T_3$] (d) Mode 4 [$T_3 \sim T_4$]

The energy stored in the transformer leakage inductor freewheels through *Q1* and *Q4*. Since both point A and point B are connected to the input, *Q5* and *Q6* are on during this mode, which provide the current freewheeling paths for the synchronous rectifier.

D. Mode 4 [$T_3 \sim T_4$]

Q1 turns off at T_3. The leakage inductor of the transformer resonates with the output capacitors of *Q1* and *Q3*, and similarly, the gate capacitor of Q5 joins the resonance because it is in fact in parallel the output capacitor of *Q3*. In order to achieve ZVS for *Q3*, two conditions are necessary: one is the appropriate dead time between Q1 and *Q3*, which is one-fourth of the self-resonant period; the other condition is that the energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output capacitances as well as the gate capacitance of *Q5*. These two conditions can be expressed as

$$T_{d2} = \frac{\pi\sqrt{L_k C_{eq}}}{2} \tag{3}$$

$$I_{o-\min} = \frac{2n_p C_{eq} V_{in}^2}{L_k} \tag{4}$$

where L_k is the leakage inductance of the transformer reflected to the primary side; $I_{o\text{-}min}$ is the minimum output current needed to achieve ZVS. From *T4* to *T8*, another half-period starts, and the operation principle is the same except for polarity changes. It should be noted that not only can the proposed circuit achieve ZVS, but also the voltage waveform at point A and B are exactly those desired to drive the synchronous rectifier MOSFETs. Simulated waveforms of the output voltage and the load current are shown in Fig. 16. A self-driven dc/dc converter for non isolated 12V VR is proposed [11]-[17]. ZVS of all the MOSFETs is achieved to reduce the switching loss. By adding a transformer, the proposed topology extends its duty cycle so that the switching loss is further reduced. This innovative self-driven concept eliminates the need for synchronous rectifier drivers which saves cost [18]-[21].

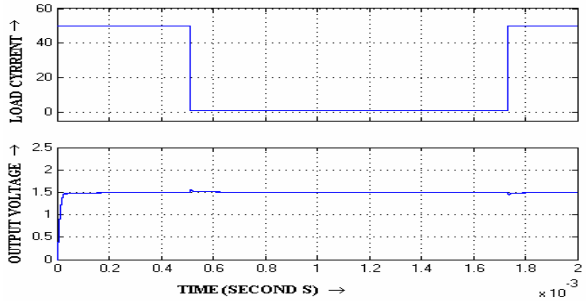


Fig. 16: Simulated waveforms of the output voltage and the load current

Table 2: Comparison of the three VRM topologies at 1MHz

Name of the VRM topology	Efficiency	Settling time
Interleaved Quasi-Square topology	75.3%	30µs
Phase-Shift Buck topology	82.9%	16µs
ZVS self-driven 12-V VR topology	88.1%	14µs

The power circuit of ZVS self-driven 12-V VR topology is shown in Fig. 17. The feedback (F.B.) is taken at the voltage divider circuit at the output side. The firing pulses for the MOSFET are generated using circuit shown in Fig. 18. A pulse width modulator 3525 is used to generate two PWM pulses. By varying the resistance at point2 of 3525, we set the reference point.

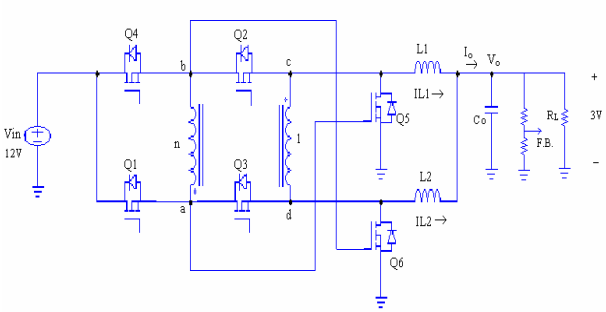


Fig. 17: Power circuit of ZVS self-driven 12-V VR topology

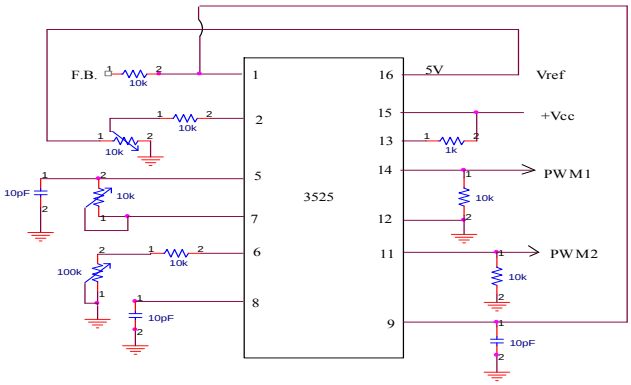


Fig. 18: Pulse generation circuit

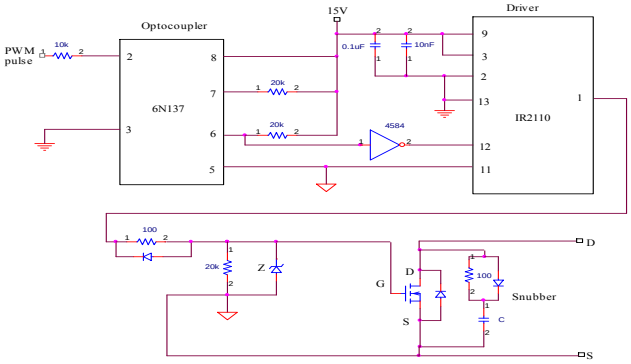


Fig. 19: Opto-coupler and driver circuit

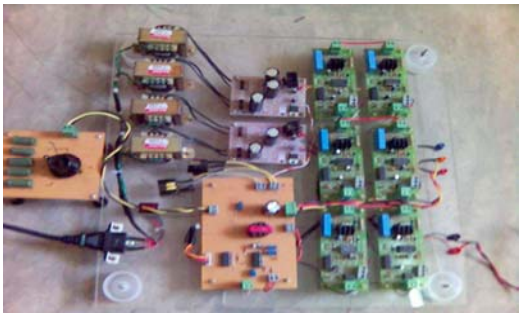


Fig. 20: Hardware of ZVS self-driven 12-V VR topology

V. Design and Implementation of ZVS Self-Driven 12V VR Topology

By adjusting the resistance between point5 and point7 of 3525, we get the requisite dead time. We attain the required frequency by adjusting the variable resistor of 100k connected at point 6 of 3525. The optocoupler is used for the isolation purpose. The PWM pulse coming from 3525 is given to point 2 of the optocoupler 6N137 as shown in Fig. 19. The output waveform of the optocoupler is the inverted version of the applied waveform. To get original waveform, we are using a NOT gate 4584. The driver IR2110 is utilized to get the original PWM pulse with required current limit. The output pulse from the IR2110 is used to drive the gate of the mosfet. The mosfets used are IRF840 (manufactured by (IRF) International Rectifier Company). The positive regulator IC used is 7815. Inductance = 100µH and Capacitance = 5µF are used for the simulation and hardware analysis. The hardware version of the ZVS self-driven 12-V VR topology is shown in Fig. 20. The hardware results are shown in the Fig. 21 to Fig. 26. The specifications followed to get these results are input voltage of 12V, output voltage of 3V, full load current of 2A and switching frequency of 25 kHz.

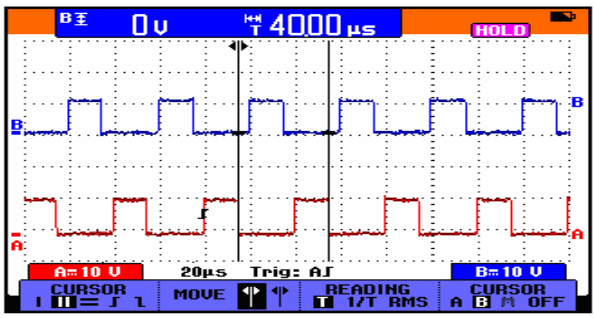


Fig. 21: Firing pulses for mosfets Q1:Ch.A and Q4:Ch.B [(10V/div)(timebase:20*us*/div)]

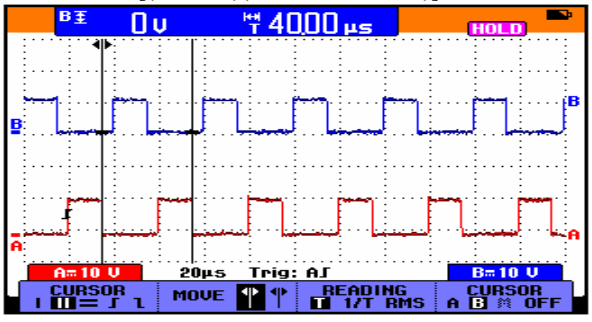


Fig. 22: Firing pulses for mosfets Q3:Ch.A and Q2:Ch.B [(10V/div)(timebase:20us/div)]

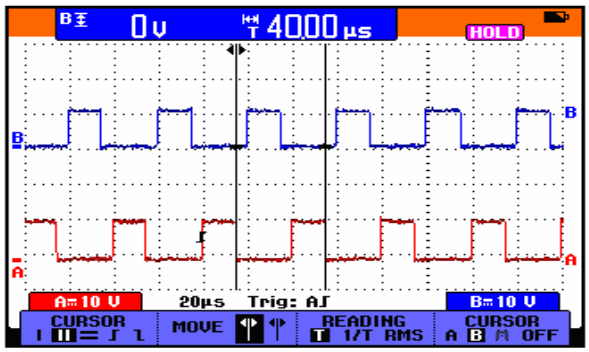


Fig. 23: Firing pulses for mosfets Q6:Ch.A and Q5:Ch.B [(10V/div)(timebase:20us/div)]

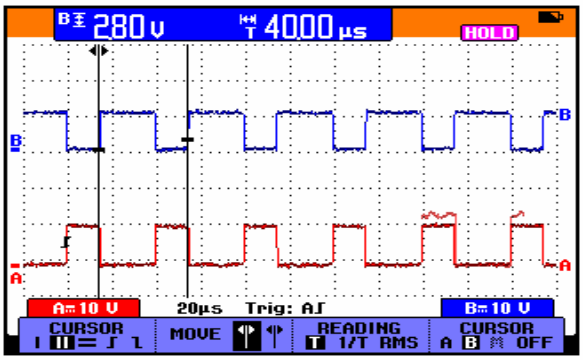


Fig. 24: Optocoupler input: Ch.A and output: Ch.B [(10V/div)(timebase:20us/div)]

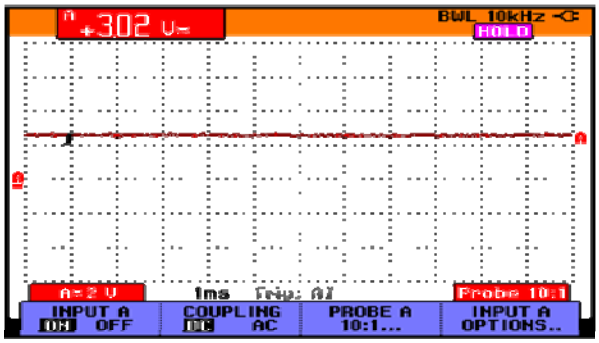


Fig. 25: Output voltage at no-load [(2V/div)(timebase:1ms/div)]

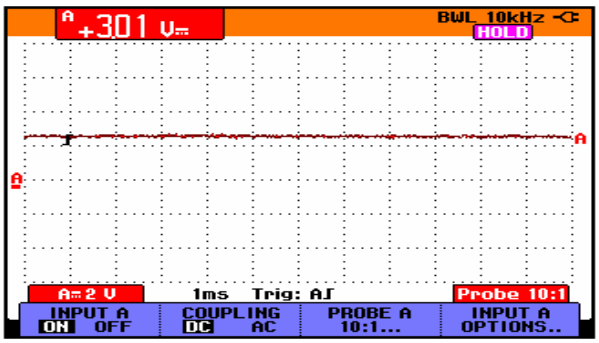


Fig. 26: Output voltage at full-load [(2V/div)(timebase:1ms/div)]

VI. Hardware Results

Fig. 21, Fig. 22 and Fig. 23 show the hardware results of the firing pulses for the mosfets Q1 and Q4, Q3 and Q2 and Q6 and Q5 respectively. Fig. 24 shows the Optocoupler input and output. Fig. 25 and Fig. 26 show the output voltage at no-load and full-load respectively.

VII. Comparison Of The Simulation Results And The Hardware Results

The simulation results and the hardware results are compared as shown in Table 3. The output voltage in volts at no-load, 25%, 50%, 75% and 100% of the full-load are presented here. The %error between the hardware results and the simulation results is calculated and is given in the table.

Table 3: Comparison of the simulation results and the hardware results

% of full-load	Hardware Results: Output voltage in volts	Simulation results: Output voltage in volts	% error
No-load	3.02	3.0	0.66
25%	3.02	3.0	0.66
50%	3.01	3.0	0.33
75%	3.01	3.0	0.33
100%	3.01	3.0	0.33

VIII. Conclusion

The simulation models for the three different VRM topologies for future microprocessors are developed. The performance of the three VRM topologies is studied through simulation. It is observed from the simulation results that the ZVS self-driven 12-V voltage regulator topology offers better performance in terms of efficiency and settling time. The topology is implemented in hardware. It is found that the output voltage is maintained constant at desired voltage level (3V) irrespective of the variations in load from no-load to full-load value, thus validating the simulation results.

References

[1] X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen , H.P. Wu, L. Amoroso, F.C. Lee, and D. Chen, "Investigation of candidate VRM topologies for future microprocessors", IEEE APEC'98, 1998, pp. 145-150.

[2] M. Zhang, M. Jovanovic, and F.C. Lee, "Design considerations for low voltage on-board DC/DC modules for next generations of data processing circuits", IEEE Transactions of Power Electronics, 1996, pp. 328–337.

[3] Y. Panov and M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules", IEEE APEC'00, 2000, pp. 39-46.

[4] J. Wei and F.C. Lee, "A novel soft-switched, high-frequency, high-efficiency, high-current 12 V voltage regulator - the phase-shift buck converter", IEEE APEC'03, 2003, pp. 724-730.

[5] J. Zhou, M. Xu, J. Sun and F.C. Lee, "A Self-Driven Soft-Switching Voltage Regulator for Future Microprocessors", IEEE Transactions on Power Electronics, Vol. 20, No. 4, 2005, pp. 806-814.

[6] P. Alou, J. A. Cobos , O. Garcia, R. Prieto, and J. Uceda, "A new driving scheme for synchronous rectifiers: Single winding self-driven synchronous rectification", IEEE Transactions of Power Electronics, Vol. 16, No. 6, November 2001, pp. 803-811.

[7] W. Chen, G. Hua, D. Sable and F. C. Lee, "Design of High Efficiency, Low Profile, Low Voltage Converter with Integrated Magnetics", IEEE APEC'97, 1997, pp. 911-917.

[8] A.Q. Huang, N.X. Sun, B. Zhang, X. Zhou, and F.C Lee., "Low voltage power devices for future VRM", ISPSDIC '98, 1998, pp. 395-398.

[9] Y. Ren, M. Xu, D. Sterk, and F. C. Lee, "1 MHz self-driven ZVS full bridge converter for 48 V power pods", IEEE PESC'03, 2003, pp. 1801-1806.

[10] A. Rozman and K. Fellhoelter, "Circuit Considerations for Fast Sensitive, Low-voltage Loads in a Distributed Power System", IEEE APEC'95, 1995, pp. 34-42.

[11] J. Wei, "Investigation of high-input-voltage non-isolated voltage regulator module topology candidates", M.S. thesis, Virginia Tech, Blacksburg, 2002.

[12] J. Wei, P. Xu, H. Wu, F. C. Lee, K. Yao, and M Ye., "Comparison of three topology candidates for 12 V VRM", IEEE APEC'01, 2001, pp. 245-251.

[13] J. Wei, P. Xu, and F. C. Lee, "A high efficiency topology for 12 V VRM push-pull buck and its integrated magnetics implementations", IEEE APEC'02, 2002, pp. 679–685.

[14] P. Wong, F.C Lee., P. Xu and K. Yao, "Critical inductance in voltage regulator modules', IEEE APEC'02, 2002, pp. 203-209.

[15] P. Wong, Q. Wu, P. Xu, B. Yang and F. C. Lee, "Investigating coupling inductors in the interleaving QSW VRM", IEEE APEC'00, 2000, pp. 973-978.

[16] P. Wong, X**.** Zhou, J. Chen, H. Wu, F.C. Lee, and D. Y. Chen, "VRM Transient Study and Output Filter Design for Future Processors", IEEE APEC'97, 1997, pp. 410-415.

[17] P. Xu, J. Wei and F. C. Lee, "The Active-Clamp Couple-Buck Converter - A Novel High Efficiency Voltage Regulator Modules", IEEE APEC'01, 2001, pp. 252-257.

[18] X.Zhou, X. Peng and F.C. Lee, "A high power density, high efficiency and fast transient voltage regulator module with a novel current sensing and current sharing technique", IEEE APEC'99, 1991, pp. 289-294.

[19] www.nationalsemiconductor.com.

[20] X. Zhou, X. Peng and F.C. Lee, "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications", IEEE Transactions on Power Electronics, Vol. 15, No. 6, November 2000, pp. 1153-1162.

[21] X. Zhou, B. Yang, L. Amoroso, F.C. Lee and P. Wong, "A novel high-input-voltage, high efficiency, and fast transient voltage regulator module - Push-pull forward converter", IEEE APEC'99, 1999, pp. 279-283.

Biographies

K.Rajambal received her Bachelor of Engineering in Electrical & Electronics, Master of Engineering in power electronics and Ph.D in Wind Energy Systems in 1991, 1993 and 2005 respectively from Anna University, Chennai, India. She is working as a Assistant professor in the Department of Electrical and Electronics in Pondicherry Engineering College, Pondicherry, India. Her area of interest includes in the fields of Wind Energy systems and Photovoltaic Cell, Power Converter such as DC-DC Converters, AC-AC Converters and Multilevel Inverters with soft switching PWM schemes and power electronics application towards power systems. She has published papers in national, international conferences and journals in the field of non renewable energy sources and power electronics.

P.Sanjeevikumar received Bachelor of Engineering (Electrical & Electronics) from the University of Madras and Master of Technology (Electrical Drives & Control) from Pondicherry University in 2002, 2006. He worked as a Lecturer in the Department of Electrical & Electronics Engineering in IFET College of Engineering, Tamilnadu, India (2002 – 2007). He also worked as Manager Training at Edutech LLC, Dubai, Middle East, UAE. He his with the Department of Electrical, University of Bologna, Italy. His area of interest includes alternate topology for Matrix converter, Luo converters, soft switching PWM schemes and power electronics application towards power systems. He has published papers in national, international conferences and journals in the field of power electronics.