Performance Evaluation of Three Single Phase Voltage Source Inverter Based Configuration of DSTATCOM

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Abstract – This paper deals with the detailed modeling and simulation of a three-phase four-wire Distribution Static Compensator (DSTATCOM) used as a shunt compensator. This DSTATCOM configuration consists of three single-phase voltage source inverter (VSI) bridges having a common dc link. The model is developed using MATLAB/ Simulink and tested for a variety of linear as well as non-linear loads. The ability of this compensator is demonstrated in improving various facets of power quality viz. power factor correction, voltage regulation and harmonic reduction. Comparisons with existing and well known DSTATCOM configurations are made and analyzed in detail.

Keywords – DSTATCOM, power quality, voltage regulation, harmonic reduction

I. INTRODUCTION

There has been a rapid rise in the development of power electronic based compensators. This has led to the development of FACTS as well as custom power devices for transmission as well as distribution systems [1-3]. Power quality issues have been a major concern for power engineers worldwide [4-8]. As a result, development of custom power devices is increasing for load compensation in distribution systems [9-13]. DSTATCOM is a popular shunt compensator having the ability to provide reactive power compensation. Both three-phase and single-phase DSTATCOMs can be designed for compensation of different load configuration. One of the most commonly used configurations of DSTATCOM is the three-leg VSI based configuration for three-phase, three-wire system. A three-phase, four-wire system also has an additional conductor. In the presence of neutral conductor, possible DSTATCOM configurations are four-leg VSI or a three-single phase VSI. This paper deals with the modeling and simulation of a three-single phase VSIs based DSTATCOM which has a number of advantages over its four-leg VSI counterpart. Each single–phase VSI has lower kVA rating and the cost of components such as DC capacitor, Insulated Gate Bipolar Transistor (IGBT) switches having low voltage and the current rating can also be effectively reduced. Moreover, modular approach involving three single-phase VSIs gives better flexibility and enhanced control.

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II. STYLE INFORMATION

The DSTATCOM system configuration considered here consists of a three-phase, four-wire ac source feeding a variety of loads. A three-phase, four-wire ac source with supply impedance (L_s, R_s) feeds power to balanced/unbalanced linear/non-linear loads. Fig. 1 shows the basic diagram of DSTATCOM connected as shunt compensator to the distribution system via three single phase transformers. The DSTATCOM configuration considered here consists of three independent single-phase voltage source inverters having a common dc bus. Three-VSI bridges are connected together at the dc link at which a dc bus capacitor (C_{dc}) provides a self-supporting dc bus. This scheme requires three single-phase transformers or a three-phase transformer with access to individual windings. The control scheme consists of providing gating pulses to the three VSI bridges. The control algorithm is suitably modified to improve various power quality features. Another advantage of this DSTATCOM configuration is that the current in neutral wire is controlled to zero value.

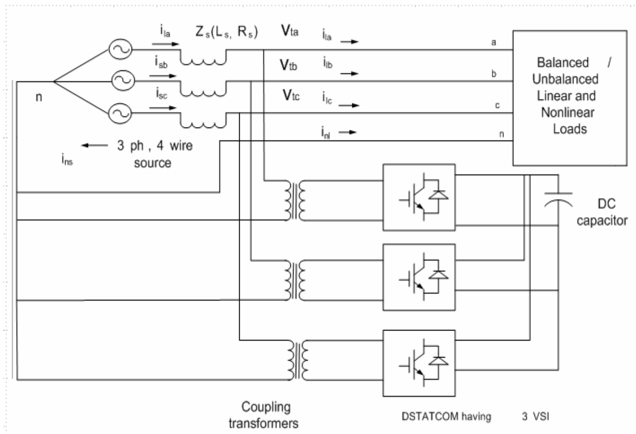

Fig. 1: Schematic diagram of DSTATCOM (3 VSI configuration) connected to a three-phase, four-wire distribution system.

III. PROBLEMS ASSOCIATED WITH NEUTRAL CURRENT

In three-phase, four-wire system, the current in the neutral conductor is the sum of three line currents. If the system is perfectly balanced, the neutral current is zero. However, practical distribution system is never perfectly balanced and the neutral current mitigation always becomes an important issue for power system engineers [7, 11-13]. The main cause of neutral conductor current is load unbalancing and presence of non-linear loads. Moreover, under certain conditions, even perfectly balanced single-phase loads could result in significant neutral currents. The presence of non-linear loads having non-sinusoidal current in nature adds up to neutral current magnitude. The triplen current harmonics are in phase with each other for three-phase-circuits and it results in net rise of neutral current. Recent advances in power electronics technology have led to a tremendous increase in loads such as computers, air conditioning equipment, florescent lights with electronic ballasts, office equipment etc. The configuration of DSTATCOM considered in this work is able to reduce neutral current in the neutral conductor to negligible amount even when there is appreciable current in the load neutral conductor due to load unbalancing and harmonics currents.

IV. CONTROL OF DSTATCOM

The most commonly used control techniques involve instantaneous reactive power theory (p-q theory), synchronous reference frame theory, indirect current control theory etc. The current control algorithm employing hysteresis rule based carrier-less PWM current control is effective and simple [12-13]. To realize this, a current controlled voltage source inverter is used as a DSTATCOM. One Proportional Integral (PI) controller is used to regulate the dc link voltage and helps to improve power-factor to unity. Two PI controllers are needed to regulate terminal voltage at PCC. The generation of reference supply currents involves computation of two components as:

A. Computation of In-Phase Components of Reference Supply Currents

The amplitude of in-phase component of reference supply currents (I_{spdr}) is computed using PI controller over the average value of dc bus voltage of the DSTATCOM (v_{dc}) and reference dc voltage (v_{dcr}) as:

$$I_{spdr(n)} = I_{spdr(n-1)} + K_{pd}\{v_{de(n)} - v_{de(n-1)}\} + K_{id}\, v_{de(n)} \qquad (1)$$

where $v_{de(n)} = v_{dcr} - v_{dca(n)}$ denotes the error in v_{dc} calculated over reference v_{dcr} and average value of v_{dc} at the nth sampling instant. K_{pd} and K_{id} are proportional and integral gains of the dc bus voltage PI controller. The in-phase components of the reference supply currents (i_{sadr}, i_{sbdr}, i_{scdr}) are computed using the in-phase unit current templates (u_a, u_b, u_c) derived from the filtered ac terminal voltages at PCC (v_{ta}, v_{tb}, v_{tc}) as:

$$u_a = v_{ta} / V_{tm} \qquad (2)$$

$$u_b = v_{tb} / V_t \qquad (3)$$

$$u_c = v_{tc} / V_{tm} \qquad (4)$$

where V_{tm} is amplitude of the supply voltage and it is computed as:

$$V_{tm} = \{2/3(v_{ta}^2 + v_{tb}^2 + v_{tc}^2)\}^{1/2} \qquad (5)$$

The computation of in-phase components of reference supply currents is carried out as:

$$i_{sadr} = I_{spdr}\, u_a \qquad (6)$$

$$i_{sbdr} = I_{spdr}\, u_b \qquad (7)$$

$$i_{scdr} = I_{spdr}\, u_c \qquad (8)$$

B. Computation of Quadrature Components of Reference Supply Currents

The amplitude of quadrature component of reference supply currents (I_{spqr}) is computed using another PI controller over the amplitude of supply voltage (V_{tm}) and its reference (V_{tmr}).

$$I_{spqr(n)} = I_{spqr(n-1)} + K_{pq}\{v_{ae(n)} - v_{ae(n-1)}\} + K_{iq}\, v_{ae(n)} \qquad (9)$$

where $v_{ae(n)} = V_{tmr} - V_{tm(n)}$ denotes the error calculated over reference V_{tmr} and V_{tm} estimated using eq(5) and K_{pq} and K_{iq} are the proportional and integral gains of the second PI controller. The quadrature unit current templates (w_a, w_b, w_c) are derived from in-phase unit current templates (u_a, u_b, u_c). Three-phase quadrature components of the reference supply currents (i_{saqr}, i_{sbqr}, i_{scqr}) are computed using the output of second PI controller (I_{spqr}) and quadrature unit current vectors as:

$$i_{saqr} = I_{spqr}\, w_a \qquad (10)$$

$$i_{sbqr} = I_{spqr}\, w \qquad (11)$$

$$i_{scqr} = I_{spqr}\, w_c \qquad (12)$$

C. Computation of Reference Supply Currents

Three-phase reference supply currents (i_{sar}, i_{sbr}, i_{scr}) are computed by adding in-phase (i_{sadr}, i_{sbdr}, i_{scdr}) and quadrature components of supply currents (i_{saqr}, i_{sbqr}, i_{scqr}) as:

$$i_{sar} = i_{sadr} + i_{saqr} \qquad (13)$$

$$i_{sbr} = i_{sbdr} + i_{sbqr} \qquad (14)$$

$$i_{scr} = i_{scdr} + i_{scqr} \qquad (15)$$

Hysteresis PWM current controller is employed over the reference supply current ($i_{sar,}$ $i_{sbr,}$ $i_{scr,}$) and sensed supply currents (i_{sa}, $i_{sb,}$ i_{sb}) to generate 12 gating pulses for the IGBTs of the single phase VSI bridge. Three such VSI bridges (connected for all the three phases) are suitably controlled using hysteresis current controller. Thus, a total of 12 gating pulses (4 per VSI) are generated simultaneously (Fig. 2).

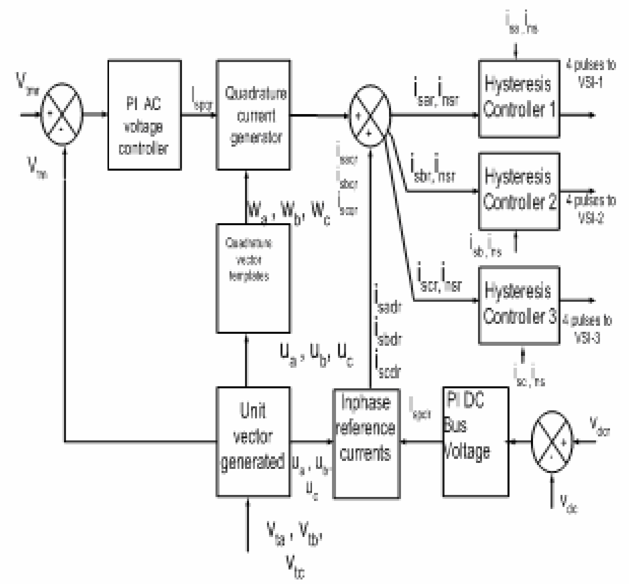

Fig. 2: Control scheme for three-VSI.

V. MATHEMATICAL MODELING OF SYSTEM COMPONENTS

This section discusses the modeling of supply system, DSTATCOM and linear as well as nonlinear loads.

A. Modeling of Three-Phase, Three-Wire AC System with DSTATCOM

The modeling of the supply can be given in terms of three volt-ampere equations as:

$$v_{sa} = i_{sa}R_s + L_s p i_{sa} + n\, v_{ta} \qquad (16)$$

$$v_{sb}= i_{sb}R_s + L_s pi_{sb} + n\, v_{tb} \quad (17)$$
$$v_{sc}= i_{sc}R_s + L_s pi_{sc} + n\, v_{tc} \quad (18)$$

where p denotes the time differential operator (d/dt). v_{sa}, v_{sb} and v_{sc} are the three-phase supply voltages. v_{ta}, v_{tb} and v_{tc} are the three-phase voltages at point of common coupling (PCC),n is the turns ratio of the transformer. i_{sa}, i_{sb}, i_{sc} are three-phase supply currents, R_s and L_s are the supply resistance and inductance parameters.

B. Modeling of DSTATCOM

The DSTATCOM configuration with three-single phase VSIs is connected in shunt configuration to the system. Each single phase VSI has two legs and it is connected to each phase and neutral. The dc link of three VSIs is held in common by a single dc bus capacitor as represented in Fig. 3. The control of each VSI is independent. The model equations for three-legged DSTATCOM can be written as:

$$v_{ta}= i_{ca}R_c + L_c pi_{ca} + v_{ca} \quad (19)$$
$$v_{tb}= i_{cb}R_c + L_c pi_{cb} + v_{cb} \quad (20)$$
$$v_{tc}= i_{cc}R_c + L_c pi_{cc} + v_{cc} \quad (21)$$

where v_{ta}, v_{tb} and v_{tc} are the three-phase ac voltages at the PCC, i_{ca}, i_{cb}, i_{cc} are the DSTATCOM currents, R_c and L_c are the DSTATCOM resistance and inductance parameters. The first order differential equation for DC link voltage (v_{dc}) can be written as:

$$pv_{dc}= (i_{cad} + i_{cbd} + i_{ccd}) / C_{dc} \quad (22)$$

where v_{dc} denotes the DC link voltage at the DSTATCOM terminals and SA_1, SA_2, SB_1, SB_2, SC_1, SC_2 are the switching functions decided by switching logic of the three phases of DSTATCOM. The three-phase ac voltages at the terminals of DSTATCOM (v_{ca}, v_{cb} and v_{cc}) are calculated as:

$$v_{ca} =(SA_1 - SA_2)\, v_{dc} \quad (23)$$
$$v_{cb} = (SB_1 - SB_2)\, v_{dc} \quad (24)$$
$$v_{cc} = (SC_1 - SC_2)\, v_{dc} \quad (25)$$

The charging currents i_{cad} , i_{cbd} ,i_{ccd} *are expressed as:*

$$i_{cad}= i_{ca}(SA_1 - SA_2) \quad (26)$$
$$i_{cbd}= i_{ca}(SB_1 - SB_2) \quad (27)$$
$$i_{ccd}= i_{ca}(SC_1 - SC_2) \quad (28)$$

C. Modeling of Loads

Different nature of load (linear, nonlinear) are modeled here.

1) Linear Load

Three-phase balanced and unbalanced star connected resistive inductive loads (Z_{la}, Z_{lb}, Z_{lc}) are connected on a three-phase, four-wire system (Fig. 4a) with switches to disconnect any phase of the loads. These inductive–resistive three phase loads may be modeled by the following equations:

$$v_{ta}= R_l\, i_{la} + L_l pi_{la} \quad (29)$$
$$v_{tb}= R_l\, i_{lb} + L_l pi_{lb} \quad (30)$$
$$v_{tc}= R_l\, i_{lc} + L_l pi_{lc} \quad (31)$$

where i_{la}, i_{lb} and i_{lc} are the three-phase load currents, R_l and L_l are the load resistance and inductance parameters.

2) Non-Linear Load

A set of three single-phase nonlinear loads is connected to three-phase, four-wire grid system (Fig. 4b). Each phase load consists of a single-phase uncontrolled bridge rectifier with an AC input impedance and DC link capacitive-resistive (R-C) loading. When the diodes are conducting, AC supply mains is connected to the load. The basic equations for the three phase loads are written as:

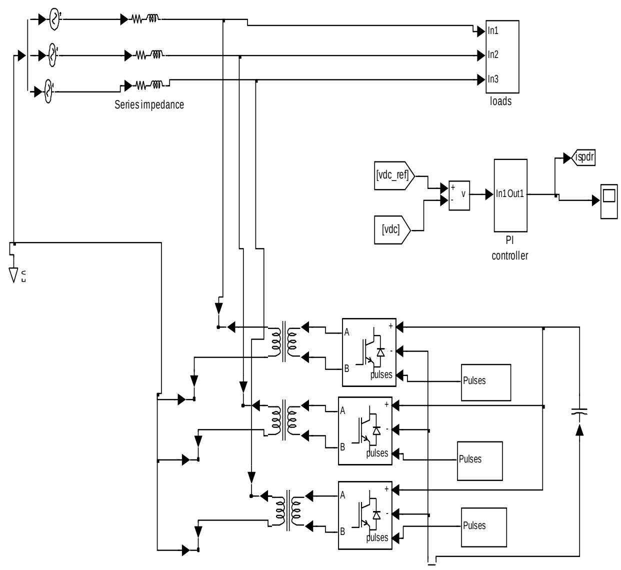

Fig. 3: MATLAB based model for the DSTATCOM configuration.

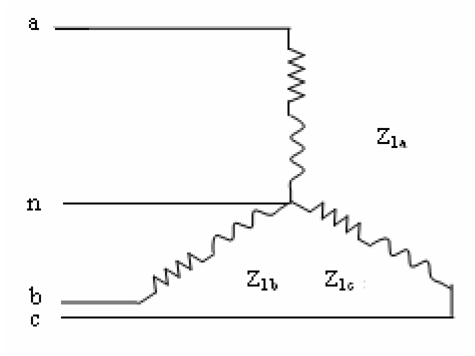

Fig. 4a: Linear load connected in star configuration.

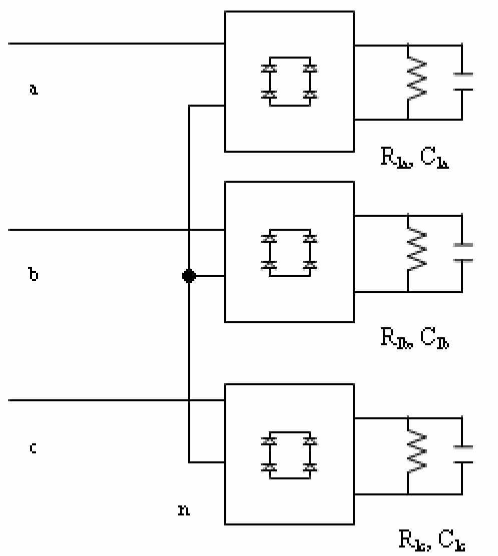

Fig. 4b: Non-Linear load connected for four-wire system.

$$v_{sa} = v_{la} + i_{la}R_s + L_s pi_{la} \quad (32)$$

$$v_{sb} = v_{lb} + i_{lb}R_s + L_s pi_{lb} \quad (33)$$

$$v_{sc} = v_{lc} + i_{lc}R_s + L_s pi_{lc} \quad (34)$$

where v_{sa}, v_{sb}, v_{sc} are three-phase ac voltages, R_s, L_s are supply impedance, v_{la}, v_{lb}, v_{lc} are voltages across load capacitors C_{la}, C_{lb}, C_{lc}. The load capacitor equations can be written as:

$$pv_{la}= (i_{da}-i_{ra}) / C_{la} \quad (35)$$

$$pv_{lb}= (i_{db}-i_{rb}) / C_{lb} \quad (36)$$

$$pv_{lc}= (i_{dc}-i_{rc}) / C_{lc} \quad (37)$$

where currents i_{la}, i_{lb}, i_{lc} are the load currents drawn from ac mains and i_{da}, i_{db}, i_{dc} are their magnitudes. The currents i_{ra}, i_{rb}, i_{rc} are dc load currents (v_{ta}/ R_{la}), (v_{tb}/ R_{lb}) and (v_{tc}/ R_{lc}) respectively. The load neutral current (i_{nl}) can be calculated from three-phase load currents i_{la}, i_{lb}, i_{lc} as:

$$i_{nl} = - (i_{la} + i_{lb} + i_{lc}) \quad (38)$$

VI. Results And Discussion

The developed model for DSTATCOM is tested over a variety of linear and non-linear loads for power quality improvement.

A. Performance of DSTATCOM with Linear Loads

The performance of DSTATCOM with linear loads is considered here for a variety of power quality improvement features viz. power factor correction and voltage regulation.

1) Power factor correction and Load balancing

Fig. 5 shows the performance of DSTATCOM for power-factor correction with R-L lagging load (20.5kW, 0.8pf). A PI controller is realized over the dc bus to regulate the dc link voltage to a value of 550V. The dynamic performance of variables like supply voltage (v_s), supply currents (i_s), load currents (i_l), compensator currents (i_c) and sensed and reference values of dc link voltage (v_{dc}) are shown to demonstrate the performance of DSTATCOM. It is observed that DSTATCOM improves the supply power-factor to unity. The supply currents are balanced, sinusoidal and in-phase with the voltages. For dynamic performance of DSTATCOM, load unbalancing is introduced at t= 0.66sec, one phase of load ('a' phase) is switched off (13.67 kW) and at t=0.76sec, the load is put back to 20.5kW. The control action provides a self-supporting dc bus.

2) Voltage regulation and Load balancing

Fig. 6 shows the response of the DSTATCOM for ac voltage regulation at PCC with 20.5kW, 0.8 lagging power-factor linear (R-L) load. The transient response for the various performance variables are shown for load changing from three-phase (30kW) to two-phase (20kW) at t=0.57sec. The dynamic performance of variables like supply voltage (v_s), terminal voltage at PCC (v_t), supply currents (i_s), load currents (i_l), DSTATCOM currents (i_c), sensed and reference values of dc link voltages (v_{dc}) and sensed and reference values of ac terminal voltage (v_{tm}) is observed in this figure. At t=0.57sec, when one phase (phase 'a') of the load is thrown off, dc link voltage tends to increase. This reflects in the form of an overshoot in DC link voltage. However, by controller action, the dc bus voltage of DSTATCOM and ac terminal voltage at PCC are regulated at their reference values. The supply currents are sinusoidal, balanced and slightly leading with respect to supply voltages. DSTATCOM maintains ac terminal voltage without any abnormal surge. The supply currents are sinusoidal, balanced and reduced in magnitude for transient period after t=0.57sec when the load currents are unbalanced.

B. Performance of DSTATCOM with Non-Linear Loads

Here a balanced three-phase nonlinear load is represented in the form of three single-phase uncontrolled diode bridge rectifiers feeding resistive load with parallel capacitor filter.

(1) Power Factor Correction and Harmonic Reduction

Fig. 7 shows the transient response of the DSTATCOM for power-factor correction and harmonic reduction with nonlinear loads. The response for the various performance variables are shown in this figure for R=25Ω and C=500μF (14.5kW) connected at end of diode rectifier. The load on the system is changed from 14.5kW to 19.8kW at t=0.4sec and back at t=0.6sec. The reference dc link voltage is set to 550V. It is observed that at t=0.4sec, the dc link voltage dips a little but the DSTATCOM regulates V_{dc} to reference value. It is observed that the supply neutral conductor has negligible current even though the load and DSTATCOM neutral conductors carry large currents. The waveform and Total Harmonic Distortion (THD) for supply current and load current are shown in Fig. 8 and Fig. 9. It is observed that THD of load current 63.88% is reduced to 3.88% in supply current.

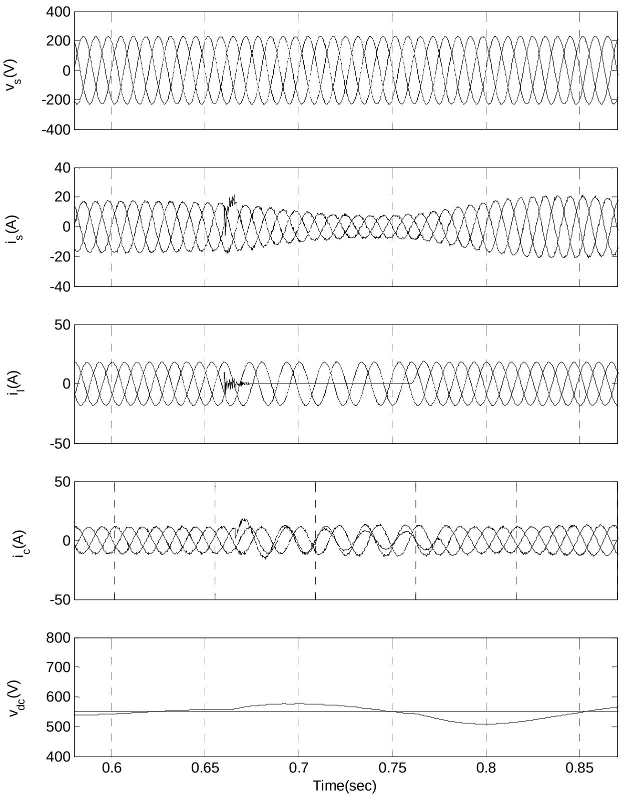

Fig. 5: Performance of DSTATCOM with linear loads for power factor correction

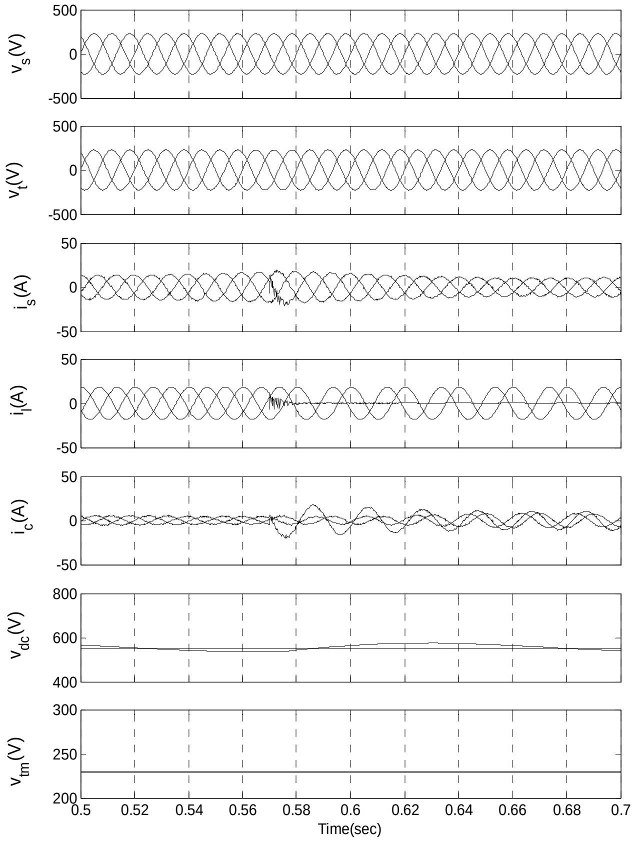

Fig. 6: Performance of DSTATCOM with linear loads for voltage regulation.

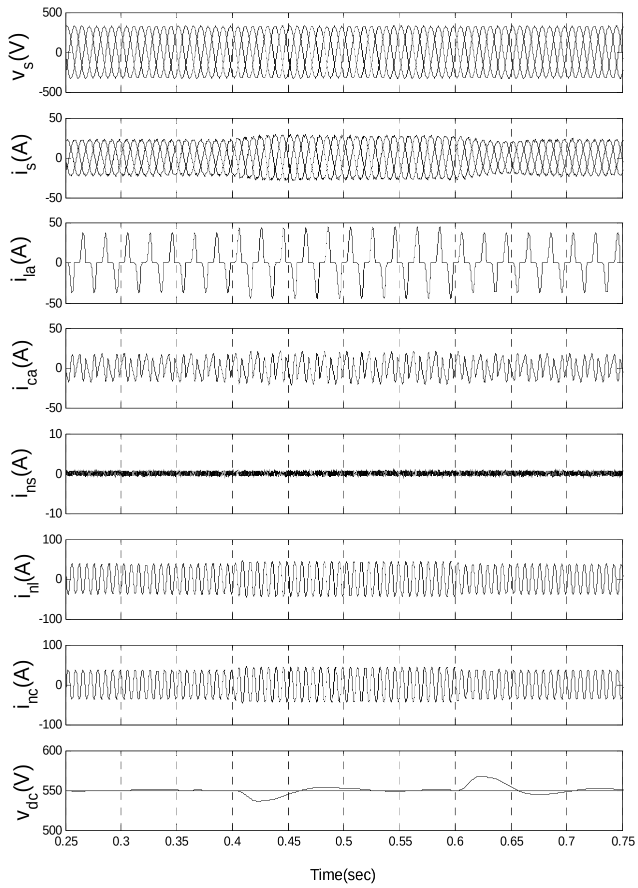

Fig. 7: Performance of DSTATCOM with non-linear load for power factor correction and harmonic reduction.

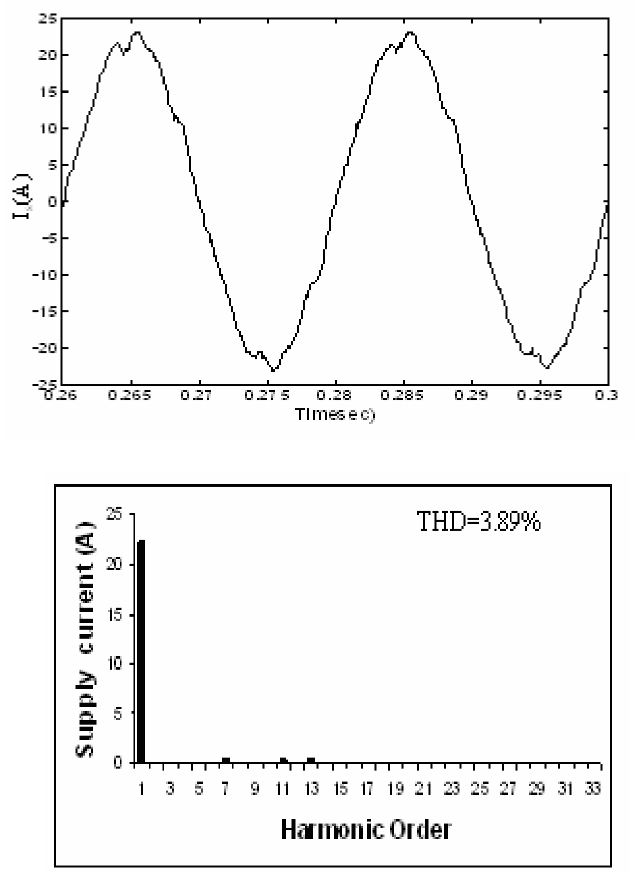

Fig. 8: Waveform and harmonic spectrum for supply current.

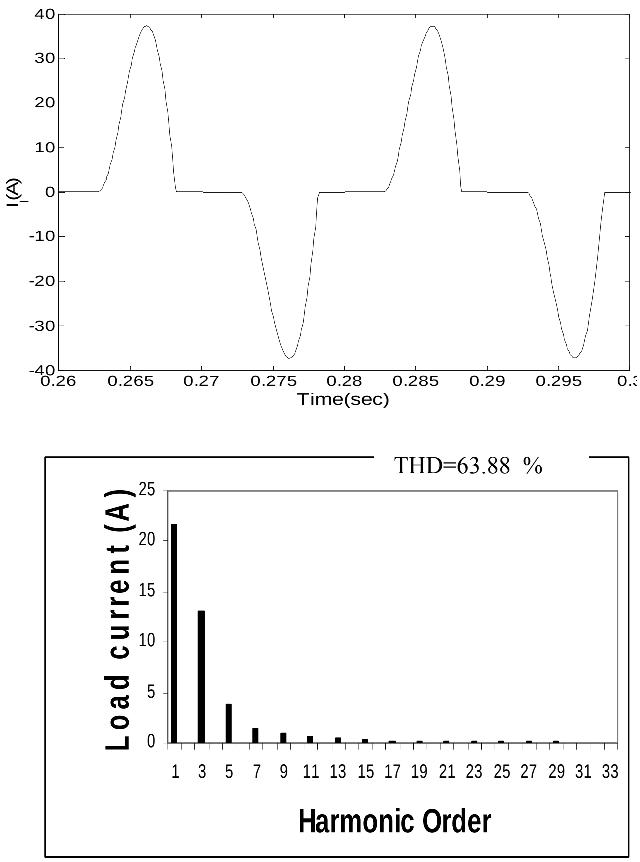

Fig. 9: Waveform and harmonic spectrum for load current I_L

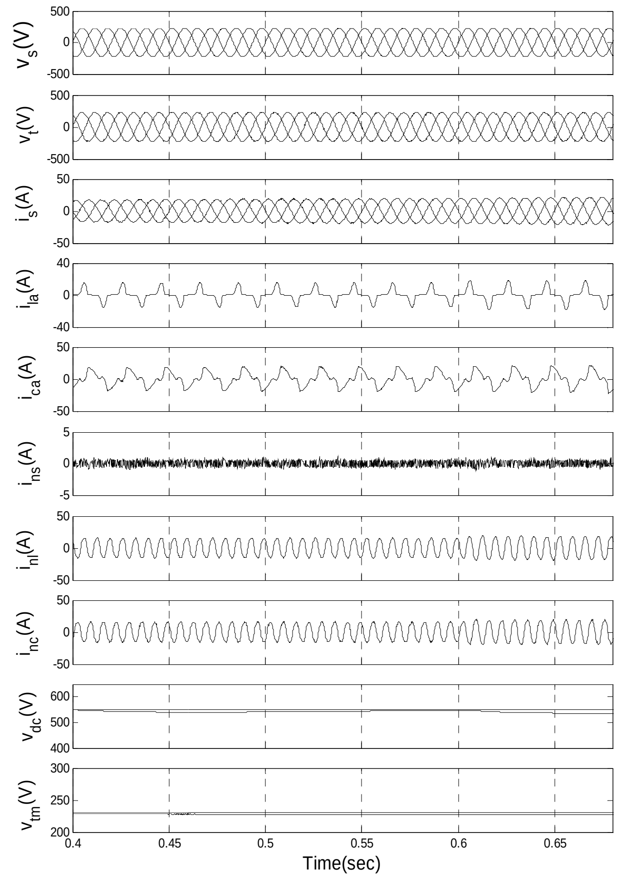

Fig. 10: Performance of DSTATCOM for voltage regulation and harmonic reduction

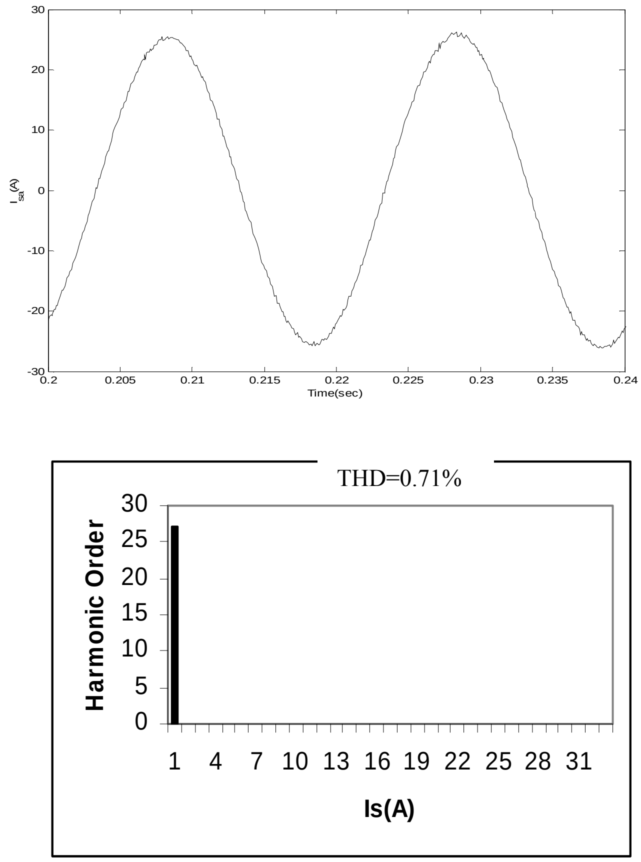

Fig. 11: Waveform and harmonic spectrum for supply current (I_s).

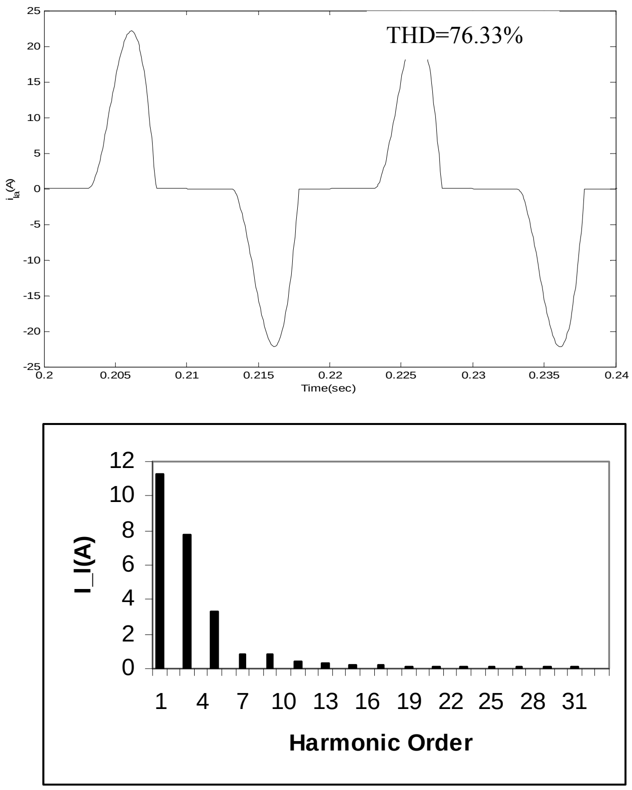

Fig. 12: Waveform and harmonic spectrum for load current (I_l)

(2) Voltage Regulation and Load Balancing

Fig. 10 shows the transient response under non-linear load for voltage regulation and harmonic elimination. Here, two PI controllers are used–one over V_{dc} and the other over V_{tm}. The dynamic response for the various performance variables are shown in this figure for R=50 Ω and C= 500μF (17 kW). The load on the system is changed at t=0.6sec (20kW). The supply currents are nearly sinusoidal, balanced and slightly leading with respect to supply voltages. Fig. 11 and Fig. 12 show the waveforms and harmonic spectra where THD of load current of 76.33% is reduced to 0.71% in supply current. The DSTATCOM controller has regulated DC bus voltage, ac terminal voltage at PCC under varying load conditions and also reduced THD of supply currents to less than the 5% limit.

VII. CONCLUSION

Detailed analysis of a three-phase, four-wire DSTATCOM has been carried out for a configuration realized from three-single phase VSIs. The advantages of this scheme are that independent control of the three VSI's is possible and a cost effective capacitor with lower voltage rating can be utilized. This in-turn reduces the cost and offers an economically viable option as compared to a four leg DSTATCOM. Power quality aspects such as pf correction, voltage regulation, the load balancing and harmonic reduction for linear as well as non-linear loads have been achieved using this DSTATCOM. The performance results have justified the load compensation of the proposed algorithm for DSTATCOM.

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