Implementation of Novel Low Cost Multilevel DC-Link Inverter with Harmonic Profile Improvement

R. Kavitha [1] P. Dhanalakshmi [2] Rani Thottungal [3]

Abstract – Harmonics is one of the most important criteria that decide the performance of the electrical devices. To reduce the harmonics, filters are used in inverter but it increases the cost and size of inverters. The multilevel inverters (MLI) are very interesting solution as it reduces harmonics and has the characteristics of synthesizing an approximate sinusoidal voltage on several DC levels. The significant advantages of multilevel configuration are voltage sharing both statically and dynamically and it produces better voltage waveforms with less harmonic contents. One particular disadvantage is it increases greater number of power semiconductor switches. To overcome this disadvantage a multilevel DC link inverter (MLDCL) is discussed in this paper. This comparatively reduces the number of switches, their gate drivers, compared with the existing MLI counterparts with harmonic profile improvement. Optimization of switching angle is performed using Simulated Annealing (SA) to reduce the 5 th, 7 th and 9th order harmonics and it is applied to a seven level cascaded MLDCL. The hardware is implemented using microcontroller based on the optimized firing angle obtained using SA.

Keywords - Multilevel inverter, optimized harmonic elimination, simulated annealing, THD

I. INTRODUCTION

The multilevel voltage source inverters are recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, and distributed energy resources (DER) area. Especially in DER area, because several batteries, fuel cells, solar cells, or rectified wind turbines or micro turbine can be connected through a multilevel inverter to feed a load or interconnected to the ac grid without voltage balancing problem [1]. In addition, multilevel inverters have a lower switching frequency than the standard PWM inverters and thus reduce the switching losses. The significant advantages of multilevel configuration are the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [2]. It also ensure even voltage sharing, both statically and dynamically.

Multilevel inverter synthesizes a desired voltage from several levels of dc voltages with low harmonics. As the number of levels increases, the harmonic distortion of the output wave decreases [5]. But the disadvantage is increase in number of switches and their gate drivers.

The paper first received 29 Aug 2008 and in revised form 13 Nov 2008. Digital ref: AI70401209

[1] Lecturer, Department of Electrical and Electronics Engineering, Kumaraguru college of Technology, Tamilnadu, India E-mail: kavithain2@yahoo.com

[2] Student, Department of Electrical and Electronics Engineering, Kumaraguru college of Technology, Tamilnadu, India

[3] Associate Professor, Department of Electrical and Electronics Engineering, Kumaraguru college of Technology, Tamilnadu, India.

As the number of level increases, the harmonic distortion of the output wave decreases. For reducing harmonics, if PWM or space vector modulation is used, it gives complexity in switching frequency in operation. Another approach is to find the switching angles in order to eliminate the specified harmonics. The mathematical theory of resultant is used to compute optimum switching angle [3]-[5]. But the disadvantage is complexity in solving polynomial equations. By employing optimized harmonic stepped waveform technique along with the multilevel topology, a low Total Harmonic Distortion (THD) output waveform without any filter circuit is possible [6]-[8]. A new Multilevel inverter topology using an H-bridge output stage with a bi-directional auxiliary switch is discussed [9].On the other hand, because of the low on state resistance and fast switching capabilities MOSFET's are utilized in multilevel inverters to reduce the cost or to provide a high bandwidth output voltage at high efficiency [10] –[11].

This paper presents a new topology of Multi Level DC Link Inverter (MLDCL), based on a MLDCL and a bridge inverter and it reduces the number of power semiconductor switches and gate drivers as the number of voltage level increases. The MLDCL's can be diode clamped, capacitor clamped or cascaded H Bridge inverter. The cascaded MLDCL topology is discussed in this paper. The MLDCL's provides a dc voltage with the shape of a staircase approximating the rectified shape of a commanded sinusoidal wave to the bridge inverter, which in turn alternates the polarity to produce an ac voltage. For a given number of voltage levels m, the required number of active switches is $2*(m-1)$ for the existing multilevel inverters but is $m+3$ for the MLDCL inverters [12]. Simulated Annealing (SA) based optimization technique is applied to determine the switching angle for cascaded MLDCL inverter, which eliminates specified higher order harmonics while maintaining the required fundamental voltage.

II. CASCADED MULTILEVEL INVERTER

A. Cascaded H-Bridge Multilevel Inverter

The traditional cascaded inverter formed by connecting single phase H-Bridge or cells in series as shown in Fig. 1. Each cell supplied by separate dc source and generates output voltage with different duty ratio. In this paper a seven level-cascaded multilevel inverter is considered and the switching angles θ_1, θ_2, θ_3 are obtained for harmonic optimization. The number of voltage levels generated by using N number of DC sources is given by $2N+1$. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, s1-s4, each inverter level can generate three differentvoltage outputs, $+Vdc$, $-Vdc$, and zero. The ac

outputs of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

B. Cascaded Half-Bridge–Based MLDCL Inverter

The cascaded MLDCL inverter consists of half bridge cells and one full bridge cell. Each half-bridge cell has two switches S_1 and S_2. They operate in a toggle fashion. The cell source is bypassed when S_1 is on and S_2 is off. The cell source adds to the DC link voltage when S_1 is off and S_2 is on. The half bridge cell produces DC bus voltage waveform with the shape of staircase and the full bridge inverter cell alternates the voltage polarity to produce an AC voltage of staircase waveform. A seven level MLDCL inverter is considered in this paper and it is shown in Fig. 2. Single-phase bridge inverter contains four switches from S_a to S_d. They are always work in pairs at the fundamental frequency of the output voltage. Specifically, the MLDCL formed by the n half-bridge cells provides a staircase-shaped dc-bus voltage of n steps to the full bridge inverter, which in turn alternates the voltage polarity to produce an ac voltage V_{an} of a staircase shape with $(2*n+1)$ levels .The IGBT is used for switches S_a, S_b, S_c, S_d of full bridge inverter as the voltage rating is higher.

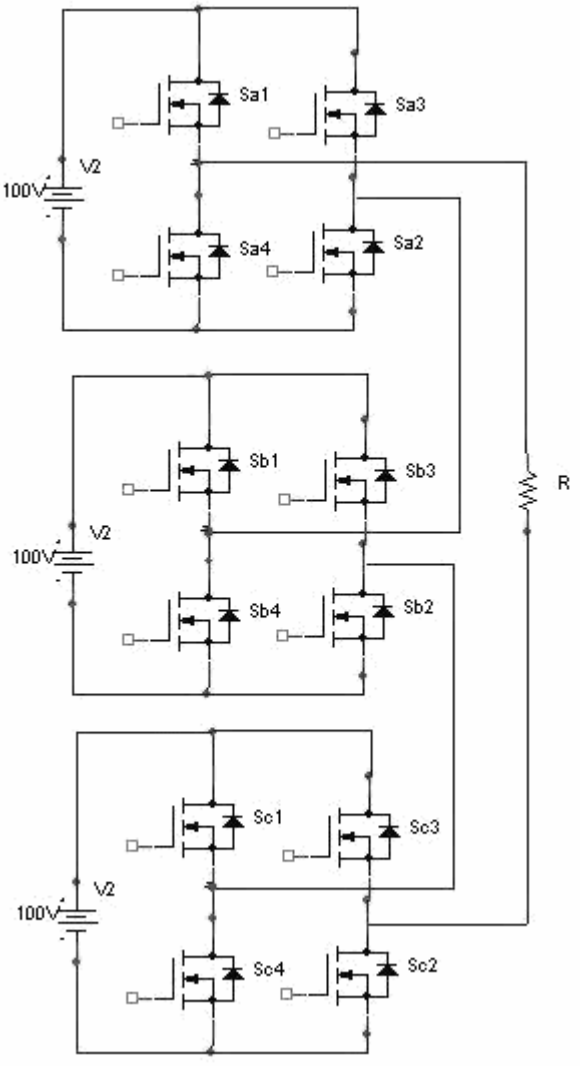

Fig. 1: Traditional 7-level cascaded multilevel inverter

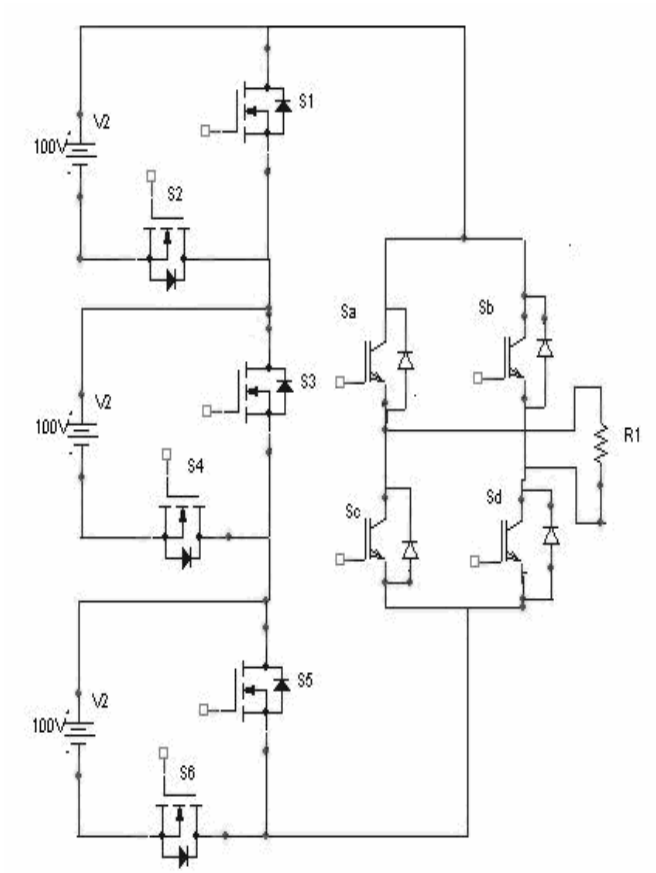

Fig. 2: 7-level Cascaded multilevel DC link inverter

C. Optimization using Simulated Annealing

Optimized harmonic stepped waveform technique is used to optimize the switching angles. 2_s+1 output levels can be synthesized with H-bridge inverters and separate dc sources (SDCSs). It consists of 3 switching angles θ_1, θ_2, θ_3 in each cycle as shown in Fig. 3. These voltage levels are supplied by SDCSs, whose amplitudes may be different or same. By considering the waveform, there are three possible optimization techniques to reduce the voltage THD. 1) step heights are optimized with equally spaced steps. 2) step spaces are optimized with the steps of equal height; and 3) optimizing both heights and spaces. This paper focuses on the second method, which uses equal voltage amplitude and optimizes the switching angles. By employing optimized harmonic stepped waveform technique along with the multilevel topology, a low Total Harmonic Distortion (THD) output waveform without any filter circuit is possible. By using above technique the energy function is obtained and solved using SA.

Simulated Annealing (SA) is a randomized algorithm for solving the global optimization problem. In the fields of chemistry and physics, there is a technique called Annealing used to create solid state metallic by slowly cooling the melted metal. The energy function E is the function to be minimized. The temperature T decreases gradually during the process. D is the difference between the energies of two states E_new and E_current. The Probability function depends on T and *D.* i.e.

exp (– (D/T))

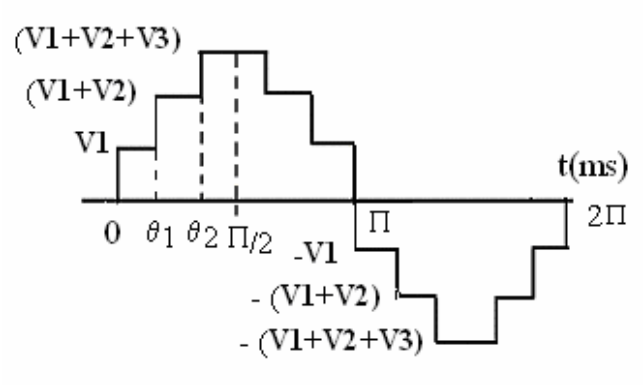

Fig. 3: The quarter-wave symmetric multilevel waveform

The idea of iterative improvement algorithms is to begin with a potential solution and to make adjustments to the solution over much iteration, moving the solution gradually toward a global optimum. In this project, the energy function is the total Harmonic distortion (THD) and is given in the equation (2). Higher number of iteration and temperature increase the rate of convergence.

$$THD = \frac{\sqrt{\sum_{n=2}^{200} 1/n \left[\sum_{k=1}^{N} (-1)^{k+1} \cos n\alpha_k\right]}}{\sum_{k=1}^{N} (-1)^{k+1} \cos n\alpha_k} \qquad (2)$$

N is the number of switching angles per quarter
n is the harmonic order
α_k is the calculated switching angles.

The steps for formulating a problem and applying SA as follows:

- Initialize temperature to 2000, iteration
- Select switching angles, current E, at random
- Substitute in Energy function
- Update E Generated
- While Temp>1
- For 1 to iteration
- Select new angles, in the neighborhood of current angles using the two Interchange methods with random values
- Update angles Generated
- Update E Generated
- Calculate D= *E*_new – *E*_current
  If (D<=0)
  Best E= *E*_new
  Else if random [0, 1] < exp – (D/T)
  Best E = *E*_new
  End if.
- Iteration = iteration-1
- End iteration.
- Temp =Temp -1
- End

This Simulated Annealing code is programmed in the MATLAB m-file. This code can find the switching angle solutions for a multilevel inverter with any number of levels and for the elimination of any number of harmonics.

III. Simulation And Experimental Results

A. Simulation results

Simulated Annealing is used to determine the optimum switching angles and the results are shown in table I. The simulated waveform of MLDCL inverter without optimization is given in the Fig. 4. The simulated waveform of MLDCL inverter by using the optimized angle from simulated annealing is given in the Fig. 5. The simulation is performed with 100V DC source using IGBT and MOSFET. Ode23tb solver with relative tolerance is used for simulation. Harmonic spectrum is obtained using power GUI in Simulink.

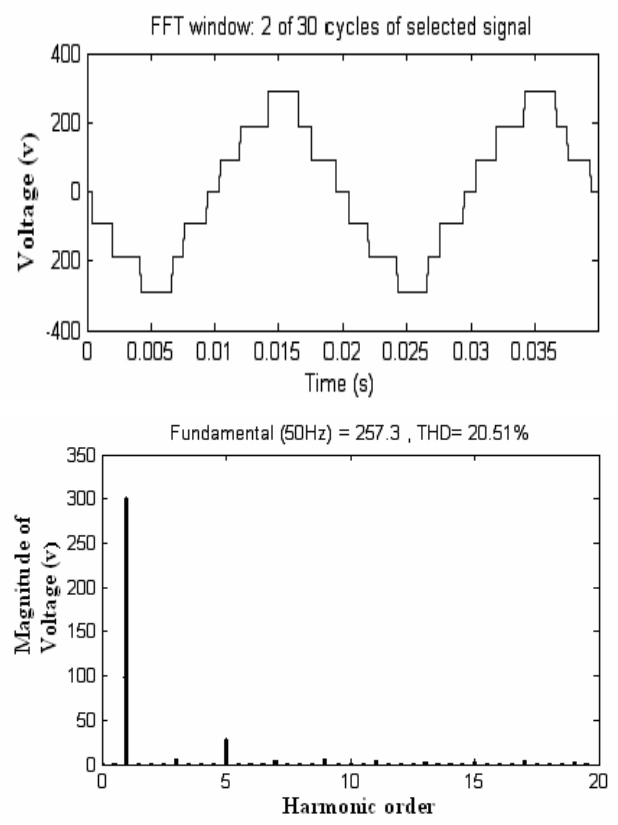

Fig. 4: Simulated waveforms and harmonic spectrum of seven level cascaded MLDCL inverter without optimization

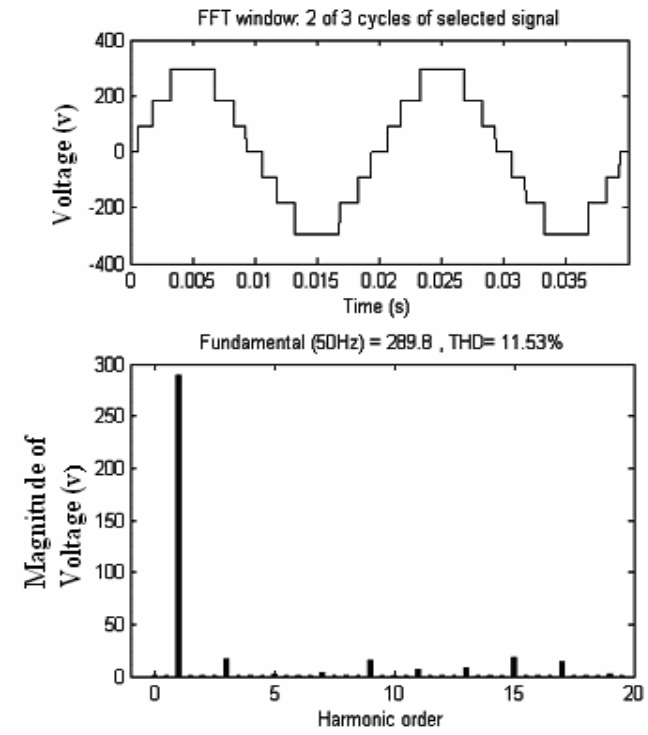

Fig. 5: Simulated waveforms and harmonic spectrum of seven level cascaded MLDCL inverter using SA.

B. Comparison of multilevel dc-link inverter and existing counterparts

The multilevel dc-link inverter effectively reduce the number of switches and their gate drivers. Cascaded multilevel inverter requires $2*$ (m-1) number of switches and the cascaded MLDCL require only (m+3) number of switches. In addition, the new multilevel dc-link inverter saves the cost of the inverter circuit by having an additional module of single-phase full bridge (SPFB) inverter. With higher voltage levels, only two switches are enough for fabricating each bridge in multilevel dc-link (MLDCL) with four switches in SPFB inverter.

Fig. 6 mentions the reduction in number of switches when increasing the number of levels. As the number of level increases switches are considerably reduced. For a eleven level inverter cascaded Multilevel inverter requires 20 switches and cascaded MLDCL requires 14 switches.

Table 1: component count comparison—seven levels

No of switches for seven level(m=7)		Optimised angles			THD (%)
Multilevel DC link(m+3)	Multilevel 2*(m-1)	θ_1	θ_2	θ_3	11.53
10	12	9.57	36.9	54.2	

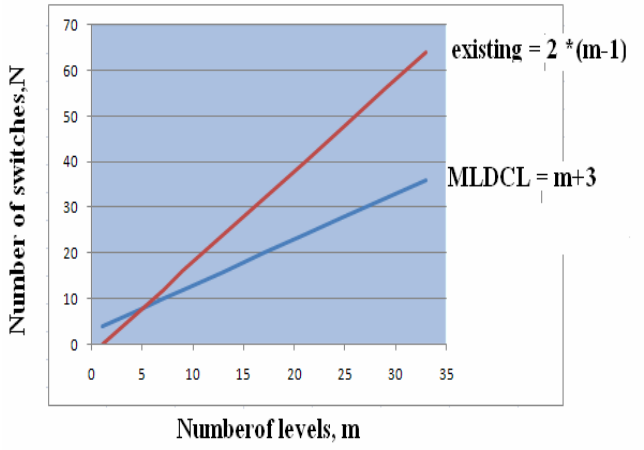

Fig. 6: Comparison of required number of switches.

C. Hardware implementation

A microcontroller based seven level-cascaded multilevel dc-link inverter is fabricated and tested. The circuit diagram of opto-isolator with half bridge cell and the experimental setup is given in Fig. 7 and Fig. 8 respectively. The microcontroller PIC 16F877A is used to generate the pulses. Port c of the microcontroller generates pulse for triggering the MOSFET. Timer 0 is used for producing the delay required for the duration T_{ON} and T_{OFF}. The microcontroller operates at a clock frequency of 20 MHz. The opto-isolator 4N35 is used for isolation between the controller and the inverter circuit. The experimental parameters are given in Table 2. The pulses are generated based on the optimized firing angles obtained by SA method in simulation. The hardware prototype is shown in Fig. 9. The oscillogram of voltage waveform is given in Fig. 10.

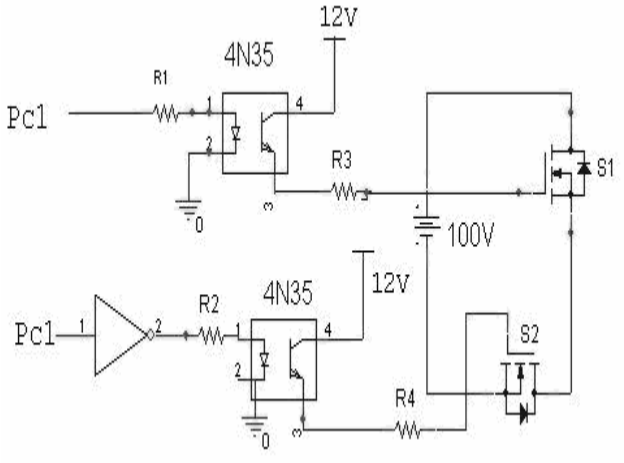

Fig. 7: Circuit diagram of opto coupler and half bridge cell

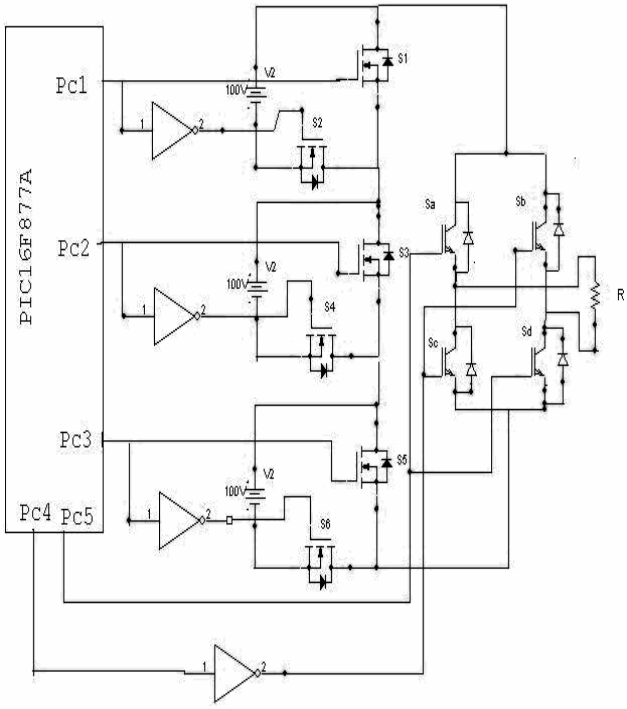

Fig. 8: Experimental circuit diagram

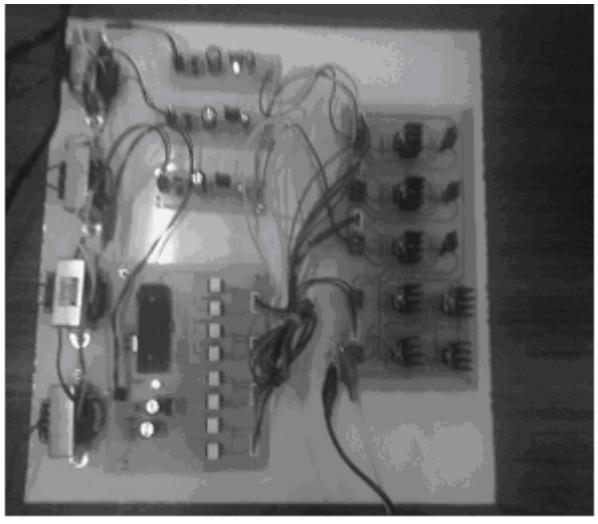

Fig. 9: Hardware prototype

Table 2: Experimental parameters

Components	Value
MOSFET	IRF740
PIC Microcontroller	PIC16F877A
IGBT	CM400DY
Optocoupler	4N35
DC Voltage	100V
R-Load	50Ω

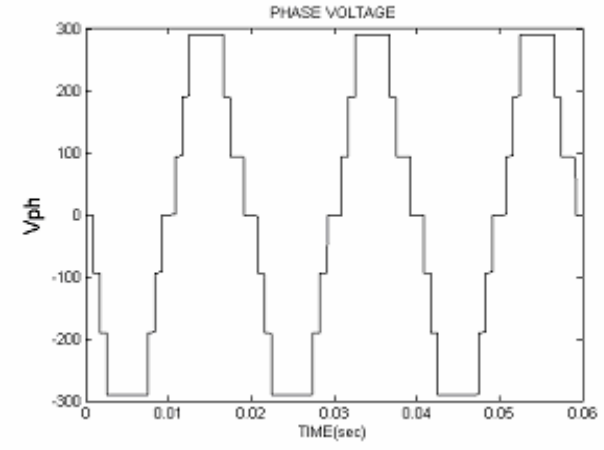

Fig. 10: Oscillogram of voltage waveform

IV. Conclusion

Cascaded multilevel dc-link, inverter is simulated using MATLAB Simulink based on the optimized firing angle obtained from SA and the convergence time is 180 seconds. The hardware prototype is implemented using Microcontroller. A seven level-cascaded multilevel dc-link inverter is successfully fabricated and tested. The Total Harmonic Distortion obtained using simulation is 11.53% and hardware is 13.21%. The optimized angle obtained by simulation is used for experimental verification and it shows harmonic profile improvement .The new multilevel dc-link inverter needs least number of components than the existing multilevel inverters for the same level of output waveform. By increasing the number of levels of the multilevel dc-link inverter topologies, the parameters like switches, gate driver, are reduced with better output waveform.

Acknowledgment

The authors thank the Management of Kumaraguru College of Technology for providing infrastructure to implement the project.

References

[1] Manjrekar, P. Steimer, and T. Lipo, "Hybrid multilevel powerconversion system: A competitive solution for high-power applications", IEEE Trans. Ind. Applications, Vol. 36, No. 3, pp. 834–841.

[2] L. M. Tolbert, F. Z. Peng, T.G. Habetler, "Multilevel converters for Large Electric Drives", IEEE Trans. Ind. Applications, Vol. 35, No.1, Jan/Feb. 1999, pp. 36-44.

[3] Jose Rodriguez, Jih-Sheng Lai, Fang ZhengPeng "Multilevel inverters: A survey of topologies, controls and applications", IEEE Trans. Ind. Electron., Vol.49, No.4, August 2002.

[4] J. Chiasson, L. M. Tolbert, K. McKenzie, and Z. Du, "Eliminating harmonics in a multilevel converter using resultant theory", in Proc. IEEE Power Electronics Specialists Conf., 2002, pp. 503–508.

[5] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "A complete solution to the harmonic elimination problem", IEEE Trans. Power Electron., Vol. 19, No. 2, Mar. 2004, pp. 491–499.

[6] Z.Du, L.Tolbert and J.Chiasson, "Active Harmonic Elimination on Multilevel power converters", IEEE Trans. Power Electron., Vol. 21, No. 2, Mar. 2006, pp. 459–469.

[7] J. Chiasson, L. M. Tolbert "A unified approach to solving the harmonic elimination equations in multilevel converters", IEEE Trans. Power Electron., Vol. 19, No. 2, Mar. 2004, pp. 478–490.

[8] S. Sirisukprasert, J.S. Lai, and T. H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters", in Conf. Rec. IEEE-IAS Annu. Meeting, Rome, Italy, Oct. 2000, pp 2094-2099.

[9] Gerardo Ceglia "A new simplified Multilevel inverter Topology for DC –AC conversion" IEEE Trans. Power Electron., Vol. 21, No. 5, September 2006, pp. 1311–1317.

[10] Takahasti and K.Iwaya "100 kHz 10 kW switching type power amplifier using multilevel inverter" in proc. 4th IEEE International Conf. Power Electronics and Drive Systems.,Vol.1, Oct 22-25, 2001, pp. 286-291.

[11] B.A.Welchko, M.B.de Rossiter Correa and T.A.Lipo "A three level MOSFET inverter for low power drives" IEEE Trans. on Industrial Electron., Vol. 51, No. 3, Jun 2004, pp. 669-674.

[12] Gui-jia Su "Multilevel DC Link Inverter" IEEE Trans. Ind. Applications, Vol. 41, No.1, May/June. 2005, pp. 848-854.

Biographies

R. Kavitha obtained her B.E from Bharathiar University and M.E Degrees from Anna University in 2001 and 2004 respectively. She has 6 years of teaching Experience. She is now working as Lecturer in Kumaraguru college of Technology, India. She is member of ISTE. Her research interests are Multilevel inverters and Resonant converters.

Rani Thottungal obtained her B.E and M.E Degrees from Andhra University-India and her Ph.D. from Bharathiar University-India. She is currently working as Associate Professor in Kumaraguru college of Technology, India. Her research interest includes power system and power Inverters.

P. Dhanalakshmi obtained her B.E and M.E Degrees from Anna University- India. She is currently working in patni Computers-India. Her research interests are Multilevel inverters and optimization techniques.