High Voltage Multilevel DC-DC Converter in Auto Balancing Mode

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Abstract — In this paper balancing theory of a three level DC-DC converter is presented. It is proposed to make dc link voltages balanced across the capacitor stack. This voltage distribution gets equally distributed by selecting the appropriate switching frequency. This work is to investigate the new control scheme to incorporate the current adaptive switching in DC-DC converters. The major advantage of this novel scheme is to develop the bi-directional high voltage multilevel converters required in many high power industrial applications. A systematic approach and mathematical study is presented. Simulation results validates this proposed scheme.

Keywords - Adaptive current control, DC-DC bi-directional Converter, High power converters.

I. INTRODUCTION

Multilevel DC-DC converters are mostly used in high power applications in many industrial applications. They offer advantage of operating at relatively high DC bus voltages with reduced harmonic content, low EMI and low voltage stress on the devices. Multilevel converters can achieve smoother and less distorted AC-DC, DC-AC, and DC-DC power conversion. These technologies are used in the utility and large motor drives applications. These are presented in many of the literature [1].

In multilevel converters, DC bus capacitor banks are stacked in series. These converters will meet more voltage balance problem than that in AC-DC or DC-AC converter. Because of the asymmetric DC output voltage, fewer redundant switching states will be available in DC-DC multilevel converter. Also the difference of characteristics for each individual component, either on semiconductors or on passive components, will cause the voltage unbalance [2]-[7],[10]-[11].

In most cases, a dynamic balance control strategy is necessary to balance the capacitor voltages, which requires enough redundant switching states.

The transfer of energy from one end to another in DC – DC converter is of application dependent and also decided by the type of load.

The paper first received 2-Jun-2009 and in revised form 1-Sept- 2009. Digital Ref: A17050214

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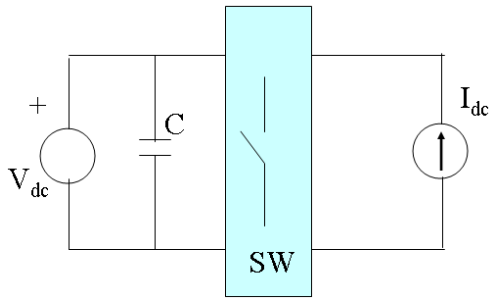

Fig 1: Generalized converter

The most convenient structure is to control the load current while maintaining the source side voltage constant across the supply side. This simple configuration is presented in figure 1. The industrial application of bi-directional DC/DC converters is for the interfacing the energy storage device like Superconducting Magnetic Energy Storage (SMES) coil to the power system through the voltage source inverters to mitigate the power quality problems. The SMES coil is charged from the power system under the normal operating condition and discharge in case of real power demand by the power system. The interface of the coil to inverter is across the dc link has to be at the high voltage level. This causes the dc capacitor and inverter semiconductor components to operate on high stress levels. Therefore the multilevel DC/DC converters are preferred. However, this leads to have multiple dc stages with capacitors. The voltages across these dc stages are governed by converter operating conditions. It is necessary to maintain the dc voltage constant during the converter operation [8]. There are various dc voltage balancing control strategy involving the additional sensor and control circuits [9].In this paper, dc voltage balancing is achieved with proposed control strategy.

The energy balance theory with basic circuit laws can be used for analysis this circuit. However, the controlled power conversion process involves the switching structure of the DC-DC converters. One such converter structure is analyzed in this paper. In this paper, analysis of DC-DC converter is presented with the voltage balancing across the capacitor. The typical design considerations are also presented. In figure 2, three level topology of a proposed DC-DC converter is shown.

The operating principal of the three level DC-DC converter and current adaptive switching control is presented. The benefits of the proposed circuit with high power capability are as under.

- Voltage balancing at DC bus
- Soft-switching is realized
- High power applications
- Lower cost due to high frequency transformer
- Use of multilevel structure can reduce the Total Harmonic Distortion (THD).

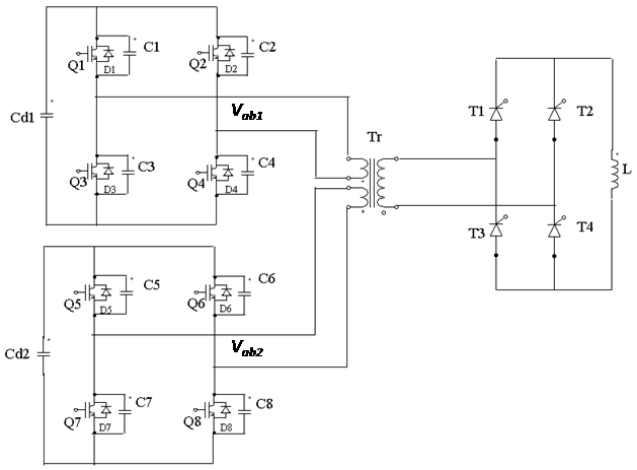

Fig 2: Multi level converter

II. CONVERTER OPERATION

The circuit topology is shown in figure 2 is analyzed for its operation. The one complete cycle is presented in the following figures. The circuit is built with the switches Q1-Q8 and C1-C8 capacitors connected across them. The secondary of the transformer (T_r) is having full bridge converter connected to the inductor coil (L). The switching signals to H bridge on primary side and for the full bridge thyristors on secondary are shown in figure 3 (a) and (b) respectively. The voltages and currents across the each primary winding of the transformer is shown in figure 4. The secondary side currents (I_{T1}, I_{T2}) and voltages are shown in figure 5.

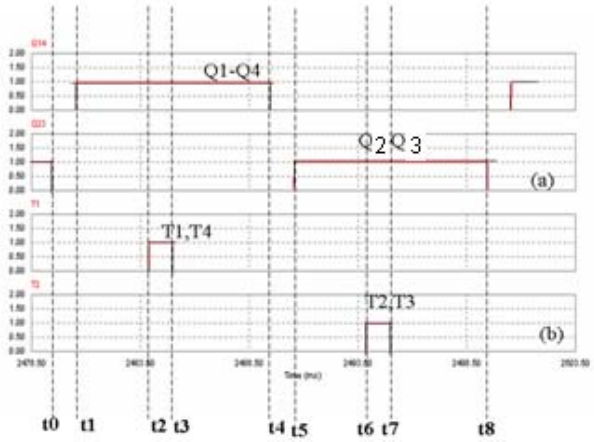

Fig 3: (a) Switching pulses for H-bridge on primary and (b) bridge on secondary side of the transformer

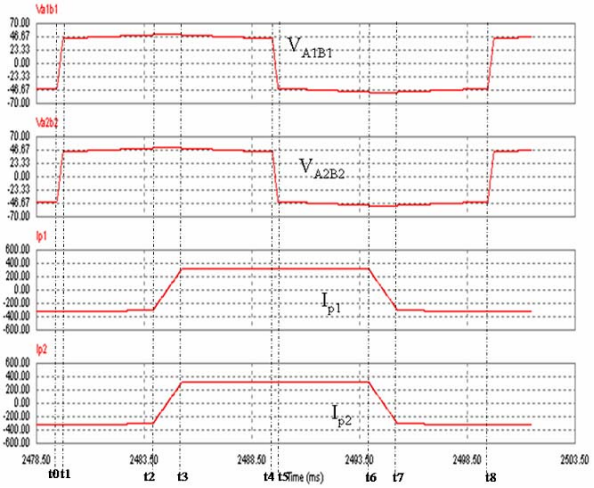

Fig 4: Voltages $V_{A1B1,}$ V_{A2B2} and currents I_{p1} and I_{p2}

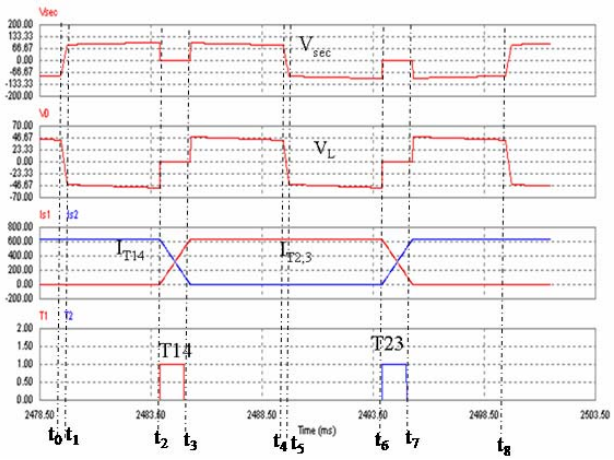

Fig 5: Output voltage- V_{sec} and coil voltage- V_L and with thyristor currents I_{T14} and $I_{T2,3}$ with respect to switching pulses

The switch Q2 and Q3, Q6 and Q7 at the t_o instant are off and circuit is shown in figure 6.The time t_o-t_1 indicates the blanking time and its operating condition is indicated in figure 7.The operation of the switching, Q1 and Q4, Q5 and Q8 indicates the discharging operation during the time t_1-t_2. This is shown in figure 8. The change over of the switching on secondary side by triggering the thyristors is shown in the figure 9.This is causing current (I_{T23}) to transfer to another pair of thyristor. This current transfer is due to the voltage (V_L) applied across the coil. The average current through the coil (I_o) is constant and maintains its direction. After this half cycle, the charging cycle starts as the voltage across coil is positive. The subsequent operation is shown in figure 10, 11 and 12.

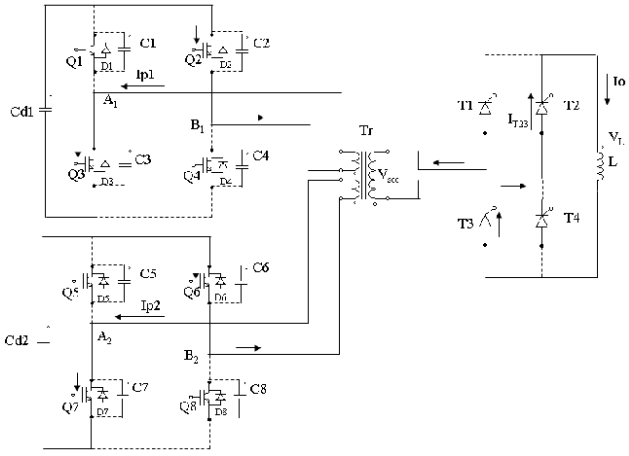

Fig 6: Operation at t_o

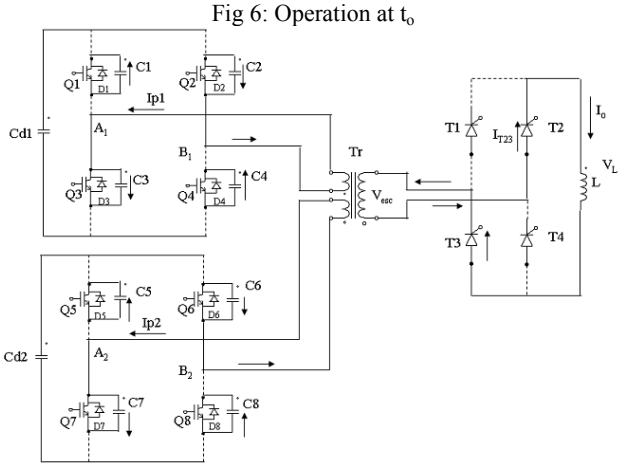

Fig 7: Operation during t_o-t_1

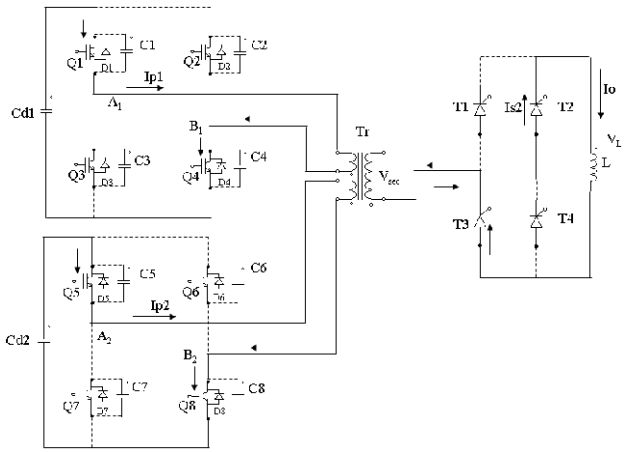

Fig 8: Operation during t_1-t_2

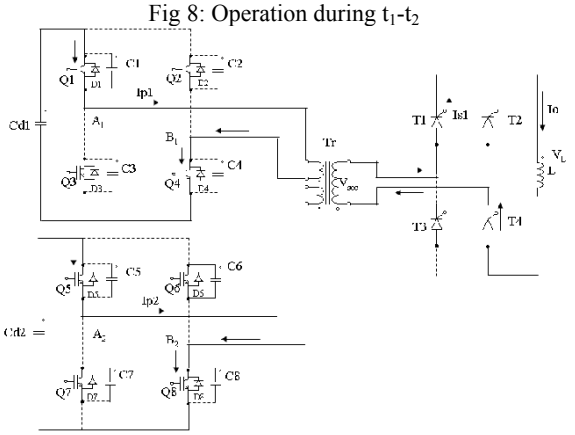

Fig 9: Operation during t_2-t_3

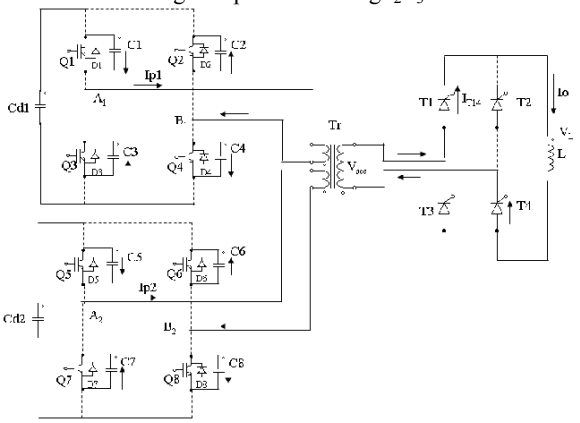

Fig 10: Operation during t_3-t_4

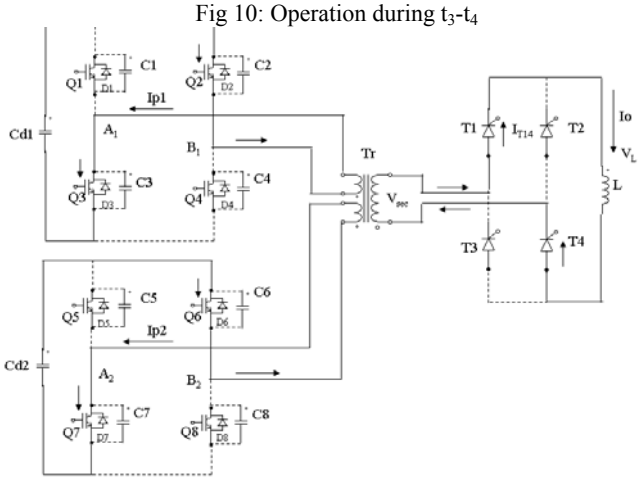

Fig 11: Operation during t_4-t_5

III. BALANCING THEROY OF MULTI-LEVEL CONVERTERS

The equivalent circuit for H- bridge under energy transferred across the transformer, that is from capacitor to inductive coil and from coil to capacitor is shown in figure 13 (a) and (b) respectively.

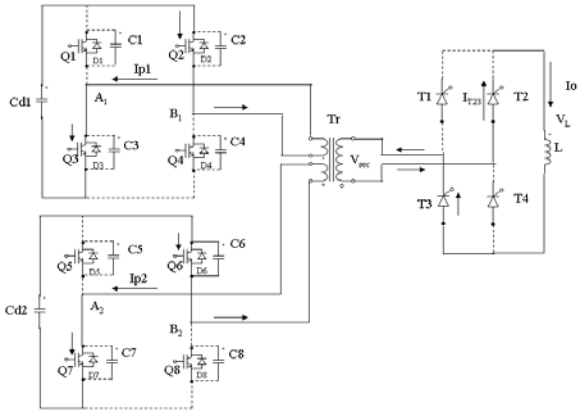

Fig 12: Operation during t_5-t_6

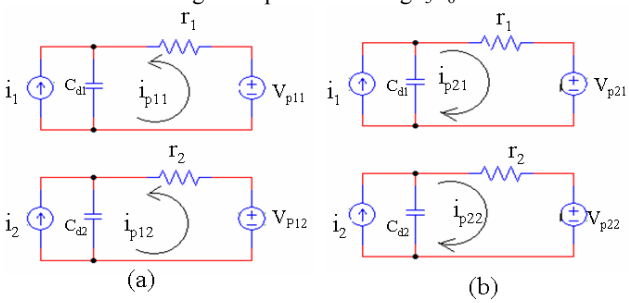

Fig 13: Circuit equivalent stages under first and third stage

The energy transfer across the transformer is simply represented from current source (i_1) and voltage source (Vp_{11}) with one stage converter having equivalent resistances r_1, representing the drop across converter and transformer winding. Similarly another winding is also represented.

The mathematical analysis is carried out with these circuits. The ampere turns across the transformer winding is written as

$$N_p * \left(i_{p11} + i_{p12}\right) = N_s * I_0 \qquad (1)$$

The N_p and N_s represents the primary and secondary number of turns respectively. The current through coil is I_o.

$$i_{p11} + i_{p12} = \frac{I_0}{K} \qquad (2)$$

Where, K is the turns ratio.
Assuming that the sum of the voltage across C_{d1} and C_{d2} are 2V, the voltage across C_{d1} is $V + \Delta V$ and the voltage across C_{d2} is $V - \Delta V$, then from figure 3, current equations can be written as

$$i_{p11} = \frac{V_{p1} - (V + \Delta V)}{r_1}, i_{p21} = \frac{V_{p11} - (V + \Delta V)}{r_1} \qquad (3)$$

$$i_{p12} = \frac{V_{p1} - (V + \Delta V)}{r_2}, i_{p22} = \frac{V_{p12} - (V + \Delta V)}{r_2} \qquad (4)$$

The average current on the primary can be written as

$$i_{p1} = \frac{\frac{V_{p1} - (V + \Delta V)}{r_1} T_1 + \frac{V_{p2} - (V + \Delta V)}{r_1} T_2}{T} \qquad (5)$$

$$= \frac{V_{p1} - (V + \Delta V)}{r_1} d + \frac{V_{p2} - (V + \Delta V)}{r_1} (1 - d)$$

$$i_{p2} = \frac{V_{p1} - (V + \Delta V)}{r_2} d + \frac{V_{p2} - (V + \Delta V)}{r_2} (1 - d) \quad (6)$$

The period $T_1 = t_2 - t_o$ and $T_2 = t_4 - t_3$. can be represented in terms of duty cycle $d = \frac{T_1}{T}$, and $\frac{T_2}{T} = 1 - d$.

The difference of current is Δi_p on the primary side is

$$\Delta i_p = i_{p1} - i_{p2}$$
$$= \frac{\left[V_{p1} - (V + \Delta V) r_2\right] - \left[V_{p1} - (V - \Delta V)\right] r_1}{r_1 r_2} d$$
$$+ \frac{V_{p2} - (V + \Delta V) r_2 - \left[V_{p2} (V - \Delta V)\right] r_1}{r_1 r_2} (1 - d) \quad (7)$$

The unbalance due to equivalent resistance of these two stages can be represented with the reference value of resistance R. Which is represented as $r_1 = R$ and $r_2 = R + \Delta R$.

From above equations and after simplification it is represented as

$$\Delta i_p = \frac{-2\Delta V R - \Delta R\left[(V_{p2} - V_{p1}) d + V - V_{p2}\right] \Delta R \Delta V}{R(R + \Delta R)} \quad (8)$$

Neglecting the term $\Delta R \Delta V$ and considering the balance of the charging and discharging mode, the currents are represented as $(i_{p11} + i_{p12}) = -(i_{p21} + i_{p22})$. By substituting the values of currents and simplifications

$$\left[4V - 2(V_{p1} + V_{p2})\right] R + \left[2V - (V_{p1} + V_{p2})\right] \Delta R + \Delta R = 0 \quad (9)$$

It can be written as

$$2V - (V_{p1} + V_{p2}) = 0 \quad (10)$$

This gives the value of voltage V as

$$V = \frac{V_{p1} + V_{p2}}{2} \quad (11)$$

From equation 2, it can be written as

$$V_{p1} - V_{p2} = 2 \frac{I_0}{K} * \frac{R(R + \Delta R)}{(2R + \Delta R)} \quad (12)$$

Substituting these values of voltages in the equation 8,

$$\Delta i_p = \frac{-2\Delta V R - \Delta R\left(\frac{1}{2} - d\right) 2 \frac{I_0}{K} * \frac{R(R + \Delta R)}{(2R + \Delta R)}}{R(R + \Delta R)} \quad (13)$$

The current flow in capacitors are

$$i_{cd1} = (i_1 + i_{p1}), i_{cd2} = (i_2 + i_{p2}) \quad (14)$$

$$\Delta i_{cd} = i_1 + i_{p1} - (i_2 + i_{p2}) = \Delta i + \Delta i_p \quad (15)$$

combining (13) and (15), the effective current difference is written as

$$\Delta i_{cd} = i_1 - i_2 + \frac{-2\Delta V R - \Delta R\left(\frac{1}{2} - d\right) 2 \frac{I_0}{K} * \frac{R(R + \Delta R)}{(2R + \Delta R)}}{R(R + \Delta R)} \quad (16)$$

From the above equation, if the current Δi_{cd} is positive then current flowing in to the C_{d1} is larger than current flowing into the C_{d2}, and the voltage across C_{d1} raises relatively more than the C_{d2}. It will be reverse if the Δi_{cd} is negative. If $i_1 = i_2$ then Δi_{cd} become

$$\Delta i_{cd} = \frac{2\Delta V}{R} \quad (17)$$

If ΔV is positive and Δi_{cd} becomes negative, a very small voltage difference will result in a very large Δi_{cd}, which will cause the voltage across the C_{d1} diminish relatively very quickly to the voltage across C_{d2}. The voltage ΔV will decrease quickly to zero. The voltage balance will be achieved across the C_{d1} and C_{d2}.

The difference of voltage ΔV is more sensitive to the change in converter current and the equivalent resistance of the switches and circuit components. The design parameters of the converters are selected to maintain the voltage drop near to zero to operate this bidirectional converter in stable condition. One of the control factors to achieve the voltage balance is to operate the converter with selected switching frequency zone. This is one of the most important parameters to make these converters operations more robust and economical. The concept of variable switching frequency control through adaptive current control is introduced and presented in next section.

IV. ADAPTIVE CONTROL OF DC-DC CONVERTER

The control scheme is incorporated to maintain the voltage balance across the dc link capacitors by sensing the dc voltages and controlling the switching frequency. The dc link capacitor and front end high frequency transformer are the two components, which selects the switching frequency. By keeping the duty ratio constant, frequency is varied through the current balance sensing circuit. The limit is decided upon the maximum allowable safe operating voltages required for the DC converters. Analysis indicates the balances are maintained from no load to full load operating conditions with 15-20 % variation in switching frequency.

The inductive coil current regulation is carried out by regulating the switching pulses of thyristors. This regulates the energy storage in the inductor. There are three stages of operation. In the first case, the current is maintained constant, in the second, coil current is increased and in third case, current is reduced. The pulse position is shown in the figure 14. The thyristor pulse width is 20^o and positioning of the pulses for both the thyristors are placed 180^o apart. The location of the pulse in the half cycle decides the charging or discharging. To maintain the current through the coil constant, these pulses are to be located at 90^o in each half cycle. The average coil current is constant. If the charging is required then the pulses are to be moved above 90^o and for discharging the pulses are to be placed below the 90^o. The reference for this is considered with the storage capacity of the inductor coil.

The control of current in coil is one variable while the dc voltage across the capacitors is another.

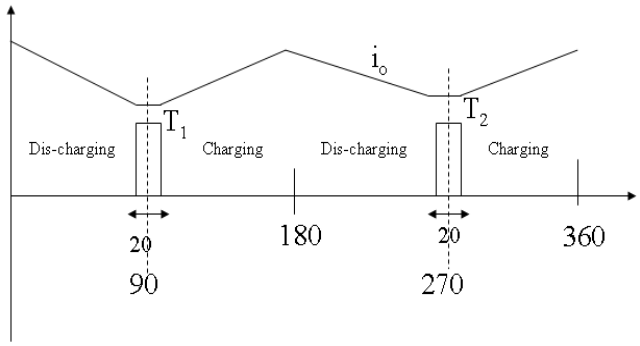

Fig 14: Charging and discharging pulse positions

The control scheme is implemented as shown in figure 15. The reference current set for the coil is generally a maximum current to which the coil can be charged. This reference can be made adaptive with system load current to get the advantage of the off-period availability of the power. This can be made to follow the load demand if the system is interfaced with the power system with the balance voltage source inverters. The switching of DC-DC multilevel converter is set to the frequency from 50 Hz to 5 kHz. This is depending on the power handling capacity of the converter. The switching frequency will be low as the power rating of the converter is more. The frequency is regulated by using voltage controlled oscillator (VCO). The required control on position (α) of the pulses for the half bridge converter is generator through the synchronizing circuit. The charging or discharging mode is regulated by comparing the actual coil current with the set reference value of the current. This control algorithm can be implemented on digital signal processor.

V. PERFORMANCE OF THE CONVERTER

This control with the circuit considering the IGBT switches is simulated in the PSIM. The design parameters are chosen to make it more realistic so that the prototype could be built. The simulation parameters are given in the Table-I. The switching frequency of the DC-DC converter is set to visualize the operating of the converter switches on both the sides of the transformer. The voltages across the switch (Q1) are shown with the capacitor voltage (C1) in the figure 16. The switching of these devices takes place exactly at the zero voltages.

This confirms the ZVS operation. Similarly the secondary side converter is operating at the zero current (ZCS). This is observed from the current and operating pulses as shown in the figure 17. The results of simulation indicating the charging operation of the coil is presented in figure 18.The charging current is .indicated with the time period of charging and discharging. In the charging mode, the discharging period is always less than the charging time period to push the storage of the energy. This indicates the pulse positioning of the thyristors on secondary side of the transformer governs the control of coil current. The capacitor voltages across each of the stages (V_{d1} and V_{d2}) and current I_o is shown in figure 19.

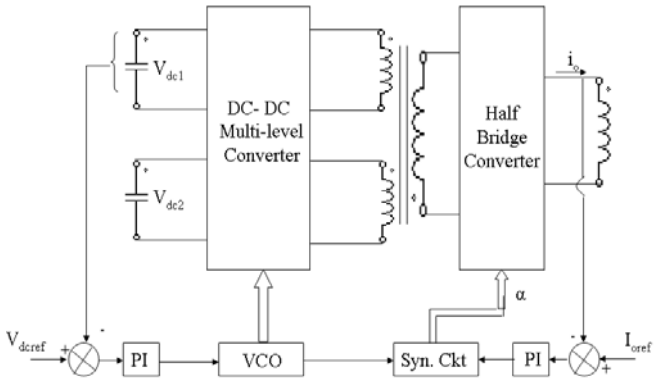

Fig 15: Control scheme for DC-DC converter

The effective charging of the current with the balancing of the voltage are taking the place. The voltages on these capacitors are set to a value of 500 volts and 300 volts and charging starts from the zero current in the coil. The final steady state is achieved where both the capacitors are having same voltages. This voltage is 40 volt. The current increases in the coil up to the value of 550 amps.

Table 1: Simulation parameters

C_{d1} ,C_{d2}	$20e^{-2}$ F	V_{d1}- Volts	300
L	0.1 H	V_{d2} -Volts	500
C_1-C_8	$10\ e^{-4}$	I_o -Amps	0-1000
Sw. Freq.	50 Hz	Thy. pulse width	20^o
Tr-leakage inductance (Primary)	0.0001	Tr-leakage inductance (Secondary)	0.00001

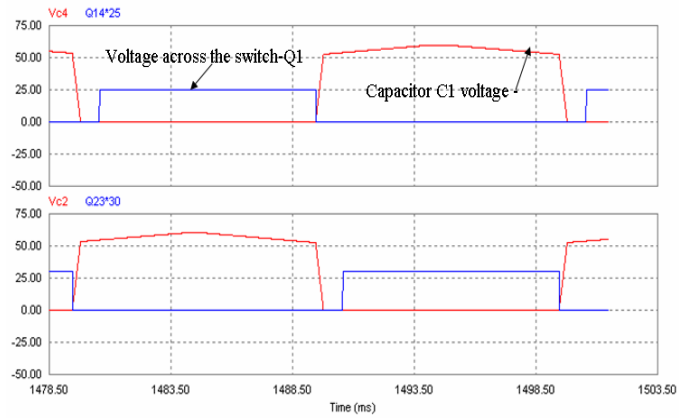

Fig 16: Voltages across the switch Q1 and capacitor C1-A ZVS operation

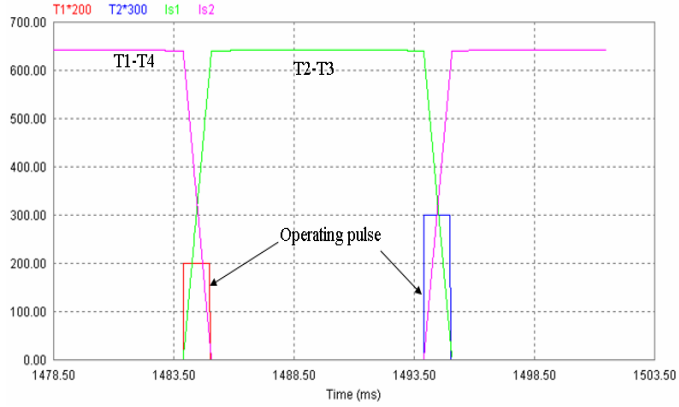

Fig 17: Currents through the thyristor- T1 and T4 snd T2-T3 (ZCS operation)

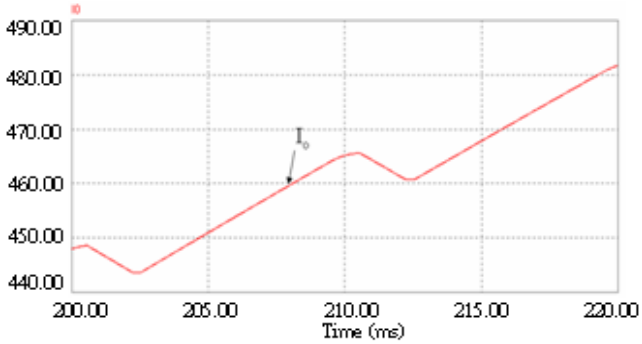

Fig 18: Coil charging-charging period is more than discharging

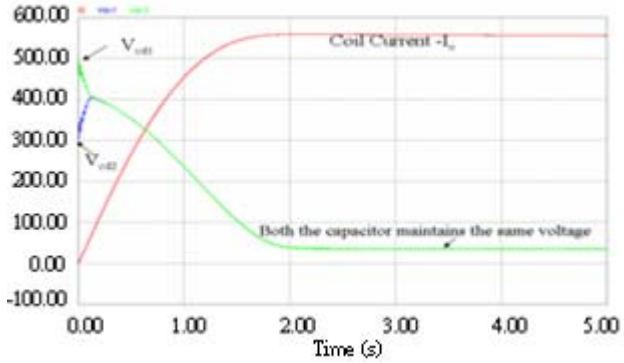

Fig 19: Capacitors voltages are balancing with the charging coil current

VI. CONCLUSION

In multi level DC-DC converters, voltage across the DC bus is more sensitive and often interferes in its operation. This paper presents the analysis of the voltage balancing at the dc bus of multi- level converters. The high power converter design with selection of circuit parameters is also presented. The operation of the circuit indicates the multi-level dc-dc converters gets balance with the appropriate switching of the H-bridge. The control scheme proposed also regulates the coil current. The new adaptive current controlled auto balancing is implemented to get stable operation of multilevel DC-DC converter. This converter works in soft switching mode hence over all efficiency and operating stability is ensured with more economical design. This has applications in interfacing of superconducting magnetic energy storages to be interfaced with the power system.

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