Design and Development of an Optimal Capacitor Charger

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Abstract – With coupled inductances, we can load a capacitor placed in parallel with the secondary inductance by the transfer of magnetic energy stored in the primary inductance (flyback principle). Calculations have shown that the time required to the complete energy transfer decreases with the incremental initial value of the voltage between the terminals of the capacitor. That behaviour has led us to model a simple circuit (based on the NE555) which allows minimizing dead time between the command pulses of the switching transistor in order to optimize the speed of the charge. For this optimization only the sensing of the capacitor voltage is needed. The simulation of the model allowed us to confirm the theoretical estimations. The experimental results are in good agreement with those obtained by the simulation performed by MicroSim Relase 8 which constituted a validation of our model.

Keywords – Flyback, capacitor charger, energy-storage capacitor, flash lamp pumping.

I. INTRODUCTION

The capacitor discharge is a widely used technique in excitation systems, especially for those intended to excite pulsed lasers and plasma-based systems [1]. With the development of new efficient semiconductor components, such as IGBTs (Isolated Gate Bipolar Transistor), capacitor charger systems become solely based on the principle of SMPS (Switch Mode Power Supply). Many previous works have been achieved in this context with various topologies. The latter mainly consist of forward configuration, Full bridge configuration [2-3], H-bridge configuration [4-5] and flyback configuration [6].

We have also opted for a flyback configuration, where the primary and the secondary excitation current are uncoupled. Indeed the capacitor charge results from energy transfer. Unlike Sokal [6], we have chosen a system with a complete energy transfer. The minimization of the time between the command pulses of the switching transistor is based on a relationship predetermined analytically and carried out with a simple an intelligent circuit based on a NE555. For this control, only the sensing of the capacitor voltage is needed. That avoids difficulties and perturbations inherent to secondary current measurement. The discrete pulse number allowing the load of the capacitor is determined according to the energy value transferred per pulse, the loading duration and the total energy to load. Our system stops the charge when this one reaches a predetermined value. Also our charging system doesn't need an auxiliary wending to detect the demagnetization of the transformer core and the driving circuit doesn't need a soft-start feature as a conventional driving circuit.

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II. FUNDAMENTAL RELATIONS

The basic flyback circuit is given in Fig 1. [7]

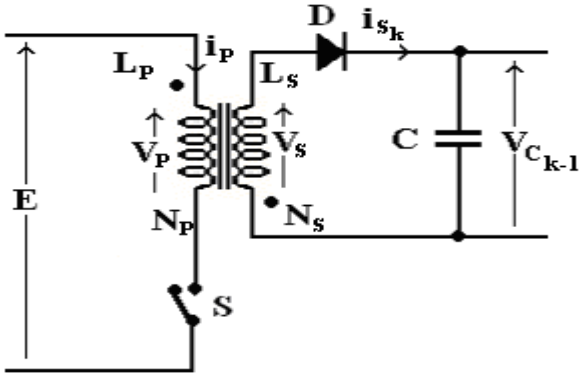

Fig. 1: Flyback circuit

The primary current pulse i_p, the secondary current pulse i_{sk}, the switching command pulses V and the voltage of the capacitor C are respectively represented in Fig 2.

The variation of the primary current flowing through the primary winding of the transformer writes:

$$i_P(t) = I_{P\max}\frac{t}{\tau} \tag{1}$$

where I_{Pmax} is the maximum primary current, t is the time and τ is the pulse command width of the switching transistor (S) as shown in figure 2.

The maximal primary current is:

$$I_{p\max} = \frac{E}{L_P}\tau \tag{2}$$

where E is the rectified and filtered main power voltage and L_P is the primary inductance.
The secondary current varies according to the relationship:

$$i_{S_k}(t) = I_{S\max}\cos(\omega_0 t) - \frac{V_{C_{k-1}}}{Z}\sin(\omega_0 t) \tag{3}$$

with:

$$\omega_0 = \frac{1}{\sqrt{L_S C}}, \quad Z = \sqrt{\frac{L_S}{C}}$$

where I_{Smax} is the maximum secondary current, L_S is the secondary inductance, C is the storage capacitor, Vc_{k-1} is the storage capacitor voltage and the index k is an integer and corresponds to the k^{th} pulse.

The transfer of the stored energy in the magnetic circuit towards the capacitor C is complete when the secondary current is cancelled. We can thus deduce the needed time for the energy transfer from a pulse to another as follows:

$$\Delta t_k = \frac{1}{\omega_0}\,arctg\left(\frac{Z\cdot I_{S\max}}{V_{C_{k-1}}}\right) \tag{4}$$

We notice that Δt_k decreases as $V_{C_{k-1}}$ increases.

For: $(Z \cdot I_{S\,max}) << V_{C\,k-1}$, equation (4) becomes:

$$\Delta t_k = \frac{1}{\omega_0}\left(\frac{Z \cdot I_{S\,max}}{V_{C_{k-1}}}\right) \quad (5)$$

The evolution of $V_{C\,k}$ from pulse to pulse is given as:

$$V_{C_k} = \frac{Z \cdot I_{S\,max}}{sin\left[arctg\left(\frac{Z \cdot I_{s\,max}}{V_{C_{k-1}}}\right)\right]} \quad (6)$$

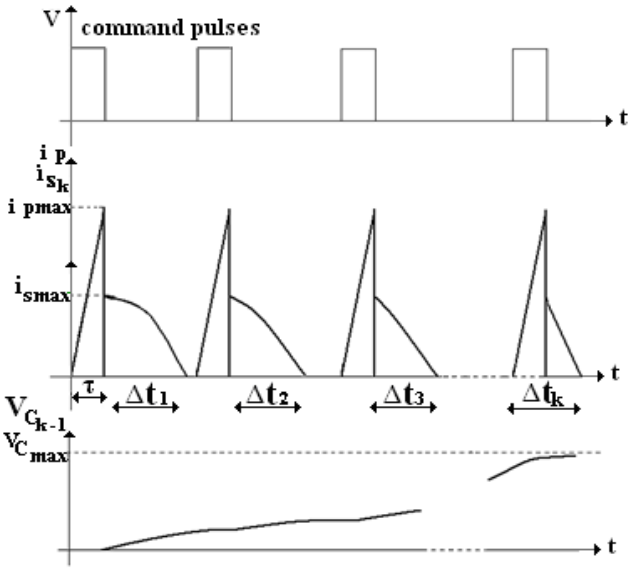

Fig. 2: Temporal variation of the primary current pulses, the secondary current pulses and the voltage of C.

As shown in Fig 2 the necessary time to the cancellation of the secondary current decreases from a pulse to another. To allow the complete demagnetization of the transformer's secondary winding for the first pulse we must choose a period great or equal to $(\Delta t_1 + \tau)$. But if we use this fixed period the lost time would increase between the next pulses and the load of *C* would be slowed down. To solve this problem we had to minimize this dead time, in other way to compress these command pulses.

III. MODELLING

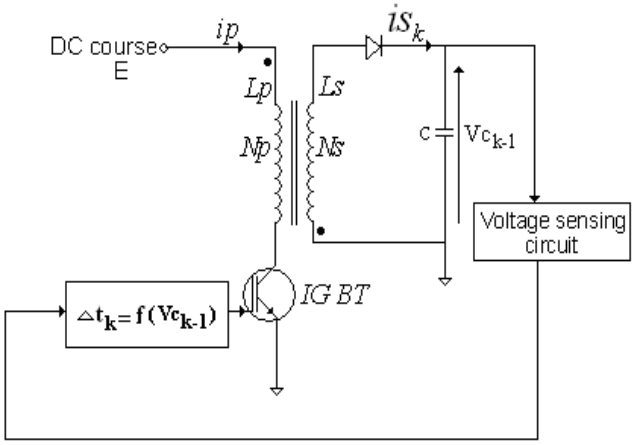

Fig. 3: The Synoptic scheme of the system.

The purpose is to design an electronic circuit which supplies pulses to the switch depending on the voltage load capacitor. The low level width of these pulses has to vary in the same manner as the time necessary to cancellation of the secondary winding current. The scheme of this system appears in Fig 3.

The circuit which allows following the variation of Δt_k in terms of $V_{C\,k-1}$ is given in Fig 4.

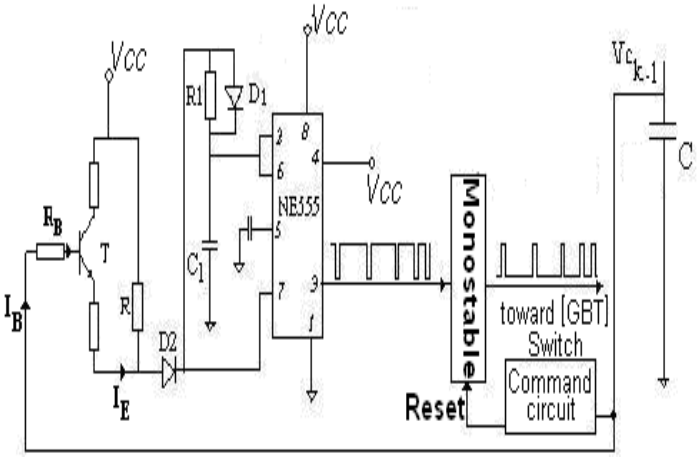

Fig. 4: The scheme of the pulses compression circuit.

The designed circuit is based on a NE555 assembled in astable. The values of the components *R*, R_1 and C_1 (Fig 4) were calculated so that the period of the control signal (low level for Vc_0=0V) performs a complete demagnetization of the secondary winding during the first energy transfer. The capacitor C_1 discharges through R_1 resistance during a fixed time representing the low level of the pulses at the output of the NE555, while the time of load of C_1, which represents the high level, is modulated by sensing the storage capacitor voltage of *C*. The signal obtained at the output of the NE555 attacks the entry of the monostable of precision that provided the control signal to the switch having constant high level to fix the I_{Pmax} value and variable low level which follows the time of cancellation of the secondary current. This circuit also makes it possible to stop the load of *C* when this one reaches a predetermined value by blocking the monostable. As we see it on Fig. 4, the output voltage Vc_{k-1} controls the base current of the transistor (T) through the feedback resistor R_B. The emitter current charges the capacitor C_1 of NE555. This transistor constitutes a current generator and can be schematized as in Fig 5. The calculation of the necessary time to charge the capacitor C_1 of NE555 between 1/3 and 2/3 of supply voltage of the circuit *Vcc* gives the following relationship:

$$\Delta T_k = R \cdot C_1 \cdot Ln\left(1 + \frac{1}{1 + \frac{3 \cdot R \cdot \beta \cdot V_{C_{k-1}}}{V_{CC} \cdot R_B}} - 6\frac{V_D}{V_{CC}}\right) \quad (7)$$

where V_D is the threshold voltage of the diodes D_1 and D_2 and β is the gain of the transistor (T),

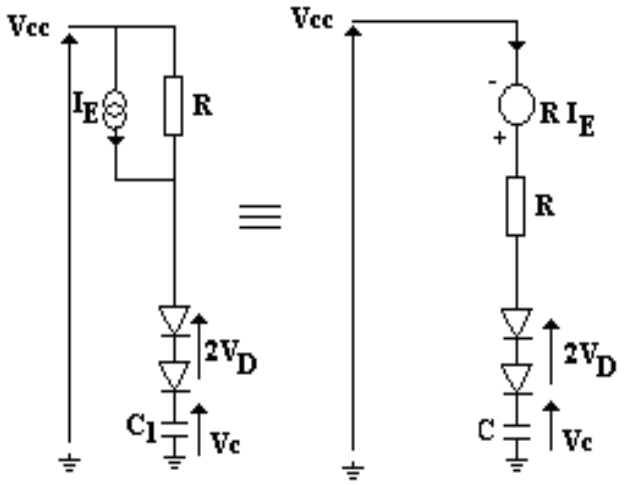

Fig. 5: The equivalent scheme of the current generator.

In the case where:

$Vc_{k-1} >> 6.V_D \frac{R_B}{3.R.\beta}$, the first term of the series expansion of relation (7) gives the new relation:

$$\Delta T_k = \frac{R.C_1}{1 + \frac{3.R.\beta.Vc_{k-1}}{Vcc.R_B} - \frac{6.V_D}{Vcc}} \tag{8}$$

In order to determine the value of the resistor R of the NE555 circuit, we rewrite the equations (4) and (7) for k=1 (Vc_{k-1}=Vc_0=0V).
The new equations are:

$$\Delta t_1 = \frac{\pi}{2\omega_0} \tag{9}$$

$$\Delta T_1 = R.C_1.Ln\left[1 + \frac{1}{\left(1 - 6.\frac{V_D}{Vcc}\right)}\right] \tag{10}$$

Equalising equations (9) and (10) we have:

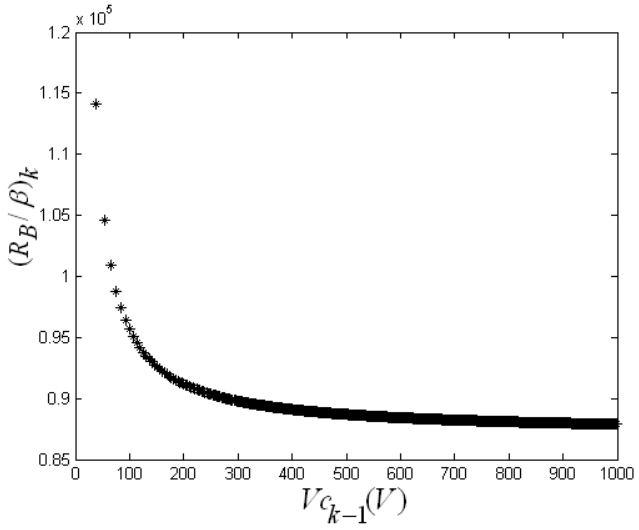

Fig. 6: The variation of $\left(\frac{R_B}{\beta}\right)_k$ versus $V_{C_{k-1}}$

$$R = \frac{\pi}{2.\omega_0.C_1.Ln\left[2 - \frac{6.V_D}{V_{CC}}\right]} \tag{11}$$

For a fixed value of C_1 we calculate the R value.

Also from equalising equations (5) and (8) results the following expression:

$$\left(\frac{R_B}{\beta}\right)_k = \frac{Z.I_{smax}.3.RV_{C_{k-1}}}{(\omega_0.R.C_1.VccV_{C_{k-1}} - Z.I_{smax}Vcc + 6V_D.Z.I_{smax})} \tag{12}$$

Fig 6 represents the variation of $\left(\frac{R_B}{\beta}\right)_k$ in terms of $V_{C_{k-1}}$.

We notice on figure 6 that after a certain load voltage the ratio $\left(\frac{R_B}{\beta}\right)_k$ tends to be constant. By choosing a transistor with a known gain β we calculate the correspondent value of R_B.

The curve of both Δt_k and ΔT_k (using equations (4), (6) and (7)) versus $V_{C_{k-1}}$ for $\left(\frac{R_B}{\beta}\right)_k = 10^5$ kΩ, is represented in figure 7.

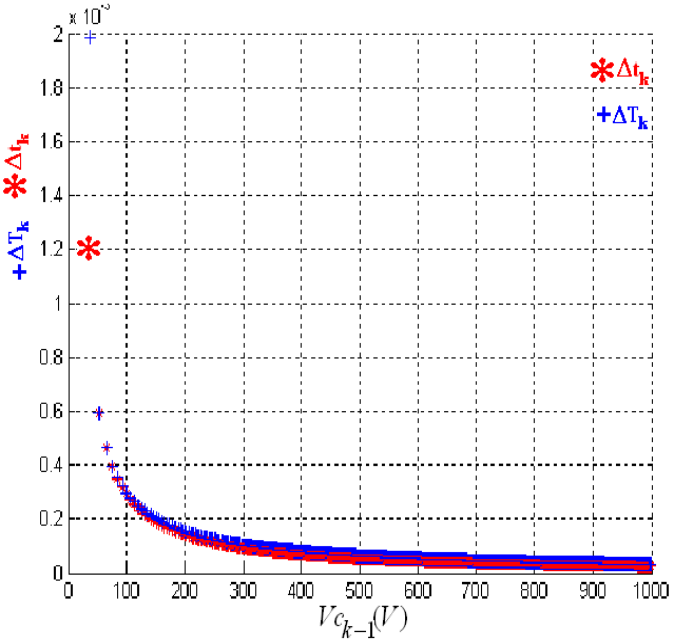

Fig. 7: Variation of Δt_k and ΔT_k versus $V_{C_{k-1}}$.

We notice on this figure that the two curves coincide that prove the efficiency of our model.

We can see clearly from the Fig 8 that the pulses compression makes the capacitor charging faster.
The curves represented in Figs 6, 7 and 8 were plotted by using the software Matlab.

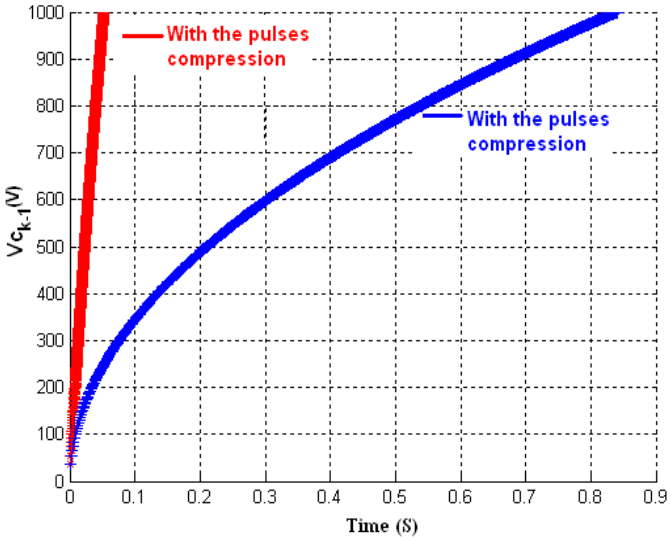

Fig. 8: Capacitor charging with and without pulses compression.

IV. SIMULATION

The proposed circuit was simulated with MicroSim Relase 8 software. The obtained results are given in the following figures.

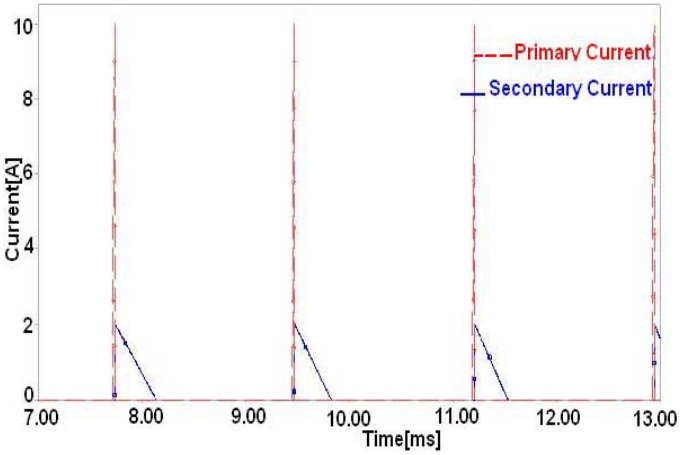

Fig. 9: The primary and secondary currents without pulses compression.

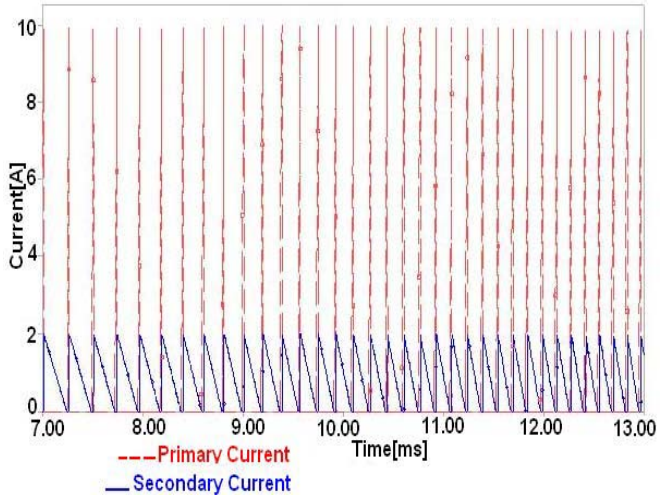

Fig. 10: The primary and secondary currents with pulses compression.

Figs 9 and 10 show the variation of the primary and secondary currents without and with pulses compression.

These figures point out clearly the advantage of our circuit, which consists of practically complete delete of the dead time.

We can also see this advantage in the charging process in Fig 11 where the charge is becoming faster.

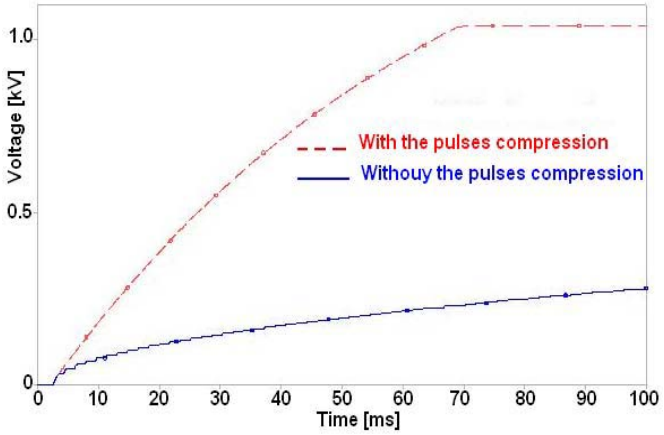

Fig. 11: The capacitor charging with and without pulses compression.

The curves of the Figs 6, 7, 8, 9, 10 and 11 were obtained with the following parameters value:
L_S =14.3 mH, I_{Pmax}=10A, I_{Smax}=2A, C=40µF, $C1$=82nF, V_D =0.6V V_{CC}=12V, $\left(R_B/\beta\right)_k$ =10^5 kΩ.

V. EXPERIMENTAL RESULTS

Figs 12 and 13 show the experimental results for an input voltage of 220 Vac. These results are obtained with and without the pulses compression. As soon as the 1kV charge value is reached, the system stops the charging process. One has to note that these experimental results are in good agreement with that of simulation. The storage capacitor voltage was measured using a Tektronix scope and probe with attenuation setting of 1000. Therefore the scaling factor of this measure is 200V/div. We can note also that reducing the dead time between the commands pulses of the switching transistor makes the time of the capacitor charging faster.

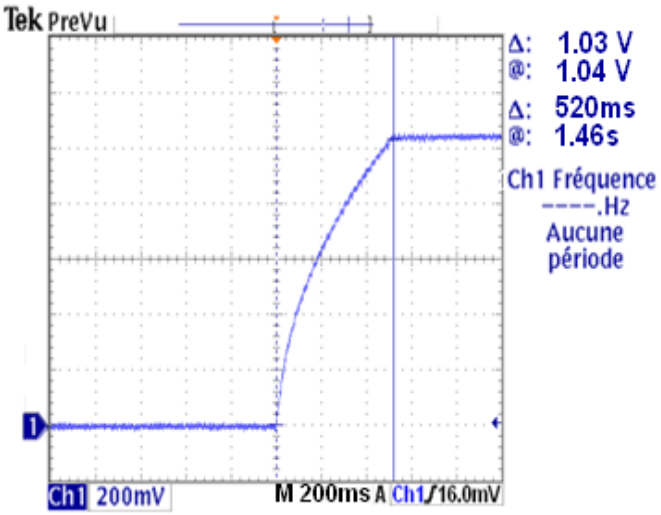

Fig. 12: The capacitor charging without pulses compression.

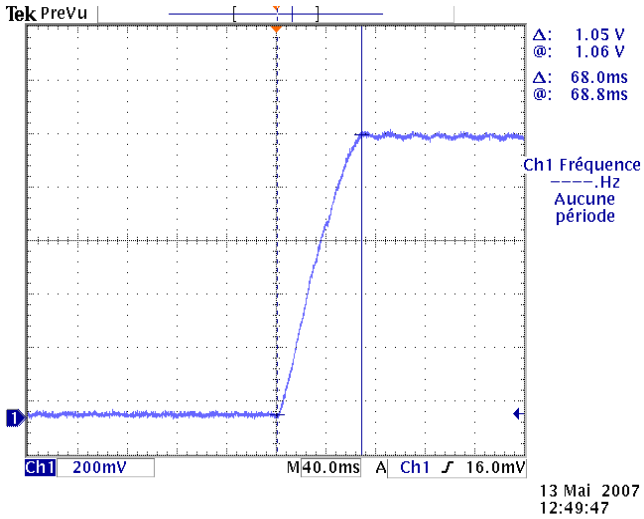

Fig. 13: The capacitor charging with pulses compression.

Figs 14 and 15 give the experimental wave forms of the primary and secondary currents using a resistor of 0.1 Ω in series with the primary and secondary windings.

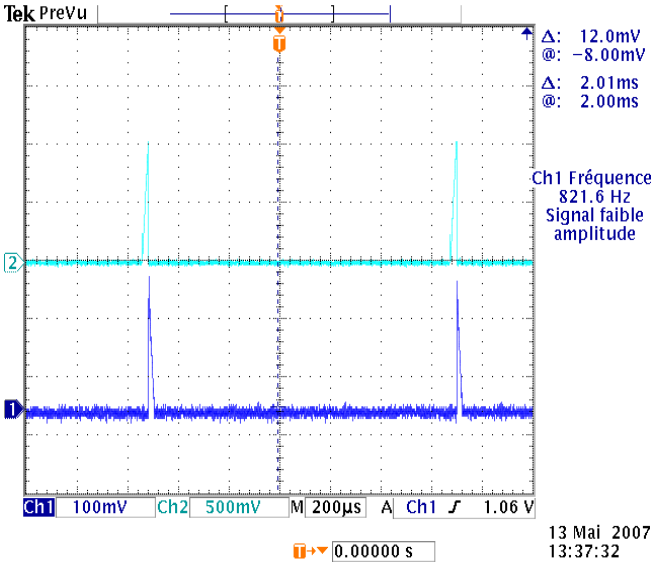

Fig. 14: The primary current (upper trace) and secondary current (lower trace) without pulses compression.

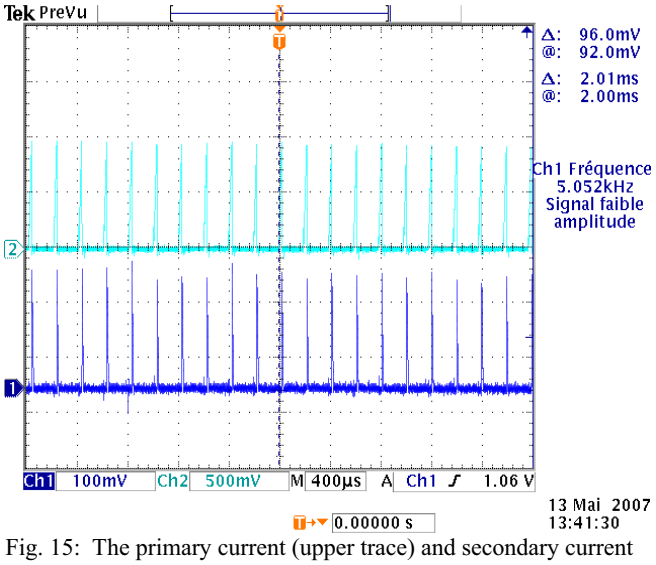

Fig. 15: The primary current (upper trace) and secondary current (lower trace) with pulses compression.

Figs 16 and 17 show the IGBT driving signal (the switching command pulses) with and without the command pulses compression.

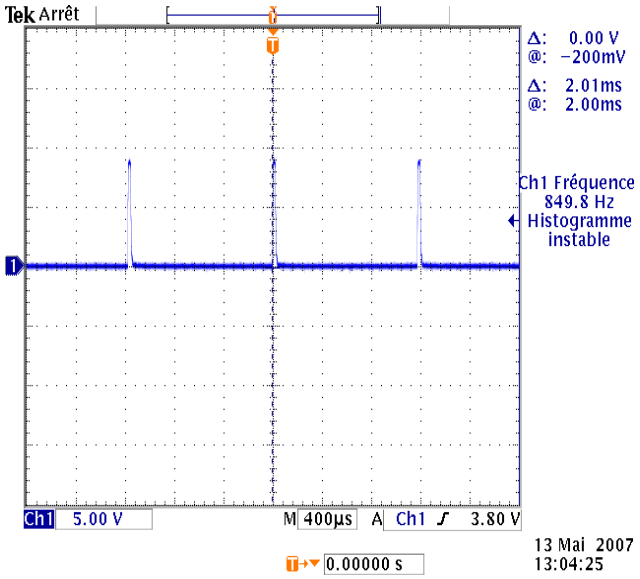

Fig. 16: The IGBT driving signal without pulses compression.

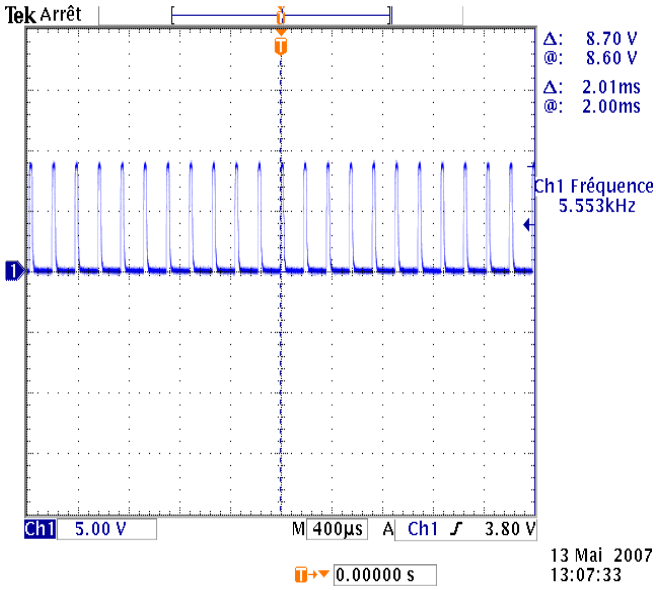

Fig. 17: The IGBT driving signal with pulses compression.

VI. Conclusion

We developed a simple method that allowed us to optimise the capacitor charging time. This system need only the sensing of the capacitor voltage during the charging process in order to drive the switching transistor by the use of a simple and intelligent command circuit.
Our charging circuit has been validated by both simulation and experiment. For application the charge of a capacitor of 40µF up to a voltage of 1kV in 68 ms allowed us to supply a xenon flash lamp for pumping a solid-state laser at a repetition rate of 10 Hz.

For more power we can put in parallel several modules identical to that shown in Fig 3.

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BIOGRAPHIES

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