Modeling and Analysis of Conducted EMI Emissions of a Single-Phase PWM Inverters

D. Anand[1] S. Jeevananthan [2]

Abstract - In this paper, the analysis of conducted electromagnetic interference (EMI) from single-phase pulse width modulated (PWM) inverter is presented. The simple equivalent circuit model of the inverter is used for this purpose. The causes for conducted emissions are identified. Also simulated results of conducted noise in the single-phase SPWM inverter for various circuit conditions are presented.

Keywords - Conducted EMI, electromagnetic compatibility (EMC), parasitics, PWM inverters.

I. INTRODUCTION

The significant advancements in power electronics have led to improve the performance of converters and have enlarged their application area. All equipments comprising switching power processors generate and emit high frequency noises. This high frequency noises can interfere with nearby sensitive electronic components, called electro-magnetic interference (EMI). EMI can cause unpredictable degradation in the performance of any equipment. There are two modes of propagation of EMI emissions, one is *conducted* EMI emission (ranging from 15 kHz-30 MHz) and the other is *radiated* EMI emissions (ranging from 30MHz-10GHz). The frequency range of EMI signals generated by power electronics equipments extend to about 1GHz [1]. The widespread use of PWM inverters is now one of the major sources of the increasing electromagnetic pollution. PWM inverters require high-speed switching devices such as MOSFETs, IGBTs etc to achieve high performance in dynamic response and efficiency with reduced acoustic noise, size and weight. It is commonly realized that high switching *dv/dt* and *di/dt* are the main sources of EMI noise [2]. To secure an interference-free environment, the engineering discipline of Electromagnetic Compatibility (EMC) has been developed. The regulatory authorities viz. CISPR, IEC, VDE, FCC, and military standards, have various standards and regulations, which specify the maximum limit on the conducted and radiated noises [3].

The PWM inverters may operate at under different modulation index (m_a), modulation frequency (m_f), supply voltage and load current. The variation in any one of the control parameters mentioned above has direct influence in EMI effects. If there is any accountability of EMI both in conducted and radiated propagations are available for any PWM inverter, it will be useful for the designer to decrease post development modifications for EMI compliance, which is very costly at later stages.

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The general approach to analyze EMI caused by power semiconductors is circuit simulation based on the parasitics extraction. Because of the complexity in the inverter circuits, the extraction of parasitics becomes impracticable in some cases. Further more, R-L-C network is not enough to indicate the propagation characteristics of nonlinear components (such as inductance with core, digital circuit, semiconductor components, etc.) in the equipments. Many researchers used transfer impedance or transfer function approach to analyze conducted emissions of the inverters. To avoid complicated models, a simple mathematical approach to identify the cause for conducted emissions is proposed in this paper [5].

This paper describes the understanding of conducted EMI emission levels in full-bridge PWM inverter circuit. The mathematical models are proposed for solving the EMI problems in converter by analyzing the transient responses of current and voltage waveforms. In addition, this paper explains and compares the simulation results of single-phase SPWM inverter under various modulation index (m_a), modulation frequency (m_f), and supply voltage using IsSpice (Intusoft, USA) and Orcad simulation softwares.

II. CONDUCTED EMI

There are two principle propagation modes for conducted EMI; differential mode (symmetrical) and common mode (asymmetrical). The propagation of differential mode EMI takes place between conductor pairs, which form a conventional return circuit, e.g., the line phase and neutral conductors. The propagation of common mode EMI takes place between group of conductors and either ground or another group of conductors. The differential mode EMI is the direct result of the fundamental operation of the switching power processors: the pulsating switching current, or at least a small portion of it, flows in the power line. The origin of the common mode EMI is either electrical or magnetic.

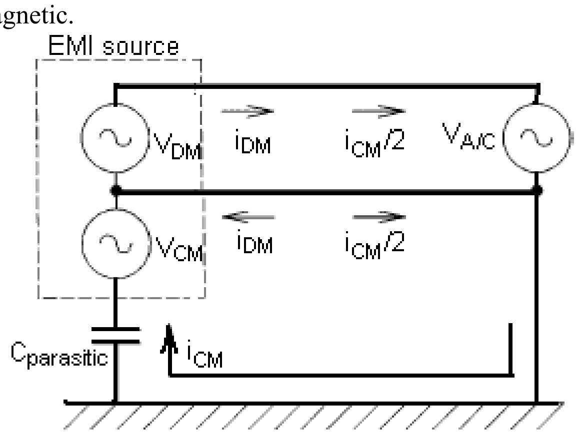


Fig. 1: Propagation of conducted EMI

EMI is generated electrical when a circuit conductor with a large *dv/dt* has a significant parasitic capacitance to ground.

Magnetically generated common mode EMI appears when circuit loop with large *di/dt* in it has significant mutual coupling to a group of nearby conductors [2]. The propagation path for conducted EMI is shown in the Fig. 1, representing the equivalent differential and common mode noise voltages and their respective currents.

III. Full- Bridge Inverter

The conventional full- bridge inverter without parasitic is shown in Fig. 2. The switching current and voltage waveforms during turn-on and turn-off of the MOSFET for the non parasitic case is shown in Fig.3 and Fig.4.These waveforms do not have ringing on themselves.

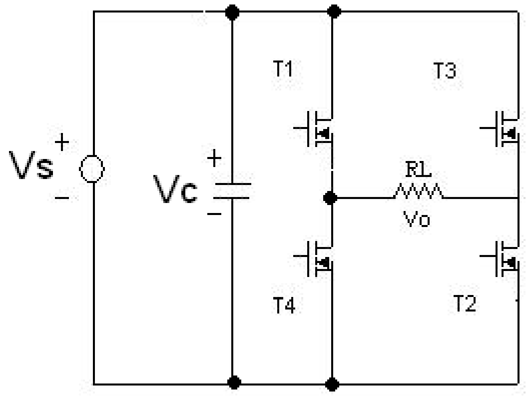


Fig. 2: Full-Bridge inverter

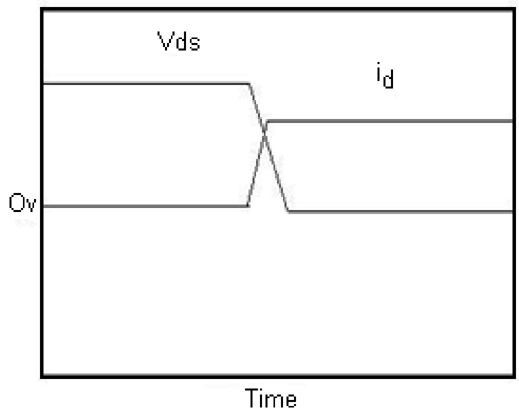


Fig. 3: Voltage and current waveform during typical turn- on

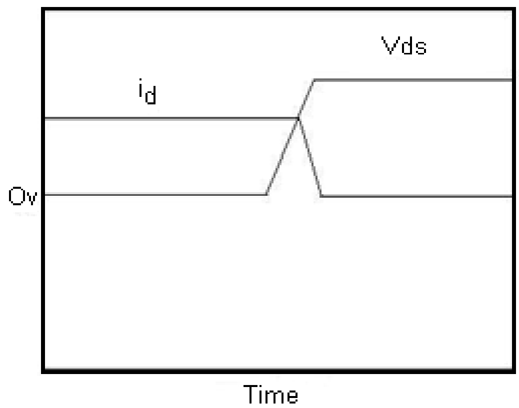


Fig. 4: Voltage and current waveform during typical turn- off

In the above shown waveforms there is no ringing in the switching current and voltage due to the absence of parasitics, but in practical case it is unavoidable to include the parasitics of wiring, switches etc.

IV. Proposed Model

The proposed model of single-phase full–bridge inverter with parasitic elements is shown in Fig. 5. The second order equation is used in this model for magnifying the small signal over the current and voltage waveforms [7]. The analysis is divided into two parts; one is for turn-on state and the other is for turn-off state. The direction of arrow indicates the direction of flow of current during the positive half cycle of the output voltage.

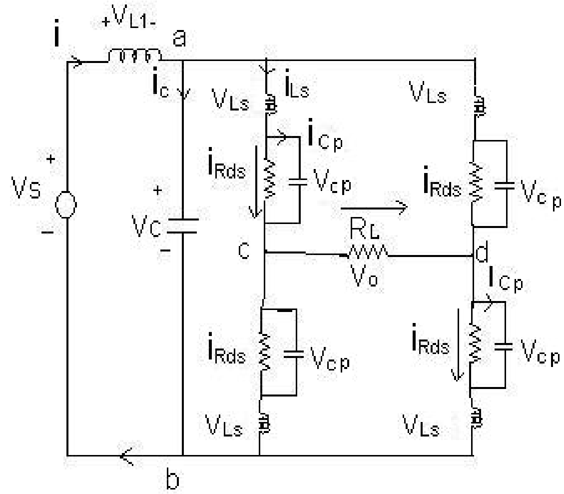


Fig. 5: Proposed model

where, L_1 is the stray inductance between source and input capacitance, L_s is the stray inductance of the wiring, R_{ds} is the drain-source resistance of the switch, C_p is the shunt parasitic capacitance.

V. Model Analysis

The mathematical model of switching current and voltage waveforms are obtained as follows.

Appling KVL to loop ab, we get

$$V_s = v_{L1} + v_c \tag{1}$$

Applying KVL to acdb loop, we get

$$v_c = v_o + 2 * v_{cp} + 2 * v_{Ls} \tag{2}$$

$$v_c = 2L_s \frac{di_{Ls}}{dt} + 2v_{cp} + i_{Ls} * R_L \tag{3}$$

Applying KCL to the model, we get

$$i_{Ls} = i_{Rds} + i_{Cp} \tag{4}$$

$$i = i_c + i_{Ls} \tag{5}$$

Since

$$i_{Rds} = v_{cp} / R_{ds} \tag{6}$$

and

$$i_{cp} = C_p \frac{dv_{Cp}}{dt} \tag{7}$$

v_{cp} is related to i_{LS} through,

$$i_{LS} = \frac{v_{cp}}{R_{ds}} + C_p \frac{dv_{Cp}}{dt} \tag{8}$$

Assuming identical wire and device parasites,

$$v_{cp} = \frac{v_c}{2} - L_S \frac{di_{LS}}{dt} - \frac{v_o}{2} \tag{9}$$

A. Voltage across Parasitic Capacitance

To find $v_{Cp(t)}$, substitute equation (8) in (9)

$$v_{Cp} = \frac{v_C}{2} - L_S \frac{d}{dt}\left[\frac{v_{Cp}}{R_{ds}} + C_p \frac{dv_{Cp}}{dt}\right] - \frac{v_O}{2} \tag{10}$$

$$\frac{d^2 v_{Cp}}{d^2 t} + \frac{dv_{Cp}}{R_{ds} C_p dt} + \frac{v_{Cp}}{L_S.C_p} = \frac{v_C - v_O}{2L_S C_p} \tag{11}$$

Case 1- Natural response: Since the excitation equals to zero by definition of natural response, denoted as $v_{cp}\ (t)$, so set $f(t) = 0$ to obtain hom**ogeneo**us equation,

$$S^2 + \frac{S}{R_{DS} C_p} + \frac{1}{L_S.C_p} = 0 \tag{12}$$

$$S_1, S_2 = -\frac{1}{2R_{DS}.C_p} \pm \sqrt{\left(\frac{1}{2R_{DS}C_p}\right)^2 - \frac{1}{L_S C_p}} \tag{13}$$

Case 2- Forced response: Due to $f(t)$ = constant value, the forced response is denoted as V_{coF}. Substitute $v_{CpF} = k$ in equation (11) to obtain

$$\frac{d^2 k}{dt^2} + \frac{1}{R_{DS} C_p}\frac{dk}{dt} + \frac{k}{L_S C_p} = \frac{v_C - v_O}{2L_S C_p} \tag{14}$$

$$\frac{k}{L_S C_p} = \frac{v_C - v_O}{2 L_S C_p} \tag{15}$$

Hence, the result of forced response is

$$k = \frac{v_C - v_O}{2} \tag{16}$$

B. Current through Wire Inductance

To find $i_{LS}(t)$, substitute equation (9) in (8)

$$\frac{d^2 i_{LS}}{dt^2} + \frac{di_{LS}}{C_p R_{ds} dt} + \frac{i_{LS}}{C_p L_S} = \frac{v_C - v_O}{2R_{ds} C_p L_S} \tag{17}$$

Case1-Natural response: To find natural response; denoted $i_{LS}\ (t)$, so set $f(t) = 0$, to obtain homogeneous equation,

$$S^2 + \frac{S}{R_{DS} C_p} + \frac{1}{L_S.C_p} = 0 \tag{18}$$

$$S_1, S_2 = -\frac{1}{2R_{DS}.C_p} \pm \sqrt{\left(\frac{1}{2R_{DS}C_p}\right)^2 - \frac{1}{L_S C_p}} \tag{19}$$

Case 2 -Forced response: To find forced response, i_{LSF}, substitute $i_{LSF} = k$ in equation (17)

$$\frac{d^2 k}{dt^2} + \frac{1}{R_{DS} C_p}\frac{dk}{dt} + \frac{k}{L_S C_p} = \frac{v_C - v_O}{2R_{ds} L_S C_p} \tag{20}$$

Hence, the result of forced response is

$$k = \frac{v_C - v_O}{2R_{ds}} \tag{21}$$

C. Complete Response

Mode 1: Switches T1 and T2 turned on, the complete response is given by,

$$i_{LS}(t) = i_N + i_F \tag{22}$$

Therefore,

$$i_{LS}(t) = e^{\alpha t}(Ae^{\beta t} + Be^{-\beta t}) + \frac{v_C - v_O}{2R_{ds}} \tag{23}$$

Where,

$$\alpha = -\frac{1}{2R_{DS}.C_p} \tag{24}$$

$$\beta = \sqrt{\left(\frac{1}{2R_{DS}C_p}\right)^2 - \frac{1}{L_S C_p}} \tag{25}$$

The voltage across the switch, when it is turned on, is

$$v_{Cp}(t) = i_{Cp}(t) * R_{ds} \tag{26}$$

Mode 2: Switches T1 and T2 turned off, the complete response, $v_{Cp}(t) = v_N + v_F$ so,

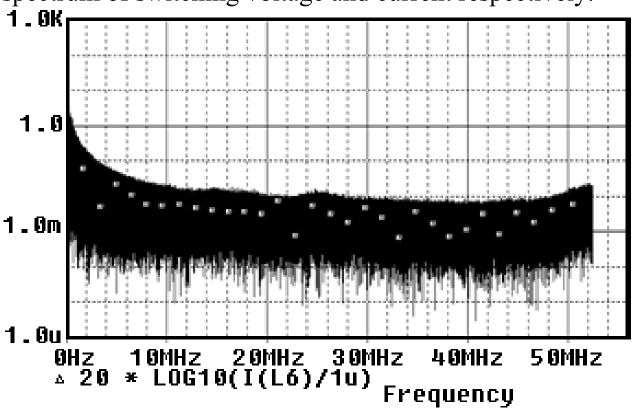
$$v_{Cp}(t) = e^{\alpha t}(c\cos\beta t + D\sin\beta t) + \frac{v_C - v_O}{2} \tag{27}$$

The current through the switch when it is turned off is Rds on/off

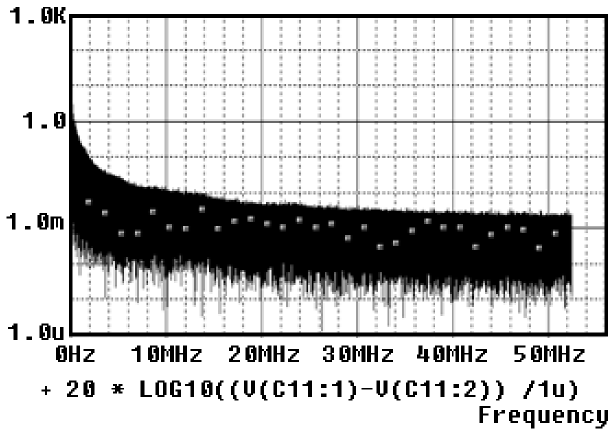
$$i_{LS}(t) = v_{Cp}(t) / R_{ds} \tag{28}$$

VI. Model Validation

The mathematical model has been validated through simulation of single-phase SPWM inverter in PSPICE package for switching voltage, current and conducted EMI. The representative simulation results are given for the switching frequency of 40 kHz in the Fig. 6(a) and 6(b), the spectrum of switching voltage and current respectively.



(a)



(b)

Fig. 6: The simulation results (Orcad)
(a) Spectrum of current waveform and (b) Spectrum of voltage waveform

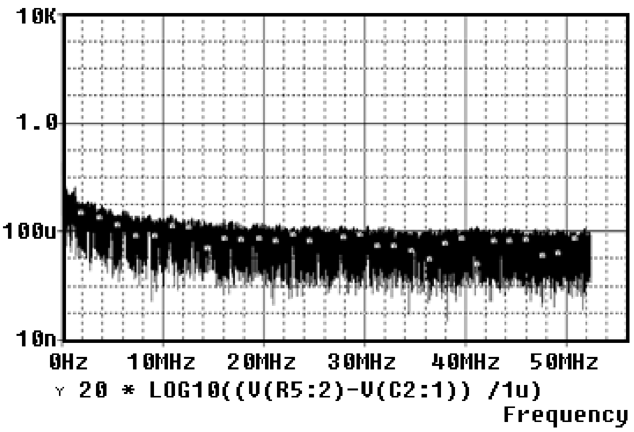


Fig. 7: The simulation results from **PSPICE** for EMI

The Fig. 7 shows the simulated result conducted EMI in the single-phase SPWM inverter. Comparing Fig.6 and Fig.7, the peak of the spectra of switching waveforms and EMI are at same frequency. So it is confirmed that high switching *dv/dt* and *di/dt* are the main sources of EMI noise. The damping frequencies of the switching voltage and current waveforms are changed by the resonant frequency of additional inductance and capacitance.

VII. SIMULATION RESULTS

Simulation of Conducted EMI emission is also done using ICAP software. The main window with simulation circuit is shown in Fig. 8.

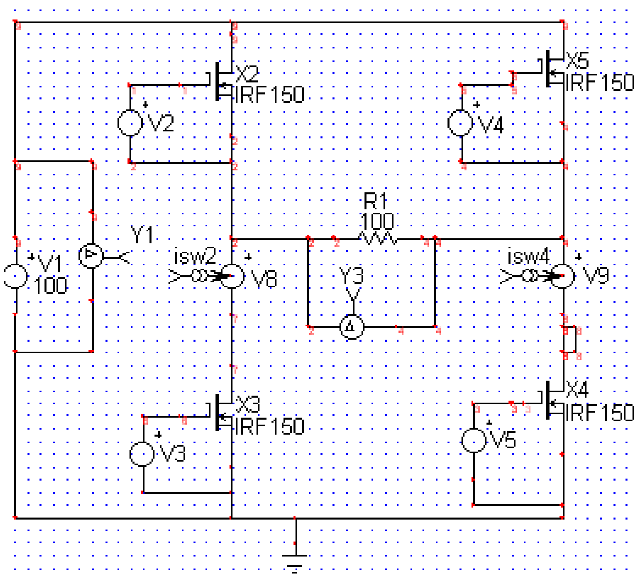


Fig. 8: ICAP simulation circuit for conducted EMI

The simulation for conducted EMI using ICAP software is one of the effective ways for analyzing the EMI. The simulation studies are conducted on various circuit conditions like modulation index (m_a), modulation frequency (m_f), and supply voltage.

Different modulation frequency

The simulated waveforms for different modulating frequency (m_f), at constant source voltage, are shown in Fig. 9. The limit for conducted EMI specified by the VDE standard is 90dbµV maximum and the minimum limit of 56dbµV.

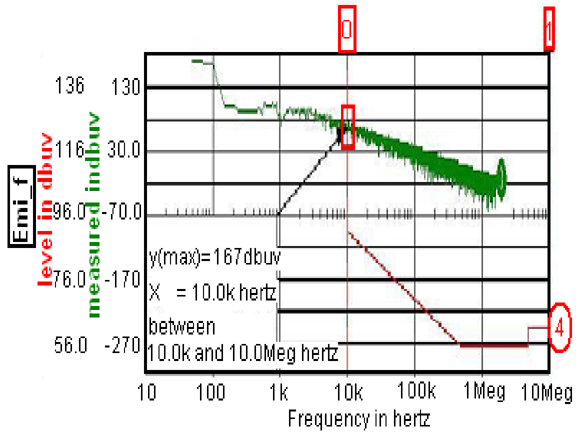


Fig. 9(a): for M_f=15

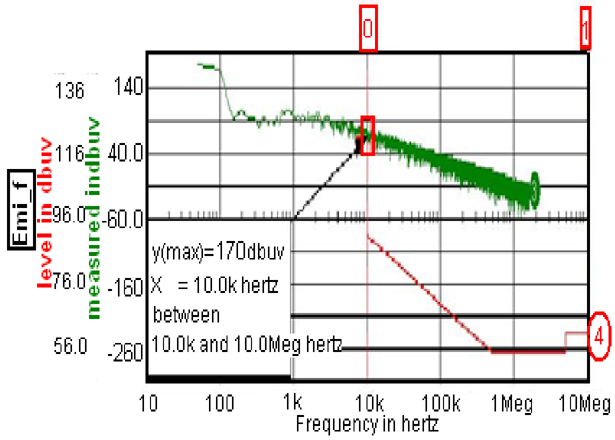


Fig. 9(b): for M_f=17

Simulation results shows that, the EMI generated by the SPWM inverter exceeds the specified limit and also it is concluded that, conducted EMI emission increases with increases with increase in switching frequency as shown in Fig.10.Also it is concluded that there is increase in range of frequencies over which the EMI generated by the inverter exceeds the limit.

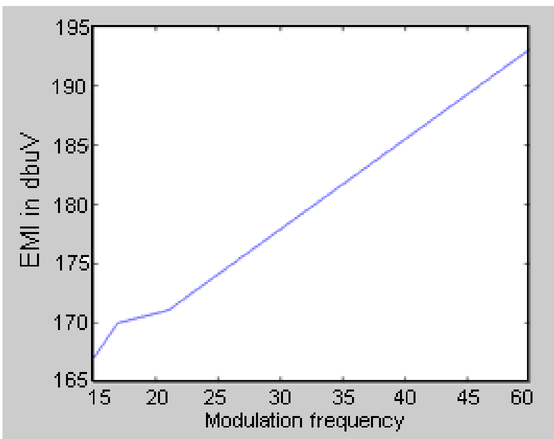


Fig.10: EMI Vs switching frequency

Case 2 Different source voltages: The simulated waveforms for different source voltage are shown in Fig. 11.

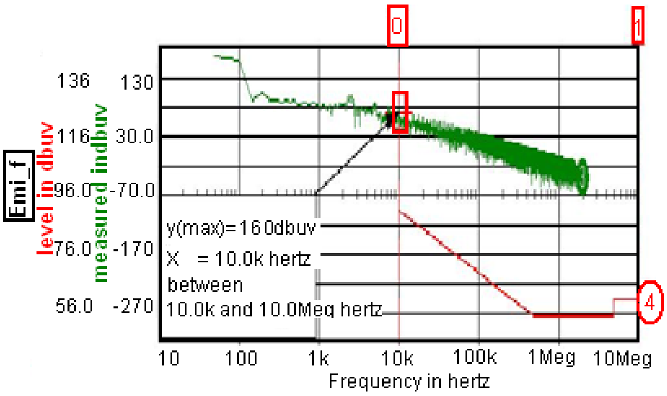


Fig. 11(a): for Vdc=100v

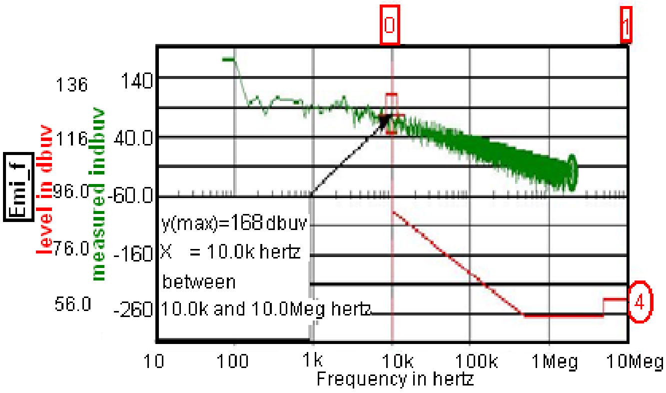


Fig. 11(b): for Vdc=250v

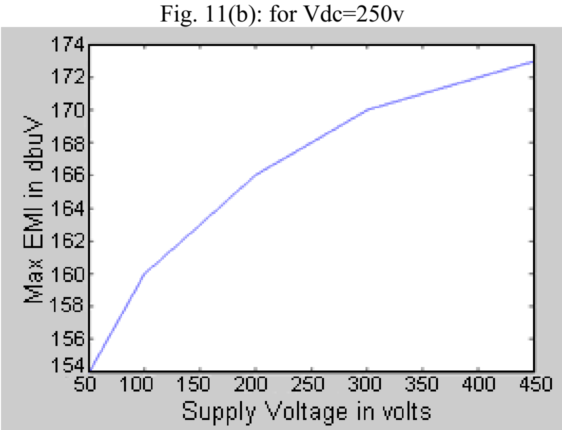


Fig. 12: EMI Vs Source voltage

From Fig. 11 and 12, it is concluded that EMI increases almost linearly with increase in source voltage.

Case 3 Different modulation indexes: The simulated waveforms for different modulation index are shown in Fig. 13.

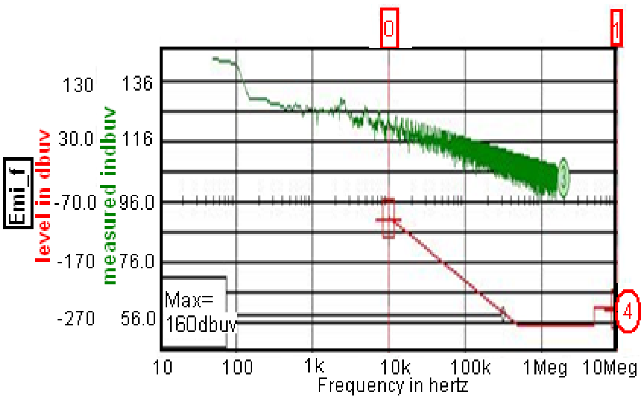


Fig.13 (a): for m_a=0.4

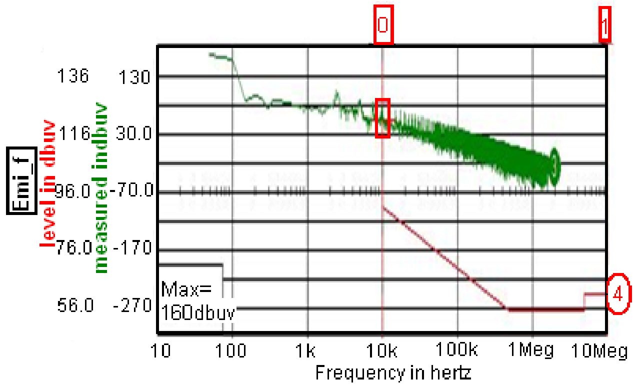


Fig. 13(b): for m_a=1

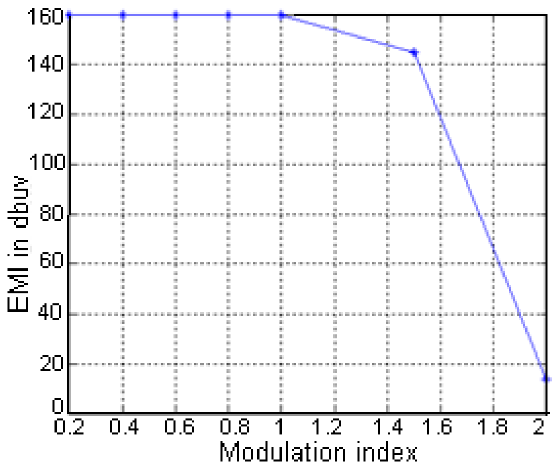


Fig.14: EMI versus Modulation index

Fig. 14 shows the plot for EMI versus modulation index, here the EMI generated by the circuit remains constant for modulation index up to 1 and decreases slowly. Hence it is concluded that EMI depends on number of switching pulses but not on the width of the pulses.

VIII. Conclusion

The mathematical model has been proposed for conducted EMI and the model has been verified in frequency domain. The mathematical model includes the effects of parasitics. The model proposed here is less complex and also helps the designer in the design stage to avoid EMI. Also the single-phase SPWM inverter is analyzed for conducted EMI under various circuit conditions.

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BIOGRAPHIES

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