Five-level NPC-VSI Capacitor Voltage Balancing Using a Novel Clamping Bridge

R. CHIBANI[1] E.M. BERKOUK[2] M.S. BOUCHERIT[3]

Abstract- A serious constraint in multilevel inverters is the capacitor voltage-balancing problem. The unbalance of the different DC voltage sources of the five-level Neutral Point Clamping Voltage Source Inverter (NPC-VSI) constituted the major limitation for the use of this power converter. To remedy to this problem, a new control solution to compensate the unbalanced DC voltages for the five-level NPC VSI is presented. It provides a fast and flexible control of the inverter capacitor voltages, leads to a simpler implementation, and present high equalization efficiency. Simulation results show the effectiveness of our methods.

Keywords- Clamping bridge, five-level , NPC VSI, Lyapunov function, Sliding mode control.

I. INTRODUCTION

In 1980, early interest in multilevel power conversion technology was triggered by the work of Nabae, who introduced the neutral-point-clamped (NPC) inverter topology [1]. It was immediately realized that this new converter had many advantages over the more conventional two-level inverter. Subsequently, the concept of the three-level converter was extended further and some new multilevel topologies were proposed.

An alternative to the diode-clamped converter, the flying capacitor topology does not have issues with clamping diodes. First proposed in 1992 [2], this approach has the advantage of a larger number of redundant switching states, which allows more freedom in balancing the clamping capacitors' voltages. The main disadvantage is the potential for parasitic resonance between the decoupling capacitors; this is made even worse by the high number of capacitors, which complicates packaging for small inductance. In addition, there are issues with voltage redistribution in the case of voltage surges. Nevertheless, the flying capacitor topology seems very promising.

The multilevel configuration with cascaded H-bridge inverters presents another alternative in the design of multilevel converters [3]. A primary advantage of this topology is that it provides the flexibility to increase the number of levels without introducing complexity into the power stage. Also, this topology requires the same number of primary switches as the diode-clamped topology, but does not require the clamping diode.

However, this configuration uses multiple dedicated DC-busses and often a complicated and expensive line transformer, which makes this a rather expensive solution. In addition, bi directional operation is somewhat difficult (although not impossible) to achieve.

Perhaps the most important improvement in cascaded converter topologies is the hybrid multilevel topology [4]. The main strength of this approach is its combination of the high voltage capacity of the relatively slow GTO devices with the high switching frequency of the lower voltage capacity IGBT devices. At the same time, the different voltage levels of the IGBT and GTO bridges create an additional voltage level without any additional complexity.

One important problem associated with the NPC inverter is its Neutral Point (NP) variation [1]. The DC link NP potential can significantly fluctuate or continuously drift to unacceptable levels due to non uniform switching device or DC link capacitor characteristics or fluctuation because of the irregular and unpredictable charging and discharging in each capacitor [5-7].

Some solutions have been proposed, which are based on redundant switching configurations [1] [8-15] or on the addition of zero-sequence voltage components to the output voltage [9].

Unfortunately, these methods modify the output voltage waveform. As the number of inverter-levels increases, the problem of capacitor balancing becomes more complex and the solution very drastic.

The unbalance DC voltage problem can also be solved by separate DC sources [6] or by adding electronic circuitry. In [16-18], clamping bridges based on transistors and resistors are proposed as a solution to this problem.

This paper deals introduces a new clamping bridge for the DC capacitor voltage equalisation has been proposed to DC-link capacitors voltages fluctuations in an NPC VSI that permits to achieve a correct capacitors voltages sharing, when conventional balancing methods compensate fail. The organization of this paper is as follows. Section 2 develops the mathematical modelling of the DC-AC converter five-level NPC-VSI and its Pulse Width Modulation control strategy (PWM) using four bipolar carriers. The control of the two-level PWM current rectifier by Lyapunov function using feedback loops to regulate the average value of DC voltages and the network currents are discussed in section 3. Therefore, a clamping bridge control is introduced to improve the performance of voltage balance strategy in section 4. Finally, in the section 5, simulations will be implemented to present a study of the phenomenon, to demonstrate the proposed method and to report the effectiveness of this solution.

II. FIVE-LEVEL CASCADE

We firstly propose a knowledge model of the three-phase five-level NPC-VSI inverter and develop a PWM strategy to control it (four bipolar carriers). The global scheme of the cascade is given on the Fig 1.

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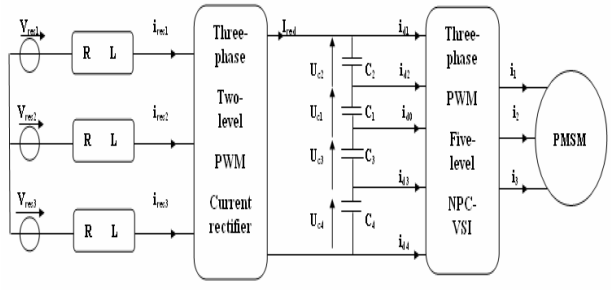

Fig.1: Structure of the cascade proposed

A. Five-level NPC-VSI modelling

The general structure of the three-phase five-level NPC voltage source inverter is shown on the figure 2. It is composed by 24 pairs transistor-diode. Every leg of this inverter includes eight pairs, four on the upper half leg and four on the lower one.

The optimal control law is given below:

$$\begin{cases} B_{k1} = \overline{B_{k5}} \\ B_{k2} = \overline{B_{k4}} \\ B_{k3} = \overline{B_{k6}} \\ B_{k7} = B_{k1}.B_{k2}.\overline{B_{k3}} \\ B_{k8} = B_{k4}.B_{k5}.\overline{B_{k6}} \end{cases} \quad (1)$$

B_{ks} is the control signal of TD_{ks}. TD_{ks} represent every pair transistor-diode by one bi-directional switch.

The voltage of the three-phase A, B, C relatively to the middle point M and using the half leg connection functions F_{kM}^{b} are given by V_{XM} with x = point A, B or C and k=1,2,3.

$$V_{XM} = [F_{k1}^{b}.(U_{c1} + U_{c2}) + F_{k7}.(U_{c1})] - [F_{k0}^{b}.(U_{c3} + U_{c4}) + F_{k8}.(U_{c3})] \quad (2)$$

The input currents of the three-phase five-level inverter using the load currents are given by the following relations:

$$\begin{cases} i_{d1} = F_{11}^{b}.i_1 + F_{21}^{b}.i_2 + F_{31}^{b}.i_3 \\ i_{d2} = F_{11}^{b'}.i_1 + F_{21}^{b'}.i_2 + F_{31}^{b'}.i_3 \\ i_{d3} = F_{10}^{b'}.i_1 + F_{20}^{b'}.i_2 + F_{30}^{b'}.i_3 \\ i_{d4} = F_{10}^{b}.i_1 + F_{20}^{b}.i_2 + F_{30}^{b}.i_3 \\ i_{d0} = i_1 + i_2 + i_3 - i_{d1} - i_{d2} - i_{d3} - i_{d4} \end{cases} \quad (3)$$

B. Control strategy of the inverter

For a five-level inverter, four carrier waves and three modulation signals are used. the modulation waves are compared with the triangular carrier waves and at the intersection points the switching decisions are made for the associated switches.

Pulse Width Modulation (PWM) of multilevel converters is typically an extension of two-level methods. The most common types of multilevel voltage-source PWM are sine-triangle modulation and space-vector modulation (SVM). Multilevel sine-triangle modulation relies on defining a number of triangle waveforms and switching rules for the intersection of these waveforms with a commanded voltage waveform [13–14]. This method is fairly straightforward and insightful for description of multilevel systems.

This strategy uses four bipolar carriers (U_{p1} , U_{p2} , U_{p3}, U_{p4}). It is characterised by two parameters **m** the index modulation and **r** the modulation rate. The algorithm of this strategy can be summarised as follows:

Step 1: Determination of the intermediate voltages

$$\begin{aligned} &\text{If } V_{refk} > U_{p1} \text{ then } V_{XM1} = +U_c \\ &\text{If } V_{refk} < U_{p1} \text{ then } V_{XM1} = 0 \\ &\text{If } V_{refk} > U_{p2} \text{ then } V_{XM2} = +2U_c \\ &\text{If } V_{refk} < U_{p2} \text{ then } V_{XM2} = +U_c \\ &\text{If } V_{refk} > U_{p3} \text{ then } V_{XM3} = 0 \\ &\text{If } V_{refk} < U_{p3} \text{ then } V_{XM3} = -U_c \\ &\text{If } V_{refk} > U_{p4} \text{ then } V_{XM4} = -U_c \\ &\text{If } V_{refk} < U_{p4} \text{ then } V_{XM4} = -2U_c \end{aligned} \quad (4)$$

Step 2: Determination of the output voltage (X=A, B,C)

$$V_{XM} = V_{XM1} + V_{XM2} + V_{XM3} + V_{XM4} \quad (5)$$

III. TWO-LEVEL PWM CURRENT RECTIFIER

The control of the two-level PWM current rectifier by Lyapunov Function using feedback loops to regulate the output DC voltage and the network currents are given.

The general structure of the two-level PWM current rectifier is given on the Fig 3.

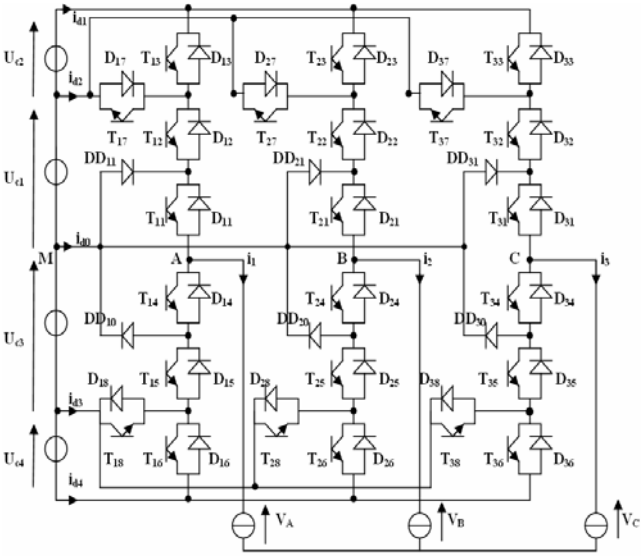

Fig.2: General structure of the three-phase five-level NPC VSI.

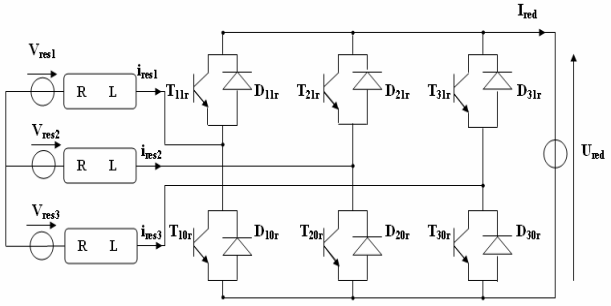

Fig.3: Structure of the two-level PWM current rectifier

A. Voltage feedback control

For each phase k (k=1, 2 or 3) of the three-phase network feeding, the rectifier considered can be represented by a R,L circuit. V_{resk} is the voltage of one phase k of the three-phase network and V_k is the voltage of the leg k of the rectifier [17].

The voltage loop imposes the effective value of the reference current of the network corresponding to the power exchanged between the network and the continue load (Fig 4).

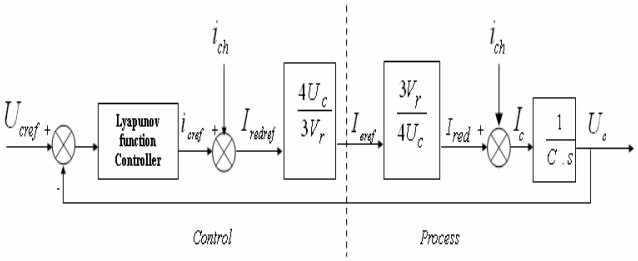

Fig.4: Control algorithm of the average output DC voltage of the two-level PWM current rectifier.

To guarantee the global asymptotic stability in the voltage loop, we obtain I_e as the output value of the voltage regulator:

$$I_e = \frac{4.U_C}{3.V_e}.\left[I_{ch} - K_U.C.(U_C - U_{Cref})\right] \qquad (6)$$

B. Current feedback control

We control the network current of the phase 1 and 2 by a sliding mode regulator. The algorithm of this current loop is given on the Fig 5. In this scheme, the transfer function $H(s)$ is expressed as follows:

$$H(s) = \frac{I_{resk}}{V} = \frac{1}{R + L.s} \qquad (7)$$

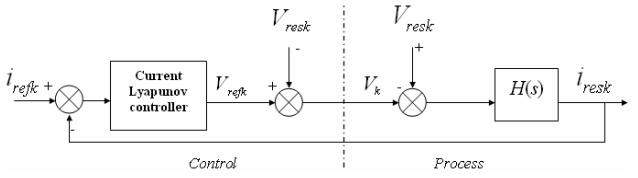

Fig.5: Control algorithm of the network current i_{resk} of the three-level PWM rectifier.

To guarantee the global asymptotic stability in the current loop, we obtain N_{gk} as the output of the current regulator:

$$N_{gk} = \frac{1}{4U_C}\left[V_{resk} - RI_{resk} - I_e\omega L\sqrt{2}\cos(\omega t - (k-1)\frac{2\pi}{3} + K_i L(i_{resk} - i_{refk})\right] \qquad (8)$$

IV. CLAMPING BRIDGE

In this section, a clamping bridge control is introduced to balance the four DC input voltages, avoid NP potential drift and improve the performances of the speed control of the permanent magnet synchronous machine.

Several publications have discussed ways to solve this balancing problem in three-level NPC-VSI [8-17]. The multitude of proposals (selection of appropriate voltage vectors) implemented to ensure DC voltage balancing can be broadly divided into two categories. In the first category based on space vector realization, redundant switching states of the converter are used while in the second category using carrier-based pulse width modulation (PWM) scheme, a zero sequence voltage signal is added to the modulation signals. In some schemes using zero sequence voltage to balance DC capacitor voltages, knowledge of load power factor (or direction of instantaneous power flow) is required which is difficult to implement under transient conditions, and in others, measurements of both capacitor voltages and load currents (magnitudes or polarities) are required. Unfortunately, these methods modify the output voltage waveform. Also, as the number of inverter-levels increases, the problem of capacitor balancing becomes more complex and the solution very drastic.

By using a separate supply for each DC-link level, the balancing issues are solved [6]. However, this solution is expensive especially for more then three-level. Another solution consists of adding electronic circuitry. In [16-18], clamping bridges based on transistors and resistors (dissipative method) are proposed as a solution to this problem. Advantages are low cost and low complexity. Disadvantages are high energy losses, high current switches and costly design thermal management requirements for large values. This method is best suited for systems that are charged often with small currents.

In order to remedy to the unbalance problem, we suggest a solution which consists in establish a bridge balancing between the rectifier and the intermediate filter (Fig 6). The aim of this use is to limit and stabilise variations of the input DC voltages of the inverter.

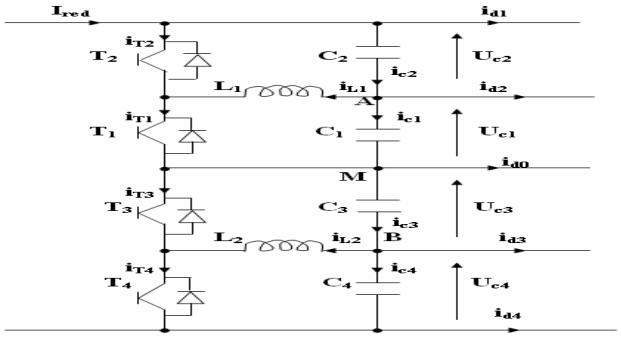

Fig. 6: Structure of the clamping bridge

The capacitor voltage equalization clamping bridge scheme has many advantages such as higher equalization efficiency and a modular design approach.

As shown in Figure 6, switches T_1 , T_2 , T_3 and T_4 are MOSFET; diodes D_1 , D_2 , D_3 and D_4 are continued flow diodes; L_1 and L_2 is the energy storage inductors; C_1 , C_2 , C_3 and C_4 are four adjacent series cells, respectively.

The basic operational principle is as follows:

* When $U_{c1}>U_{c2}$, a drive signal is given to the switches, and switch T_2 is turned off and T_1 is turned on. While T_1 is on, capacitor C_1, switch T_1 and inductor L_1 forms a loop circuit, whose current is I_{c1} . The part of energy of capacitor C_1 transfers to inductor L_1 . While T_1 is off, capacitor C_2 , inductor L_1 and the diode D_2 forms a loop circuit, whose current is I_{c2} .

  The energy of inductor L_1 transfers to capacitor C_2 .

* When $U_{c1} <U_{c2}$, switch T_1 is turned off and T_2 is turned on. The energy transfers from C_2 to C_1 until the voltages of the two capacitors are the same.

* When $U_{c3}>U_{c4}$, a drive signal is given to the switches, and switch T_4 is turned off and T_3 is turned on. While T_3 is on, capacitor C_3, switch T_3 and inductor L_2 forms a loop circuit, whose current is I_{c3}. The part of energy of capacitor C_3 transfers to inductor L_2 . While T_3 is off, capacitor C_4, inductor L_2 and the diode D_3 forms a loop circuit, whose current is I_{c2}. The energy of inductor L_2 transfers to capacitor C_3.
* When $U_{c3} <U_{c4}$, switch T_3 is turned off and T_4 is turned on. The energy transfers from C_3 to C_4 until the voltages of the two capacitors are same.

Capacitor voltage equalization control should be implemented to restrict the charge-discharge current to the allowable cell limitations in the capacitor string.

The balancing algorithm search to efficiently remove energy from a strong capacitor and transfer that energy into a weak one until the capacitor voltage is equalized across all capacitors.

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A. Switch control strategy of the clamping bridge

Step 1: Deduction of the sign of the differences.

We use the following equations:

$$C_1 . \frac{d(U_{c1} - U_{c2})}{dt} = (i_{L1} - i_{c2} + i_{d2} + i_{c1}) \quad (9)$$

$$C_3 . \frac{d(U_{c3} - U_{c4})}{dt} = (i_{L2} - i_{c3} + i_{c4} + i_{d3}) \quad (10)$$

Step 2: Deduction of the command of the transistors

$$\begin{cases} U_{c2} > U_{c1} \Rightarrow T_2 = 1; T_1 = 0 \\ U_{c1} > U_{c2} \Rightarrow T_2 = 0; T_1 = 1 \\ U_{c3} > U_{c4} \Rightarrow T_3 = 1; T_4 = 0 \\ U_{c4} > U_{c3} \Rightarrow T_3 = 0; T_4 = 1 \end{cases} \quad (11)$$

V. Simulation Results

In order to validate the solution proposed previously, we present simulation results for the two-level PWM current rectifier – five-level NPC-VSI – PMSM cascade. In the first case, the clamping bridge will not be used in order to show the instability problem of the four input DC voltages. In the second one, the solution proposed is introduced to improve the performances of DC voltages and PMSM.

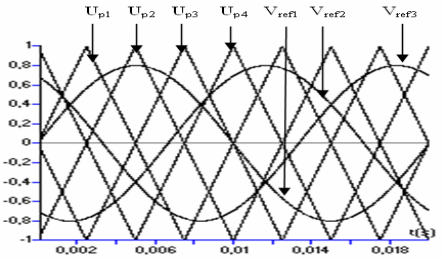

Fig.7. Reference voltages and bipolar carriers

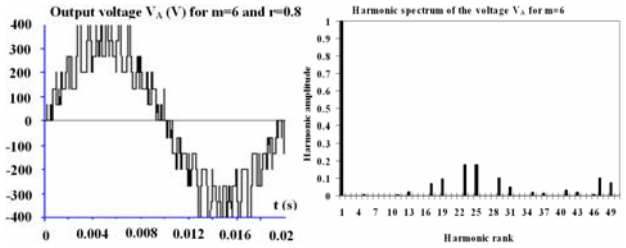

Fig.8. Output voltage V_A for m=6, r=0.8 and f=50Hz

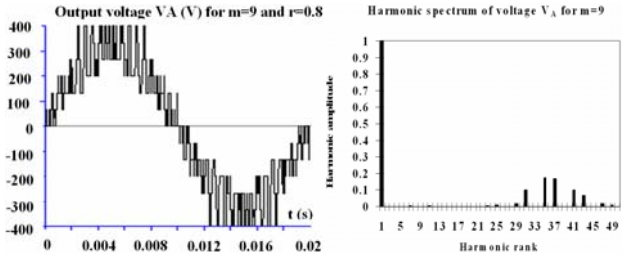

Fig.9. Harmonic spectrum of the voltage V_A (m=9 r=0.8.

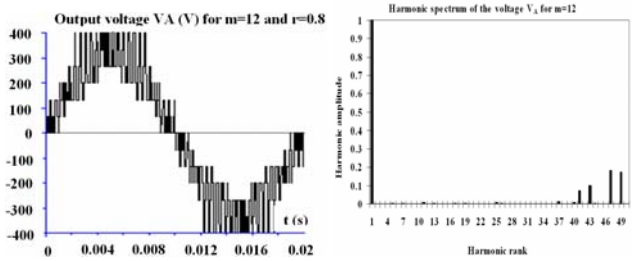

Fig.10. Harmonic spectrum of the voltage V_A for m=12 and r=0.8

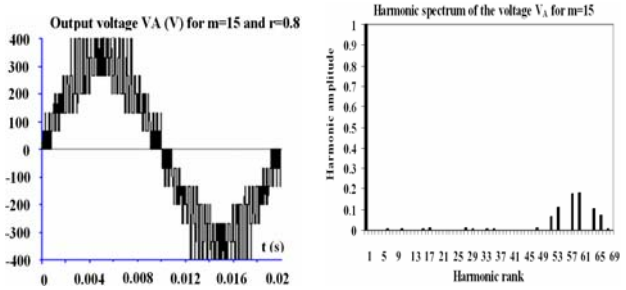

Fig.11. Harmonic spectrum of the voltage V_A for m=15 and r=0.8

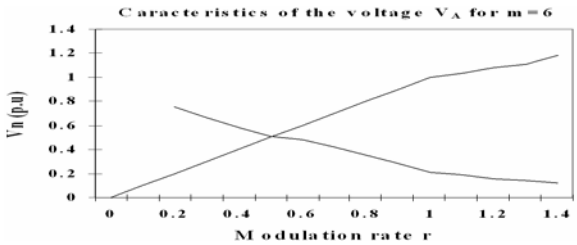

Fig.12. Characteristics of the voltage V_A for m=6

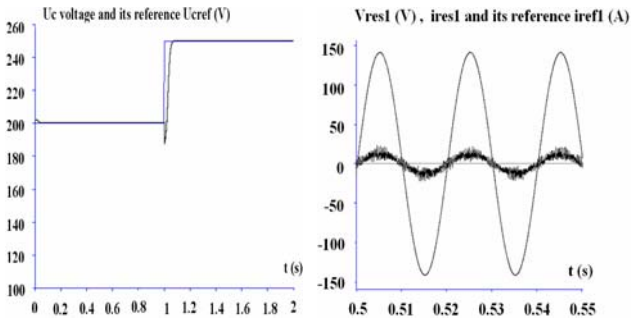

Fig.13: Voltage U_c and its reference and the network voltage V_{res1} , the network current i_{res1} and its reference i_{ref1}

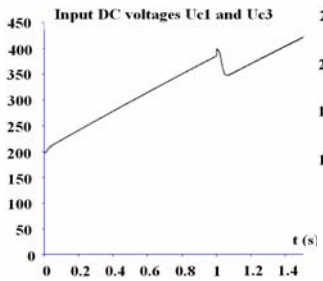

Fig.14: Voltage U_{c1} and Uc3

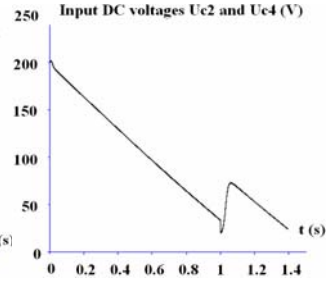

Fig.15: Voltage U_{c2} and Uc4

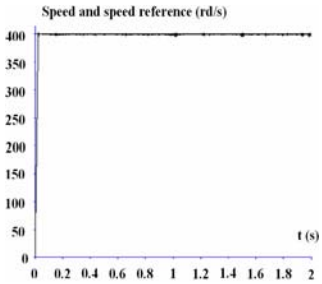

Fig.16: Speed and its reference

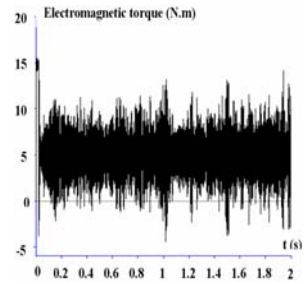

Fig.17: Electromagnetic torque

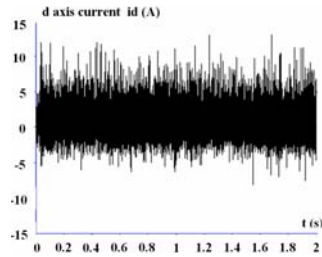

Fig.18: d axis current (i_d)

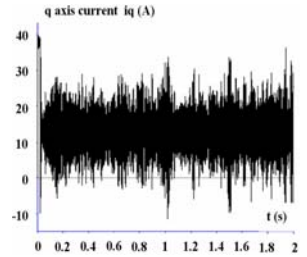

Fig.19: q axis current (i_q)

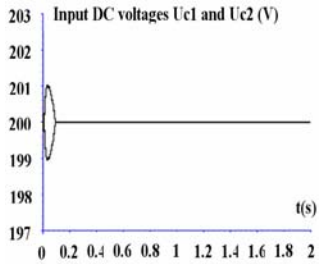

Fig.20: Voltages U_{c1} and U_{c2}

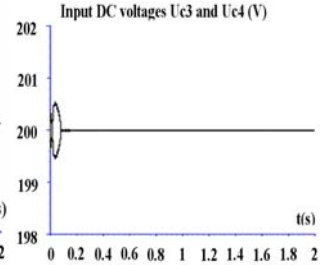

Fig.21: Voltages U_{c3} and U_{c4}

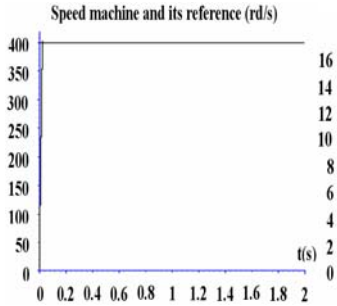

Fig.22: Speed and its reference

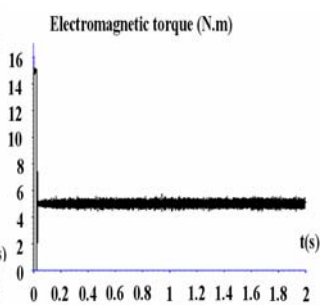

Fig.23: Electromagnetic torque

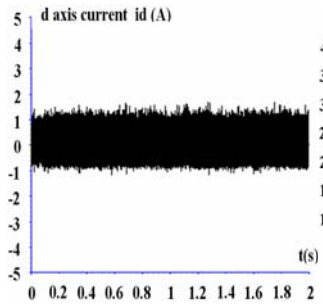

Fig.24: d axis current (i_d)

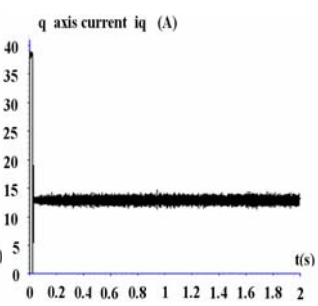

Fig.25: q axis current (i_q)

VI. Results and Discussions

The figure 7 shows the reference voltages and the four bipolar carriers used for this strategy. The figures 8 to 11 give the output voltage V_A. and its harmonic spectrum for a modulation index m=6 (Fig.8), m=9 (Fig.9), m=12 (Fig.10) and m=15 (Fig.11) and a modulation rate r=0.8. The frequency is 50 Hz. We notice that in the four cases, the harmonics gather by families centred around frequencies multiple of 4.m.f. Because of the symmetry to the quarter of the period presented by the voltage V_A, we obtain only odd harmonics. The most important harmonics gather around the first family.

The modulation rate r lets linear adjusting of fundamental magnitude from r=0 to r=1 and the harmonics rate decreases when r increases (Fig.12).

For evaluating the performances of the Clamping bridge proposed, two simulations are presented. The first one propose to study a one two-level PWM current rectifier – Five-level NPC VSI – Permanent Magnet Synchronous Machine. This study shows particularly the problem of the instability of the input DC voltages of the five-level NPC VSI and its consequence on the performances of the PMSM speed control for U_{DC}=800V, m=72, r=0.8

In order to test the Lyapunov function control of the average value of the output voltage of the two-level PWM rectifier, a voltage reference of 200V is applied and at t=1s we increase this reference from 200 to 250V. The figure 13 shows the voltage U_c and its reference obtained. This voltage follows perfectly its reference (200V). The network current i_{res1} of the rectifier is in phase with the network voltage V_{res1}. The parameters of the net are: R=0.25Ω ; L=10mH.

On the figure 14 and 15, we show perfectly the problem of the unbalance of the four DC voltages of the intermediate capacitors bridge. The voltages U_{c2} and U_{c4} are decreasing and the voltages U_{c1} and U_{c3} are increasing. The parameters of the capacitors are: C_1=C_2=C3=C4= 20µF

The figures 16 to 19 show the consequences of the DC voltages drift on the characteristics of the Permanent Magnet Synchronous Machine. The speed follows its reference (400 rd/s) but the undulations on the electromagnetic torque and different currents (i_d, i_q) are very important due to the unbalance problem of the four input DC voltages. The parameters of the PM synchronous machine are: L_d=L_q=3.2mH; R_s=1Ω; p=3; Φ_f=0.13N.m/A; J=6.10^{-4} kg.m²; F_c=$9{,}5.10^{-5}$ N.m.s/rad.

Those results show the importance of the stability of the input DC voltages of the inverter in order to have good performances for the speed control of the PM synchronous machine.

On the second simulation, we introduce the clamping bridge proposed in the precedent cascade on the Figure 1 in order to show the different input DC capacitor voltage equalization performances. We can see on the figures 20 and 21 that the four voltages (U_{c1}, U_{c2}, U_{c3} and U_{c4}) stabilise around the reference voltage value (200V) and the DC link capacitor voltages are equalized. By using this technique of stabilisation, we can remark on the figure 22, 23, 24 and 25 that the undulations on the performances (Torque and currents i_d and i_q) of the PMSM disappear and those performances are improved by using the inductive Clamping bridge. The parameters of the Clamping bridge are: L_1= 1mH L_2=1mH.

The afore-presented results confirm that the clamping bridge is able to equalize DC link capacitor voltages and stabilize the different DC voltages around the desired value. The performances of speed control of the PMSM are then ameliorating.

VII. CONCLUSION

The present contribution intends to demonstrate that permanent magnet synchronous machine control based on sliding mode control when applied with a two-level PWM current rectifier – Five-level PWM NPC-VSI may contribute both for functional performances improvement and attenuation of some technological limitations. The input DC voltages are generated by a two-level PWM current rectifier controlled by Lyapunov function. By this study, we have particularly shown the problem of the stability and its effects on the speed control of PMSM and the input DC voltages sources of the inverter.

In the last part of this paper, we propose a simple solution to stabilise the four DC voltages and this by using a clamping bridge composed by four switches (pair transistor-diode) and two inductances.

This nondissipative equalization design has many advantages such as high equalization efficiency due to the nondissipative current diverter, bidirectional energy transferring capability, and a modular design. Another advantage of this system is that no closed-loop control is needed and the process is self-limiting: when voltage equalization is complete, the switching of the capacitors consumes minimal energy.

APPENDIX

L_d , L_q : self inductance of the d and q armatures equivalent winding, R_s : resistance of an armature winding, ω : angular speed. s : Laplace operator,

J : inertia of the set machine-load , C_r : Load torque,

e_d : Error variable, S_d : Surface variable

V_{resk} : Network voltage of one phase k, V_k : Voltage of the leg k of the rectifier, R : grid resistance L : grid inductance

U_C : Average value of the four input DC voltages

C_1, C_2, C_3, C_4 : input capacitors of the five-level NPC-VSI

$V_{res}; i_{res}$: Voltage and current of the grid

V_e : Effective value of the grid voltage

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