Improved Power Quality Based Electronic Ballast for a Fluorescent Lamp with Constant DC Link Voltage

Ashish Shrivastava[1] and Bhim Singh[2]

Abstract–This paper deals with the analysis, design, modeling and simulation of a low crest factor (CF) and a high power factor (PF) electronic ballast for a fluorescent lamp. The proposed ballast uses a boost converter in continuous conduction mode (CCM) as a power factor corrector (PFC). In this topology, a half bridge series resonant parallel loaded inverter is used to convert dc to high frequency ac to feed fluorescent lamp. The modeling and simulation of this topology are carried out in Matlab-Simulink environment for a fluorescent lamp fed from 220V, 50Hz ac mains. The power quality indices are estimated such as total harmonic distortion of ac mains current (THD_i), power factor (PF) and crest factor (CF).

Keywords–Power factor correction (PFC), Continuous conduction mode (CCM), Electronic ballast, Fluorescent lamp, Zero voltage switching (ZVS), and Series resonant parallel loaded inverter (SRPLI).

I. Introduction

In recent years fluorescent lamps have become increasingly popular as an alternative to conventional incandescent lamps because of their better luminous efficacy (Lm/Watt) and power consumption. Fluorescent lamps exhibit negative resistance characteristic in the desired region of operation. This produces an unstable condition if a fluorescent lamp is directly connected across a voltage source to cause ionization. Therefore, a current-limiting device called ballast is required [1]. Compared to conventional magnetic ballasts, high frequency (20-100 kHz) electronic ballasts offer significant advantages such as reduction in power consumption, flicker, audible noise and weight [2-5]. The electronic ballast consists of a power factor correction ac-dc converter, high frequency inverter and a matching resonant circuit. The resonant circuit enables a high ignition voltage to be generated and makes the lamp current essentially sinusoidal. In electronic ballast, high frequency dc-ac conversion becomes possible with the invention of solid state switching devices namely MOSFETs which have high switching capability with almost negligible losses. The preferred method to drive the fluorescent lamp is by using an unmodulated sine wave current with a minimal ripple content. The input current crest factor (I_{peak}/I_{rms}) for the operating condition should be as low as possible, not exceeding 1.7 [1, 6].

Besides this, in comparison of magnetic ballast, electronic ballast can control lamp power more easily and has higher efficiency. Normally, a power factor corrected electronic ballast needs two level of power conversion. First level of power conversion is for ac-dc conversion and second level is for dc-ac conversion.

In this paper, a power factor corrected topology with constant dc link voltage is proposed for an electronic ballast. The power factor correction (PFC) converter improves the input power factor nearly close to unity and regulates dc voltage and the half bridge resonant inverter maintains the constant load power supplied at high frequency. Because of the zero voltage switching (ZVS), the switching losses are reduced significantly which enhances the efficiency of the electronic ballast.

II. Proposed Topology of Electronic Ballast

Fig. 1 has shown the schematic of the proposed electronic ballast, which consists of a PFC converter and a lamp driving dc-ac converter in cascade connection. The ac-dc converter achieves power factor correction (PFC) and the dc-ac converter supplies high frequency voltage to the fluorescent lamp [8-13]. In proposed electronic ballast the selection of a proper converter is made based upon the following guidelines.

- An energy storage element is used between a PFC converter and a lamp-driving dc-ac converter to prevent the lamp current from being modulated by the line voltage. For this purpose a dc capacitor is preferred over an inductor due to its lesser cost and size.
- A lamp-driving dc-ac converter is selected to be a voltage-fed inverter to save filter components.
- Low source voltage is needed to boost-up for generating a high voltage to ignite lamp without the need of a boost-up transformer.

As per the considerations given above, a boost converter is selected as the PFC converter, and a quasi-half-bridge series resonant parallel loaded inverter is used to drive the lamp. Fig. 1 shows the proposed electronic ballast derived from CCM boost converter and quasi-half-bridge series resonant parallel loaded inverter (SRPLI).

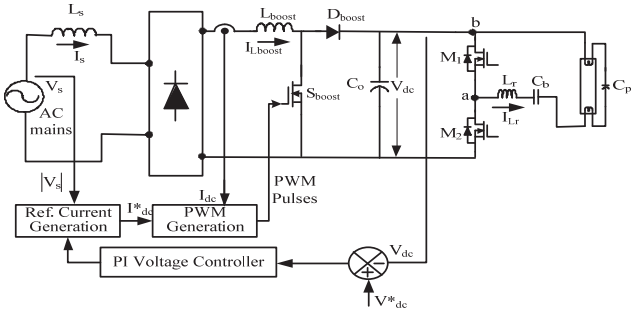

Fig.1: Proposed Topology of a Boost PFC Electronic Ballast

The active power switches of series resonant inverter M_1 and M_2 are alternately turned on and off at a 40 kHz frequency. The switching frequency of the inverter should be more than the resonant frequency of the load circuit to achieve the ZVS (zero voltage switching),

The paper first received 2 Feb 2010 and in revised form 26 Sep 2011.
Digital Ref: A190711265

[1] Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, E-mail: rewa.ashish@gmail.com
[2] Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, E-mail: bhimsingh1956@gmail.com

which reduces the switching losses and improves the overall efficiency of electronic ballast.

III. Analysis and Design of Proposed Electronic Ballast

Following considerations are made to analyze the proposed topology of electronic ballast [7-9].

- At the time of starting, the fluorescent lamp behaves as an open circuit and during steady state operation it is considered as a pure resistor.
- As compared to the lamp resistance the filament resistance is neglected and switching devices are considered ideal switches.
- The dc blocking capacitor C_b is much larger than the resonant capacitance C_p so that its voltage ripple is negligible.

The detailed design of the boost inductor and the resonant inverter components are as follows.

A. Design of Boost Inductor

The value of boost inductor is evaluated by using the below mentioned equations. The duty ratio, D is expressed in terms of dc inverse voltage gain as,

$$D = 1 - \alpha \tag{1}$$

where, α is defined as,

$$\alpha = \frac{V_{sm}}{V_{dc}} \tag{2}$$

The coefficient $Y(\alpha)$ is defined as,

$$Y(\alpha) = -2 - \frac{\pi}{\alpha} + \frac{2}{\alpha\sqrt{1-\alpha^2}}\left\{\frac{\pi}{2} + \tan^{-1}\left(\frac{\alpha}{\sqrt{1-\alpha^2}}\right)\right\} \tag{3}$$

From (3), the value of boost inductor is given as,

$$L_{boost} = \left(\frac{V_{sm}}{\omega_{switching} P_o}\right)\frac{(1-\alpha^2)Y(\alpha)}{\alpha} \tag{4}$$

where, D is duty ratio, α is dc inverse voltage gain, V_{sm} is peak value of the input rms voltage, V_{dc} is dc link voltage, P_o is rated output power of fluorescent lamp.

B. Design of Resonant Circuit Parameters

At the time of starting, the self oscillating technique provides a resonant frequency ($\omega_{starting}$) which is made equal to the switching frequency ($\omega_{switching}$). The relationship between the resonant parameters and the starting resonant frequency is given by (5) as,

$$\omega_{starting} = \omega_{switching} = \frac{1}{\sqrt{L_r\left(\frac{C_b C_p}{C_{b+} C_p}\right)}} \tag{5}$$

The steady-state resonant frequency is given by (6) as,

$$\omega_{running} = \frac{1}{\sqrt{L_r C_b}} \tag{6}$$

If the switching frequency is more than the steady-state resonant frequency then the zero voltage switching (ZVS) is ensured. Considering that,

$$\omega_{switching} = 4\omega_{running} \tag{7}$$

Fig.2 shows the equivalent circuit of the series resonant parallel loaded inverter (SRPLI) under the steady-state operation of the lamp. In this circuit L_r, C_b and C_p are the resonant circuit parameters and R_{lamp} is the resistance of the fluorescent lamp.

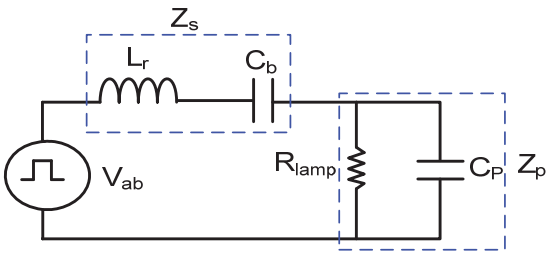

Fig. 2: Equivalent circuit of the inverter

The relationship between the rated lamp voltage and the fundamental component of the output of voltage source inverter is given in (8) in the frequency domain as,

$$\left|\frac{V_{lamp}(j\omega)}{V_{ab}(j\omega)}\right| = \left|\frac{Z_p(j\omega)}{Z_s(j\omega) + Z_p(j\omega)}\right| \tag{8}$$

By solving (5), (6), (7) and (8), the resonant parameters can be given as,

$$C_b = 15\left(\frac{V_{lamp}}{V_{ab}}\right)\left(\frac{1}{R_{lamp}\omega_{switching}}\right) \tag{9}$$

$$C_P = \frac{C_b}{15} \tag{10}$$

$$L_r = \frac{16}{C_b(\omega_{switching})^2} \tag{11}$$

This design procedure includes the calculation of the boost inductor and resonant circuit parameters.

IV. Operating Modes of Proposed Ballast

The operating modes of the proposed Electronic ballast are gives as below in Figs 3a-3d.

(a) At $t_0 < t < t_1$, body diode D_2 is conducting and dc link capacitor is charged in the process. In this duration also gate pulse has been applied to the solid state active power switch M_2. The sequence of flow of current is given and also shown in Fig.3a,

$C_o(-) \rightarrow D_2 \rightarrow L_r \rightarrow C_b \rightarrow (R_{lamp} \| C_P) \rightarrow C_o(+)$

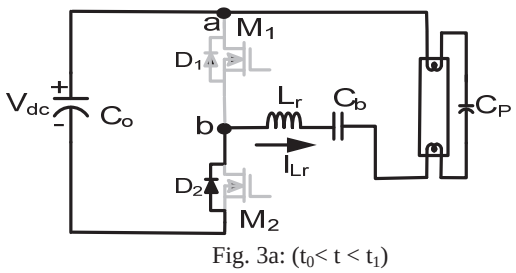

Fig. 3a: ($t_0 < t < t_1$)

At $t_1 < t < t_2$, MOSFET M_2 starts conducting and dc link capacitor is discharged in the process. The direction of resonant current changes as the current is shifted from diode D_2 to active power switch M_2. The sequence of flow of current is given and also shown in Fig.3b,

$C_o(+) \rightarrow (R_{lamp} \| C_P) \rightarrow C_b \rightarrow L_r \rightarrow M_2 \rightarrow C_o(-)$

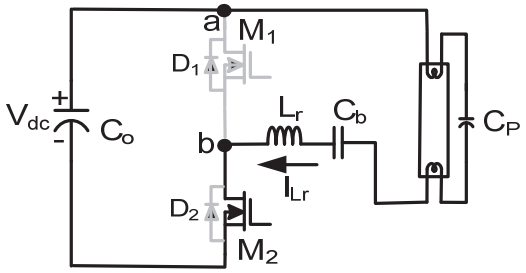

Fig. 3b: ($t_1 < t < t_2$)

At $t_2 < t < t_3$, body diode D_1 is conducting and the direction of current remains the same due to resonating nature of the circuit. In this duration gate pulse has also been applied to the active power switch M_1. The sequence of flow of current is given and also shown in Fig.3c,

$D_1 \rightarrow (R_{lamp} \| C_P) \rightarrow C_b \rightarrow L_r \rightarrow D_1$

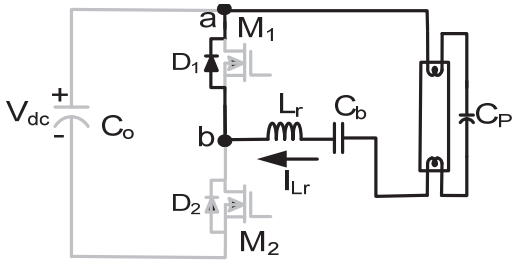

Fig. 3c: ($t_2 < t < t_3$)

At $t_2 < t < t_3$, MOSFET M_1 starts conducting and the current shifted from body diode D_1 to active power switch M_1. Hence the direction of current changes from positive to negative. The sequence of flow of current is given and also shown in Fig.3d,

$M_1 \rightarrow L_r \rightarrow C_b \rightarrow (R_{lamp} \| C_P) \rightarrow M_1$

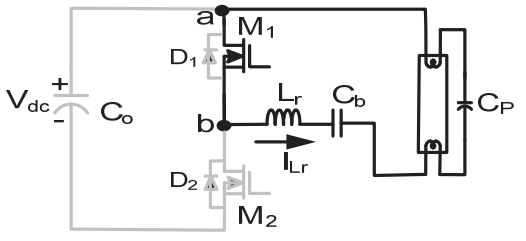

Fig. 3d: ($t_3 < t < t_4$)

Since the circuit is working at lagging power factor ($f_r < f_s$) as confirmed from Fig. 3e, the zero voltage switching (ZVS) has been achieved in resonant converter operation. Moreover, it is clearly observed from the operating modes of the above circuit that both MOSFETs (M_1 and M_2) are operating at zero voltage switching (ZVS). The theoretical waveform of series resonant inverter is given in Fig.3e.

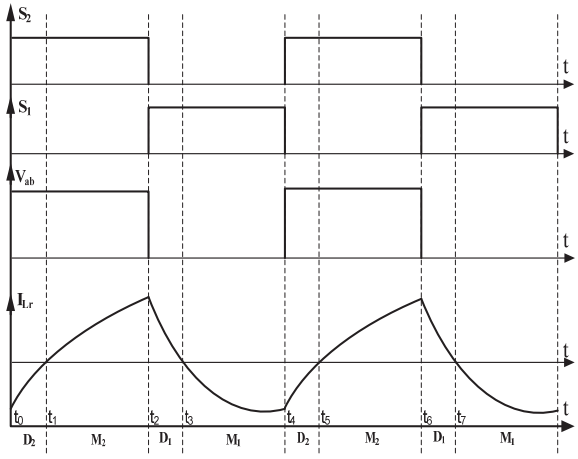

Fig. 3e: Theoretical waveforms of series resonant inverter of proposed electronic ballast

V. MATLAB MODEL OF PROPOSED BALLAST

The Matlab model of the proposed electronic ballast is developed as shown in Fig.4 in which the lamp is considered as a resistor at high frequency. The PFC topology is modeled in Matlab-Simulink model using PI (Proportional Integral) controller with current multiplier approach.

A 40 kHz triangular carrier wave is used for PWM generation. The design values of the components obtained from various design equations are appropriately selected to have desired power quality at the AC mains. These component values are given in Appendix along with other control parameters.

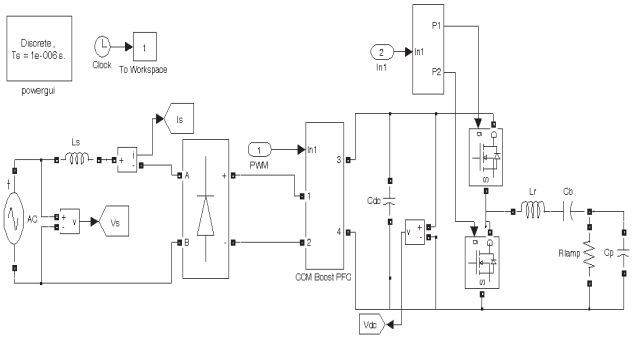

Fig. 4 Matlab model of proposed electronic ballast

VI. RESULTS AND DISCUSSION

The objective of the modeling and simulation is to validate the design of proposed electronic ballast which has improved power factor, low THD and low crest factor of ac mains current. As the ac input voltage increases from 100 V-270V, the dc link voltage remains constant at 400 V, thus the lamp current remains constant throughout this wide input ac voltage range, which realizes the constant lamp power. The input ac voltage and current waveforms, dc link voltage, boost inductor current at 100 V, 220 V and 270 V are shown in Fig. 5, Fig. 7, and Fig. 9. The lamp voltage and lamp current waveforms at 100 V, 220 V and 270 V are shown in Fig. 6, Fig. 8 and Fig. 10.

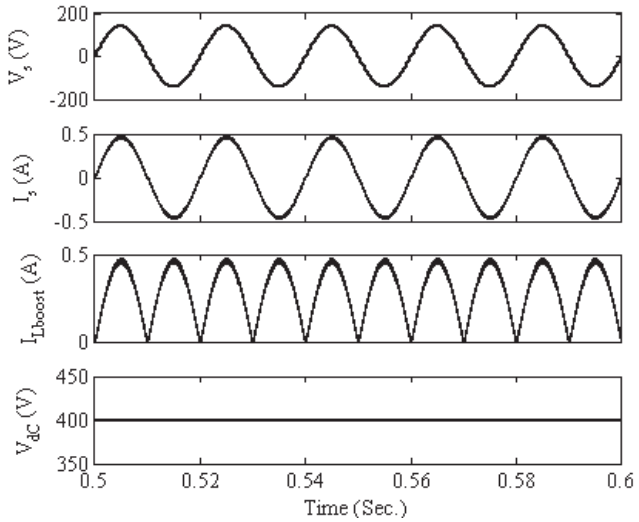

Fig.5: Performance of proposed electronic ballast in terms of source voltage (V_s), source current (I_s), boost inductor current (I_{Lboost}) and dc link voltage (V_{dc}) at 100 V

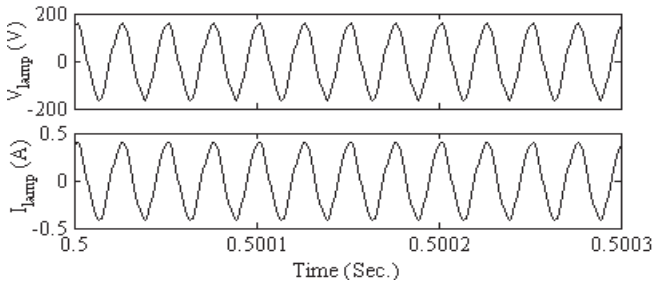

Fig.6: Performance of proposed electronic ballast in terms of lamp voltage (V_{lamp}) and lamp current (I_{lamp}) at 100 V

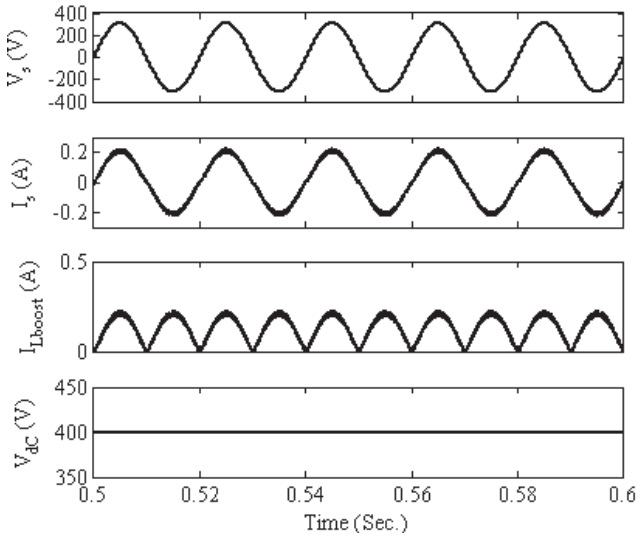

Fig.7: Performance of proposed electronic ballast in terms of source voltage (V_s), source current (I_s), boost inductor current (I_{Lboost}) and dc link voltage (V_{dc}) at 220 V

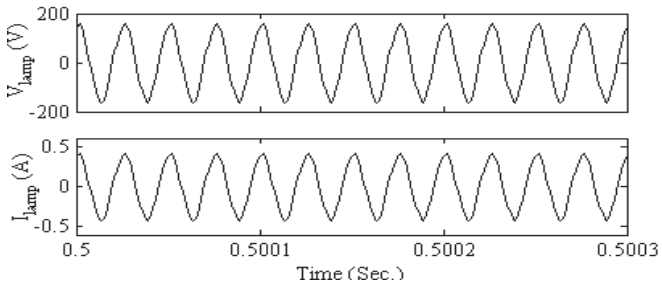

Fig.8: Performance of proposed electronic ballast in terms of lamp voltage (V_{lamp}) and lamp current (I_{lamp}) at 220 V

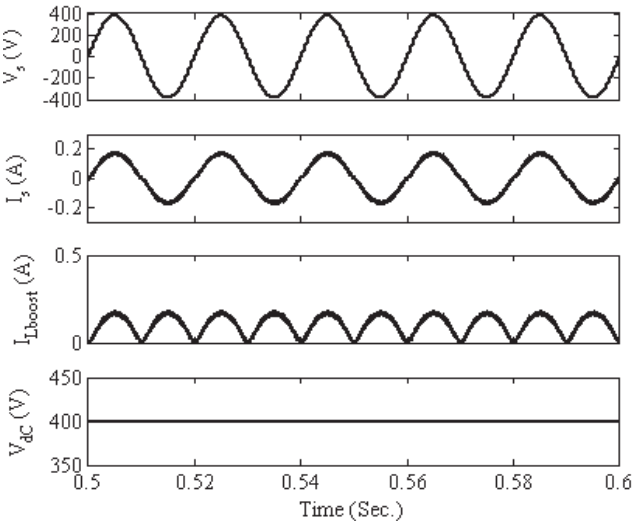

Fig.9: Performance of proposed electronic ballast in terms of source voltage (V_s), source current (I_s), boost inductor current (I_{Lboost}) and dc link voltage (V_{dc}) at 270 V

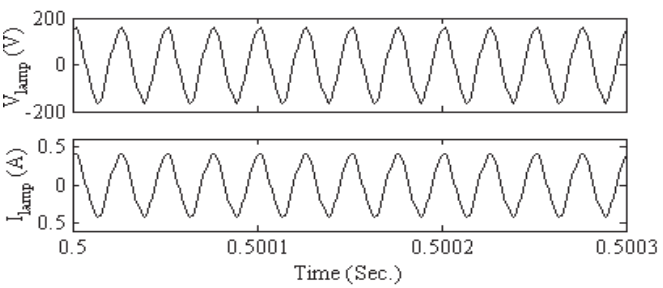

Fig.10: Performance of proposed electronic ballast in terms of lamp voltage (V_{lamp}) and lamp current (I_{lamp}) at 270 V

The fluorescent lamp is driven by a high frequency sinusoidal current generated from an LCC series resonant parallel converter, which operates above the resonant frequency to a zero voltage switching (ZVS). Fig. 11 shows the switch voltage (V_{M2}) and switch current (I_{M2}) waveforms (which is amplified 600 times to show on same scale as of V_{M2}), which confirms the zero voltage switching (ZVS).

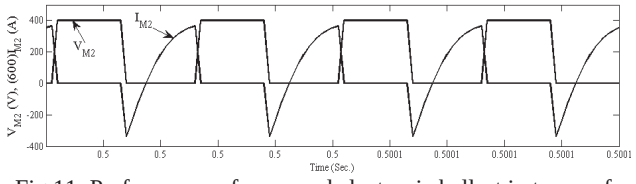

Fig.11: Performance of proposed electronic ballast in terms of switch voltage (V_{M2}), switch current ($600I_{M2}$) at 220 V

The ac mains current waveform along with its harmonic spectra and THD are shown in Fig. 12, Fig. 13 and Fig. 14 at ac mains voltage of 100 V, 220 V and 270 V.

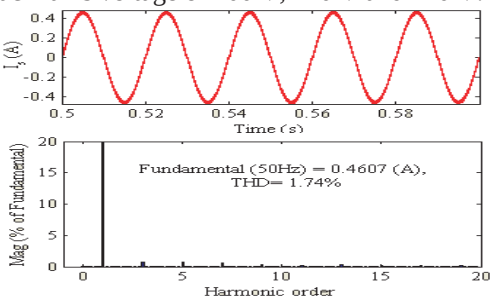

Fig. 12: Input current waveform and its harmonic spectra at ac mains voltage of 100V

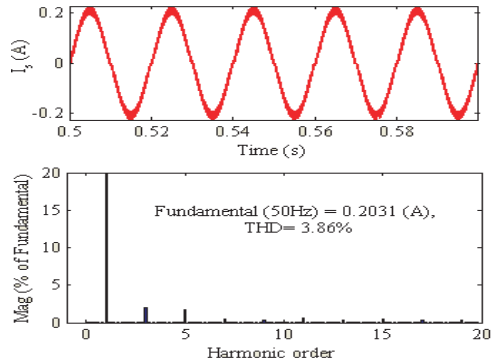

Fig. 13: Input current waveform and its harmonic spectra at ac mains voltage of 220V

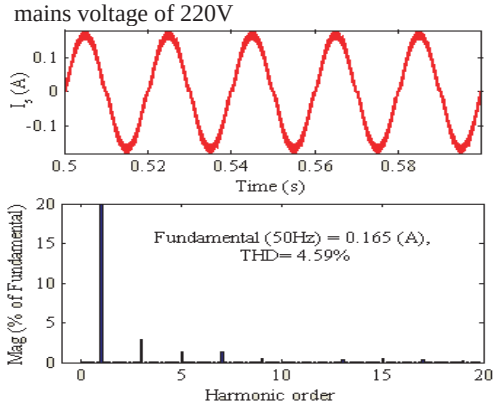

Fig. 14: Input current waveform and its harmonic spectra at ac mains voltage of 270V

The power quality parameters of the proposed boost PFC electronic ballast are listed in Table-I. The dc link voltage, lamp voltage and current have been maintained almost constant under the change in ac mains voltage from 110V-270 V. Table-I shows the variation of power factor, crest factor and % THD of ac mains current of proposed electronic ballast with input ac mains voltage. Moreover, power quality parameters of the proposed electronic ballast are within the norms of international standard IEC 61000-3-2 for class C equipment [6].

Table 1: Performance Parameters of Proposed Electronic Ballast

V_s (V)	I_s (A)	V_{dc} (V)	V_{lamp} (V)	I_{lamp} (A)	PF	THD %	CF
100	0.3258	400	109.9	0.2819	0.9997	1.74	1.41
110	0.2942	400	109.9	0.2819	0.9996	1.85	1.41
120	0.2683	400	109.9	0.2819	0.9995	2.03	1.41
130	0.2467	400	110	0.2819	0.9994	2.26	1.41
140	0.2285	400	110	0.2819	0.9993	2.39	1.41
150	0.2127	400	110	0.2819	0.9992	2.60	1.41
160	0.1989	400	110	0.2819	0.9991	2.78	1.41
170	0.1869	400	110	0.2819	0.999	3.04	1.41
180	0.1763	400	110	0.2819	0.9988	3.20	1.41
190	0.1669	400	110	0.2819	0.9987	3.40	1.41
200	0.1584	400	110	0.2819	0.9985	3.62	1.41
210	0.1508	400	110	0.2819	0.9985	3.69	1.41
220	0.1438	400	110	0.2819	0.9984	3.86	1.41
230	0.1482	400	110	0.2819	0.9983	3.88	1.41
240	0.1317	400	110	0.2819	0.9982	4.15	1.41
250	0.1264	400	110	0.2819	0.9981	4.22	1.41
260	0.1215	400	110	0.2819	0.9979	4.36	1.41
270	0.117	400	110	0.2819	0.9977	4.59	1.41

VII. Conclusion

A high power factor electronic ballast with constant dc link voltage has been designed, modeled and simulated to study its behaviour. The dc link voltage has been maintained constant, independent of changes in the ac input voltage. With an appropriate design of the resonant converter, the lamp current has been found close to the rated value. The simulation results have confirmed the low crest factor of 1.41 and high power factor almost close to unity of proposed electronic ballast. The proposed ballast has THD of ac mains current well below 5% for the universal voltage range of 100V-270V. The zero voltage switching (ZVS) has been achieved by keeping the switching frequency more than the resonance frequency of resonant inverter to reduce the switching losses.

Appendix

Rated lamp power: 31W, rated lamp current: 0.2818 A, rated lamp voltage: 110 V, switching frequency of PFC switch (f_s): 40 kHz, PI controller gains (K_p): 0.0035, (K_i): 0.0038, boost PFC inductor (L_{boost}): 15mH, dc link capacitor (C_o): 30µF, Resonant parameters: - resonant inductor (L_r): 2.7mH, dc blocking capacitor (C_b): 90nF, resonant capacitor (C_p): 6nF

References

[1] E. E. Hammer and Terry K. McGowan, "Characteristics of various F40 Fluorescent Systems at 60Hz and High frequency," *IEEE Trans. on Industry Applications*, vol. IA-21, no. 1, pp. 11-16, Jan.-Feb. 1985.

[2] Ned Mohan, P. Undeland and S. Robbins, Power Electronics: Converter Application and Design, John Wiley and Sons, (Asia) Pvt. Ltd., Singapore, 2003.

[3] Alonso, J. Marcos and Muhammad Rashid (Editor-in-Chief), Electronic Ballasts, Power Electronics Handbook, Chapter 21, pp. 507-532, Academic Press, 2001.

[4] Issa Batarseh, Power Electronic Circuits, John Wiley and Sons, NJ, 2004.

[5] R. W. Erickson, Fundamentals of Power Electronics, Chapman and Hall, New York, May 2001.

[6] Limits for harmonic current emissions, International Electrotechnical Commission Standard 61000-3-2, 2004.

[7] R. L. Steigerwald "A comparison of half-bridge resonant converter topologies," *IEEE Trans. on Power Electron.*, vol. 3, no. 2, pp. 174-182, Apr. 1988.

[8] Kwang-Hwa Liu and Young-Lin Lin "Current waveform distortion in power factor correction circuits employing discontinuous mode boost converter," IEEE PESC, pp.825-829, 1989.

[9] J. A. Alves, A. J. Perin and I. Barbi "An electronic ballast with high power factor for compact fluorescent lamps," IEEE Thirty-First IAS Annual Meeting, IAS'96, Industry Applications Conference, 1996., vol. 4, 6-10 Oct. 1996, pp.2129-2135.

[10] C.S. Moo, Y.C. Chuang and C.R. Lee "A new power-factor-correction circuit for electronic ballasts with series-load resonant inverter," *IEEE Transactions on Power Electronics*, vol. 13, no.2, pp. 273-278, March 1998.

[11] Qian Jinrong, F.C. Lee and T. Yamauchi "Analysis, design, and experiments of a high-power-factor electronic ballast", *IEEE Trans. on Industry Applications*, vol. 34, no.3, pp. 616-624, May-June 1998.

[12] C. Aguilar, A. Ruiz, F. Canales and F. Lee "Analysis of the half-bridge boost rectifier as integrated electronic

ballast with power factor correction," IEEE 32nd Annual Power Electronics Specialists Conference, PESC2001, vol. 2, pp.707-712, 17-21 June 2001.

[13] F. J. F. Martin, C. B. Viejo, J. C. A. Anton, M. A. P. Garcia, M. Rico-Secades and J. M. Alonso "Analysis and design of a high power factor, single-stage electronic ballast for high-intensity discharge lamps," *IEEE Trans. on Power Electronics*, vol. 18, no. 2, pp.558-569, March 2003.

BIOGRAPHIES

Ashish Shrivastava was born in Rewa, India, in 1973. He received B.E. (Electrical) degree from A.P.S. University, Rewa, India, in 1999 and M. Tech. degree from MANIT Bhopal, India, in 2001.

He joined Mody college of Engineering and Technology, Laxmangarh, Sikar, Rajasthan, as a Lecturer in 2001. In 2003 he joined Galgotias college of Engineering and Technology, Greater Noida,UP, as Senior Lecturer in the department of Electronics and Instrumentation Engineering. His area of interest includes SMPS, energy efficient PFC DC/DC converters and power quality.

Dr. Bhim Singh was born in Rahamapur, India, in 1956. He received B.E (Electrical) degree from University of Roorkee in 1977 and M.Tech and Ph.D. degree from IIT Delhi, New Delhi, India, in 1979 and 1983, respectively. In 1983, he joined the Department of Electrical Engineering, University of Roorkee, as a lecturer, and in 1988 became a Reader. In December 1990, he joined the Department of Electrical Engineering, IIT Delhi, as an Assistant Professor. He became an Associate Professor in 1994 and Professor in 1997. He has been granted one US patent and filed nine Indian patents. He has executed more than sixty sponsored and consultancy projects. His area of interest includes power electronics, electrical machines and drives, active filters, Flexible Alternating Current Transmission System (FACTS), High Voltage Direct Current (HVDC) and power quality.

Dr. Singh is a fellow of Institute of Electrical and Electronics Engineers (FIEEE), Indian National Academy of Engineering (FINAE), National Academy of Science, India (FNASI), the Institution of Engineers (India) (FIE), and the Institution of Electronics and Telecommunication Engineers (FIETE), a life Member of the Indian Society for Technical Education (LMISTE), the System Society of India (LMSSI), and the National Institution of Quality and Reliability.