Harmonic Analysis of Cascaded H-bridge Seven Level Inverter for RL Load Applications

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Abstract– A method is presented that a cascaded H-Bridge multilevel inverter can be implemented using unequal dc power sources. A standard cascade multilevel inverter requires n dc sources for 2n + 1 level. Proposed scheme allows the use of unequal DC power source without the requirement of transformers. Cascaded H-Bridge multilevel inverter which uses the unequal dc source shows the better performance and also significantly decreases the number of required switches. High quality output power due to its high number of output levels, results in high conversion efficiency and low thermal stress as it uses fundamental frequency switching scheme. This paper mainly discusses about the control of seven level multilevel converters with fundamental frequency switching control. The performance of single phase cascaded H-Bridge multilevel inverter with unequal dc source is simulated by using MATLAB/Simulink. A detailed harmonic analysis is done on cascaded H-Bridge seven level inverter and experimental results are presented to demonstrate the superiority of the proposed system.

Keywords–Fundamental frequency switching control, multilevel inverter, Total Harmonic distortion (THD), Unequal dc sources

I. INTRODUCTION

Multilevel converters have received more and more attention because of their capability of high voltage operation, reliable operation, high efficiency, and low electromagnetic interference (EMI). The desired output of a multilevel converter is synthesized by several sources of dc voltages [1], [2]. With an increasing number of dc voltage sources, the converter voltage output waveform approaches nearly sinusoidal waveform while using a fundamental frequency switching scheme.

Transformerless multilevel inverters are uniquely suited for this application because of the high VA ratings possible with these inverters [1]. Unique structure of the multilevel voltage source inverters allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized switching devices. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages [3], [4], [5], [6], [7]. Multilevel inverters also have several advantages with respect to hard switched two level pulse width-modulation (PWM) adjustable-speed drives.

Motor damage and failure have been reported by industry as a result of some adjustable-speed drives (ASD) operated by the inverters which has high voltage change rates (dv/dt), which produced a common-mode voltage across the motor windings.

High frequency switching can exacerbate the problem because of the numerous times this common-mode voltage is impressed upon the motor each cycle. The main problems reported have been “motor bearing failure” and “motor winding insulation breakdown” because of circulating currents, dielectric stresses, voltage surge, and corona discharge [8]–[10].

Multilevel inverters can able to overcome these problems because their individual devices have a much lower stress per switching and they can operate at high efficiencies because they can switch at a much lower frequency than PWM-controlled inverters.

In this work, a method is given to compute the switching angles for a multilevel converter so as to produce the required fundamental voltage while at the same time cancel out specified higher order harmonics. In particular, a complete analysis is given for a seven level converter and validated the performance with hardware.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

A cascaded multilevel inverter consists of a series of H-bridge (single-phase full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from separate dc sources, which may be obtained from batteries, fuel cells, or ultracapacitors [11]. Consider a single-phase structure of cascade multilevel inverter with two H-bridges as shown in Fig. 1. Separate dc source is connected to each H-bridges of a single-phase multilevel inverter. The ac output of each level is connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2, so that the output of this cascade multilevel inverter is denoted by

$$v(t) = v_1(t) + v_2(t) \quad (1)$$

By opening and closing the switches of bridge 1 appropriately, the output voltage v_1 can be made equal to −Vdc, 0, or Vdc, while the output voltage of bridge 2 can be made equal to −Vdc/2, 0 or Vdc/2 by opening and closing its switches appropriately. Therefore, the output voltage of the inverter can have the values −3Vdc/2, −Vdc, −Vdc/2, 0, Vdc/2, Vdc, 3Vdc/2, which is seven levels and is illustrated in Fig. 2.

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With enough levels, using this fundamental frequency switching technique results in an output voltage of the inverter that quasi-square waveform by phase shifting its positive and is almost sinusoidal. Each H-bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs' switching timings. Note that each switching device always conducts for 180 (or 1/2 cycle) regardless of the pulse width of the quasi-square wave. This switching method makes all of the active devices' current stress equal.

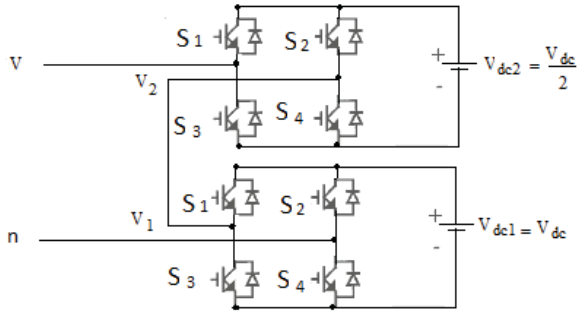


Fig.1: Structure of cascaded H-bridge multilevel inverter

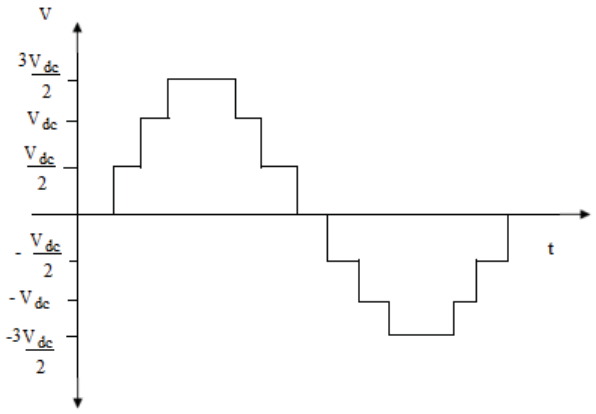


Fig.2: Output waveform of seven level cascaded H-Bridge inverter

III. Switching Angles

In conventional cascaded multilevel inverters, PWM control methods and space vector PWM method are used. These methods will cause extra losses due to high switching frequencies. To overcome this problem, low switching control methods [13],[15] are used. Here fundamental frequency switching method is used.

The Fourier series expansion of the (staircase) output voltage waveform of the seven level inverter as shown in Fig. 2 is

$$V(\omega t) = \frac{4}{\pi}\frac{V_{DC}}{2} \times \sum_{n=1,3,5}^{\infty} \frac{1}{n}(Cos(n\theta_1) + Cos(n\theta_2) + Cos(n\theta_3))\,Sin(n\omega t) \quad (2)$$

Ideally, given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1, θ_2 and θ_3 so that (2) becomes $V(\omega t) = V_1 \sin(\omega t)$. In practice, one is left with trying to do this approximately. In this case, the desire is to cancel the 5^{th} and 7^{th} order harmonics as they tend to dominate the total harmonic distortion. The mathematical statement of these conditions is then

$$\frac{4}{\pi}\frac{V_{DC}}{2}(Cos(n\theta_1) + Cos(n\theta_2) + Cos(n\theta_3) = V$$
$$Cos(5\theta_1) + Cos(5\theta_2)) + Cos(5\theta_3) = 0 \quad (3)$$
$$Cos(7\theta_1) + Cos(7\theta_2)) + Cos(7\theta_3) = 0$$

This is a system of three transcendental equations in the three unknown's θ_1, θ_2, and θ_3. There are many ways one can solve for the angles. One approach to solve the set of nonlinear transcendental (3), is to use an iterative method such as the Newton-Raphson method [12]. In contrast to iterative methods, the approach here is based on solving polynomial equations using the theory of resultants which produces all possible solutions [13], [14]. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Then the resultant method is employed to find the solutions when they exist. These sets of solutions have to be examined for its corresponding total harmonic distortion (THD) in order to select the set which generate the lowest harmonic distortion (mostly due to the 11^{th} and 13^{th} harmonics). The computed THD in percent is defined by

$$THD\% = \frac{\sqrt{V_3^2 + V_5^2 + V_7^2 + \cdots + V_{19}^2}}{V_1^2} \times 100 \quad (4)$$

IV. Simulation Study

The simulation of single phase seven level cascaded H-Bridge multilevel inverter using unequal dc sources was done using Simulink. In this proposed multilevel inverter, only eight switches are required to obtain the output voltage. More switches are required to achieve the same output voltage in the symmetrical type where equal dc sources are used. The main advantage of the multilevel inverter over conventional two level inverter is the voltage stress on each switch is reduced due to series connection of the switches. In case of the symmetrical type, the voltage of each switch is limited to the value of DC source. Since the proposed multilevel inverter uses unequal dc sources the voltage stress among the switches will be asymmetrically distributed. Hence care should be taken while selecting power switches for this type of configuration.

The simulation diagram of seven level cascaded H-Bridge multilevel inverter is shown in Fig.3. The spectrum of the output current is taken to determine the Total Harmonic Distortion (THD). The simulation results of output voltage, Load current and FFT spectrum of Load current were presented for various RL loads are shown in

Fig.4, Fig.5 and Fig.6. From the normalized FFT analysis shown in Fig.4(c) Fig.5(c) and Fig.6(c), it can be derived that the magnitude of lower order harmonics are very low and the magnitude of higher order harmonics are nearly equal to zero. A detailed THD for the different load is tabulated in the Table I. It is seen that the percentage of harmonics in the proposed multilevel inverter is less compared to classical inverter system.

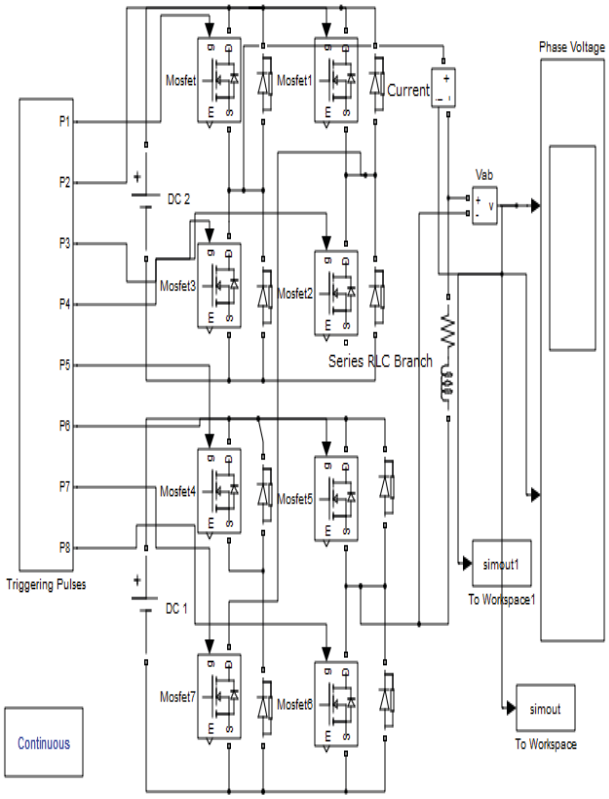
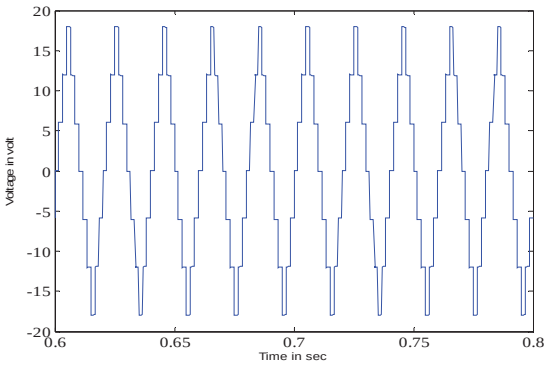


Fig.3: Simulation diagram of seven level cascaded H-Bridge inverter

Table I: Specifications adopted for the simulated parameters
V_{dc1}=12 V and V_{dc2}=6 V

R value	*L* value	THD (%)
11 Ω	125 mH	5.75
11 Ω	30 mH	7.07
22 Ω	30 mH	9.38



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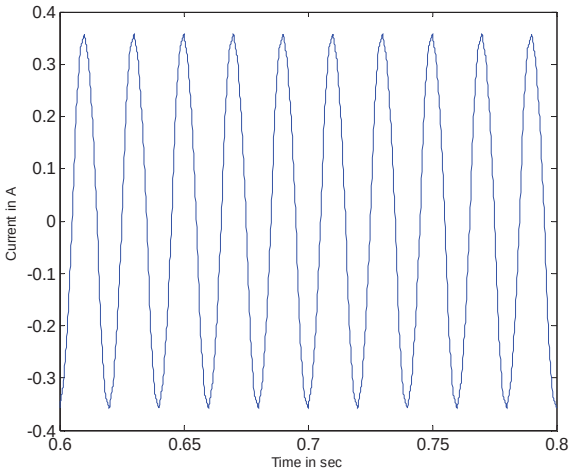

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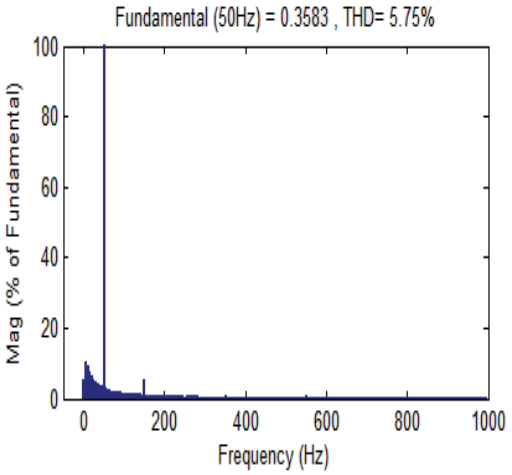
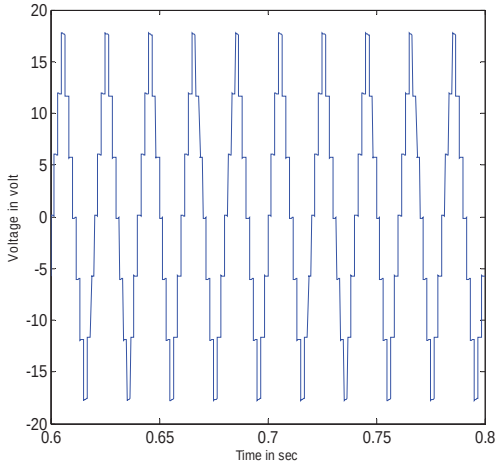


(c)

Fig.4: Simulation results for *R*= 11Ω, *L*= 125mH.
(a) Output voltage (b) Load current (c) FFT Analysis



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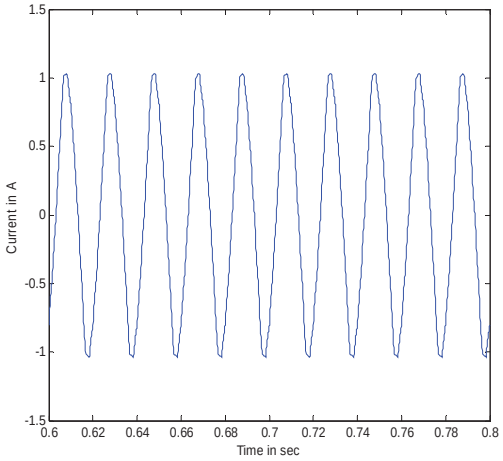

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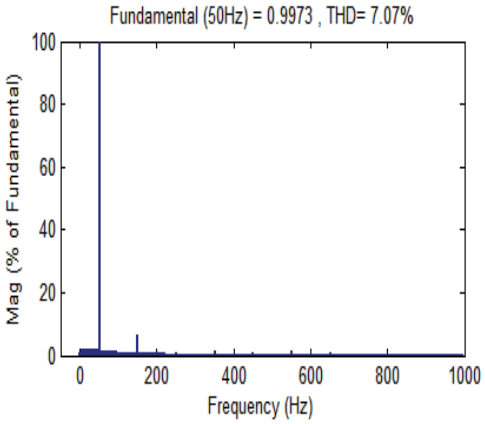
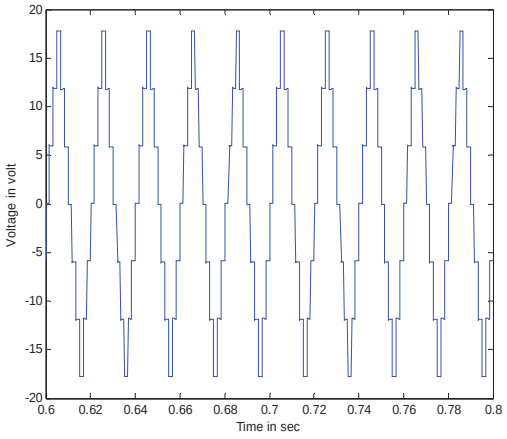
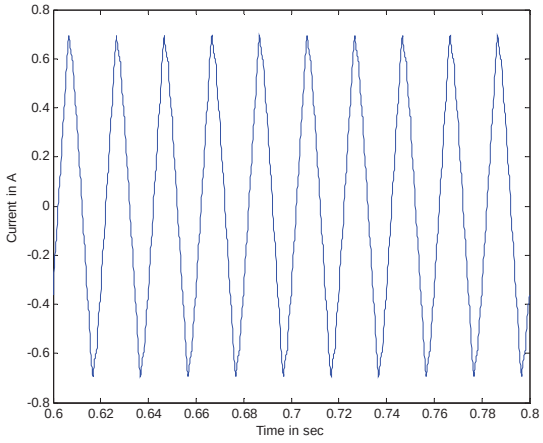


(c)

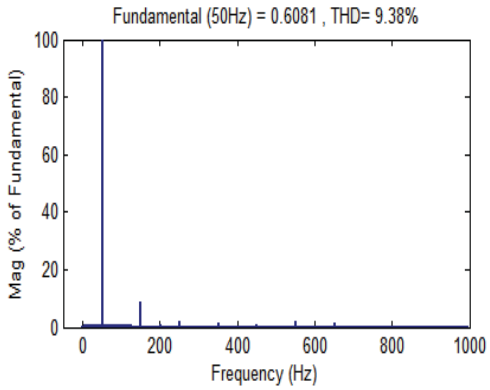
Fig.5: Simulation results for *R*= 11Ω, *L*= 30mH.
(a) Output voltage (b) Load current (c) FFT Analysis



(a)



(b)



(c)

Fig.6: Simulation results for *R*= 22Ω, *L*= 30mH.
(a) Output voltage (b) Load current (c) FFT Analysis

V. EXPERIMENTAL RESULTS

To experimentally validate the proposed multilevel inverter output voltage, hardware of single phase cascaded H bridge multilevel inverter has been built using MOSFET as the switching devices. A multi conversion cell consists of three 6 V batteries. One stage is supplied by 6 V and the other stage is supplied by 12 V (two 6 V Batteries are connected in series). A real time variable output voltage, variable frequency inverter controller based on ATmega16 Microcontroller is used to implement the control algorithm. An ATmega16 Microcontroller is used as the main processor, which provides gate signals.

According to microcontroller control signal, MOSFET gate terminal is turned on and off. Output of the inverter terminal is connected to RL load. The hardware block diagram and experimental setup of seven level Cascaded H Bridge Multilevel Inverter shown in Fig.7 and Fig.8. Hardware result of proposed multilevel inverter is exposed in Fig.9 and Fig.10. The output voltage of seven level cascaded multilevel inverter is 15 volt, with frequency of 50 Hz.

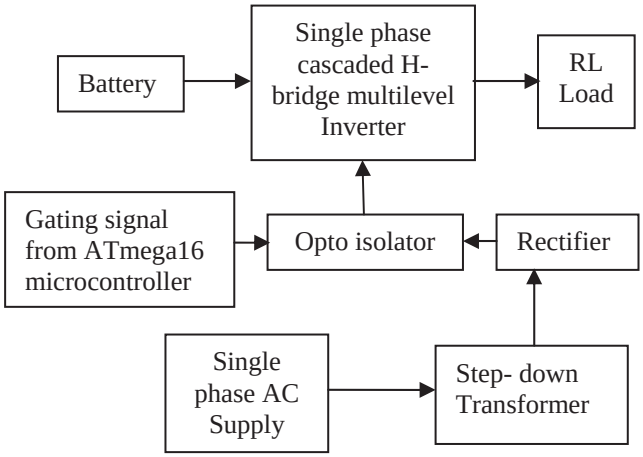


Fig.7: Block diagram of seven level cascaded H-bridge Inverter

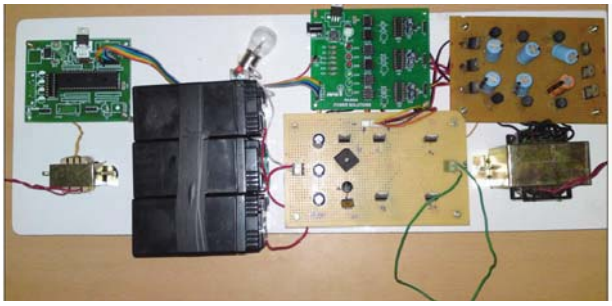


Fig.8: Experimental setup

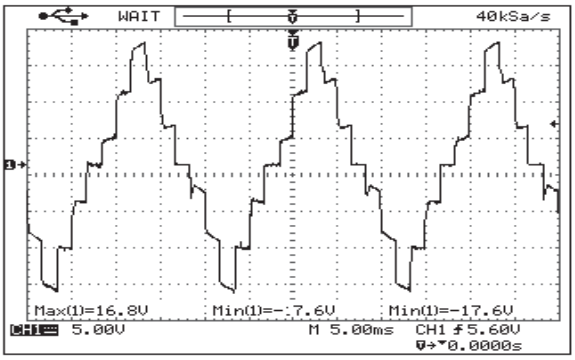


Fig.9: Output voltage of seven level cascaded H-bridge inverter

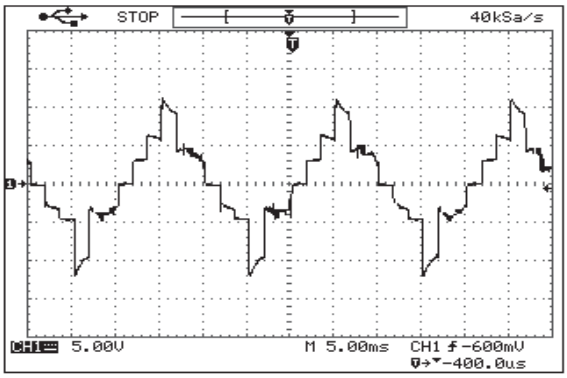


Fig.10:Output current of seven level Cascaded H-bridge inverter

VI. Conclusion

The proposed cascaded H-Bridge multilevel inverter uses unequal dc power source for producing desired multilevel voltage is simulated and validated by hardware. A fundamental frequency switching control algorithm was developed and implemented in the microcontroller. The total harmonic distortion is very low compared to that of classical inverter. The simulation results of load current waveform shows that the lower order harmonics have been reduced considerably and also higher order harmonics are eliminated.

The proposed multilevel inverter can be used for industries where the adjustable speed drives are required and significant amount of energy can be saved as the proposed system has less harmonics.

References

[1] J. S. Lai and F. Z. Peng, “Multilevel converters—A new breed of power converters,” *IEEE Trans. Ind. Applicat.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[2] L.M. Tolbert, F. Z. Peng, and T. G. Habetler, “Multilevel converters for large electric drives,” *IEEE Trans. Ind. Applicat.*, vol. 35, no. 1, pp.36–44, Jan./Feb. 1999.

[3] M. Klabunde, Y. Zhao, and T. A. Lipo, “Current control of a 3 level rectifier/inverter drive system,” in Conference Record 1994 IEEE IAS Annual Meeting, pp. 2348–2356, 1994.

[4] W. Menzies, P. Steimer, and J. K. Steinke, “Five-level GTO inverters for large induction motor drives,” *IEEE Trans. on Ind. Applicat.*, vol. 30, no. 4, pp. 938–944, July 1994.

[5] G. Sinha and T. A. Lipo, “A four level rectifier-inverter system for drive applications,” in Conference Record IEEE IAS Annual Meeting, pp. 980–987, October 1996.

[6] J. K. Steinke, “Control strategy for a three phase AC traction drive with three level GTO PWM inverter,” in *IEEE Power Electronic Specialist Conference (PESC)*, pp. 431–438, 1988.

[7] A. Maheswari, S. Mahendran and I. Gnanambal, “Implementation of fundamental frequency switching scheme on multilevel cascaded H-bridge inverter fed three phase induction motor drive ”, *Wulfenia journal*, vol 19, no. 8, pp. 10-23, Aug 2012.

[8] S. Bell and J. Sung, “Will your motor insulation survive a new adjustable frequency drive?,” *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 1307–1311, Sept./Oct. 1997.

[9] J. Erdman, R. Kerkman, D. Schlegel and G. Skibinski, “Effect of PWM inverters on AC motor bearing currents and shaft voltages,” *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 50–259, Mar./Apr.1996.

[10] A. H. Bonnett, “A comparison between insulation systems available for PWM-inverter-fed motors,” *IEEE Trans. Ind Applicat.*, vol. 33, pp.1331–1341, Sept./Oct. 1997.

[11] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. Van Coevering, “A multilevel voltage-source inverter with separate dc sources for static var generation,” *IEEE Trans. Ind. Applicat.*, vol. 32, pp.1130–1138, Sept./Oct.1996.

[12] Patel. H.S. and Hoft, R.G, “Generalized techniques of harmonic elimination and voltage control in thyristor

Inverters: Part I – Harmonic Elimination", *IEEE Trans. Ind.Appl*., vol. 3, pp.310-317, 1973.

[13] Chiasson, J.N., Tolbert, L.M., Mckenzie, K.J. and Du Z., "Control of a Multilevel Converter Using Resultant Theory", *IEEE Trans. Control Syst. Technol*., vol. 11, no.3, pp. 345-354, 2003.

[14] J. Chiasson, L. Tolbert, K. McKenzie, and Z. Du, "Elimination of harmonics in a multilevel converter using the theory of symmetric polynomials," *IEEE Trans. Control Syst. Technol.*, vol. 13, no. 2, pp. 216–223, March 2005.

[15] Z. Du, L. M.Tolbert and J. N. Chaisson, "Modulation extention control for multilevel converters using triplen harmonic injection with low switching frequency," in Proc. IEEE Appl. Power Electron. Conf., Austin, TX, pp. 419-423, Mar., 2004.

BIOGRAPHIES

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