

Transformer-less Pulse Power Supply: A Prototype Development

S K Rai ¹ P Tandon ² S Jangid ³ Rahul Varma ⁴

Abstract– High voltage pulse generators find extensive use in characterization and testing of high power microwave tubes and plasma devices along with many others industrial applications. The solid-state devices based method is now more popular than the pulse-forming network (PFN) based design, which is an old technique. However, both the methods entail the design of pulse transformer, which involves very critical design issues. This paper describes the prototype design and development of transformer-less pulse power supply, which is based on popular topology “Marx Generator”.

Keywords– Marx Generator, pulsar, droop, isolation, PRF

I. INTRODUCTION

Today, rectangular electrical pulses of high-voltage and high-frequency have many industrial applications. Some typical applications evolve in surface treatment techniques, food sterilization, waste treatment, characterization of microwave and plasma devices etc [1-3].

Several kinds of models have been widely used for the pulse power supply such as Marx generator, hard-tube type pulse generator, Thyatron type pulse power generator with pulse forming network (PFN) etc [4-6]. The pulse width and shape of these kinds of pulse power supply are load dependent. These generators are usually designed for fixed pulse width and load.

Now days, solid-state devices based pulse generators are more popular. However, the maximum pulse width, overshoot, pulse droop and pulse shape are limited by pulse transformer design, which involves very critical design issues. The Marx Generator topology based transformer-less pulse power supply is new advancement in this. It is completely based on solid-state devices and capacitors charging and discharging [5-12].

In the past, Marx Generators were usually implemented using spark gap technology and had low pulse repetition rates [13]. In recent years, Marx generators based on semiconductor switches are proposed for high pulse repetition rates [14-15].

This paper describes the simple design and prototype development of transformer-less pulse power supply based on “Marks Generator” topology.

The paper first received 24 Dec 2012 and in revised form 22 Dec 2013.

Digital Ref: APEJ-2013-10-422

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The design calculation is done for Input Voltage = 800V, Output voltage up to 15kV, f_s = up to 10kHz, Pulse Width up to 5 μ s, Droop = 10% and Maximum Pulse Current = 1A.

A combination of 20 modules with suitable gate drivers is used in this application.

II. SYSTEM DESCRIPTION AND DESIGN

The schematic diagram of proposed pulsar is shown in Fig. 1. Incoming single-phase ac supply is rectified and filtered after step-up using transformer and the output dc is controlled by using a variac. The available output dc voltage charges the capacitors (C_1 to C_{20}) using IGBTs (Q_1 to Q_{20}) for specified time and after some delay IGBTs (Q_{21} to Q_{40}) connects all the capacitors in series and so produces the required high pulse to the connected load. Diodes (D_1 to D_{40}) are used to provide unidirectional current flow in both charging and discharging of capacitors.

This system has twenty sub-modules as per design. A single sub-module is shown with the dotted rectangular box (Fig. 1).

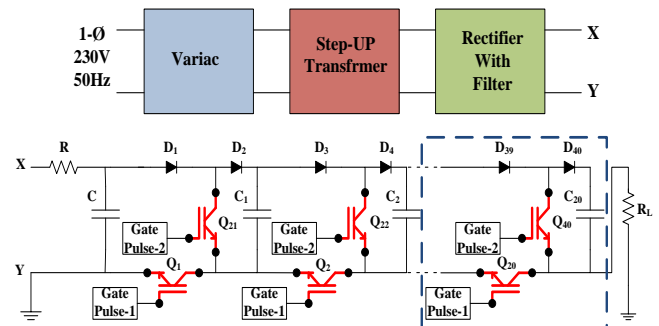


Fig. 1: Schematic diagram of proposed pulsar

The schematic diagram of developed prototype is shown in Fig. 2. Only three sub-modules are tested and an isolation transformer is used for isolation purpose at input side.

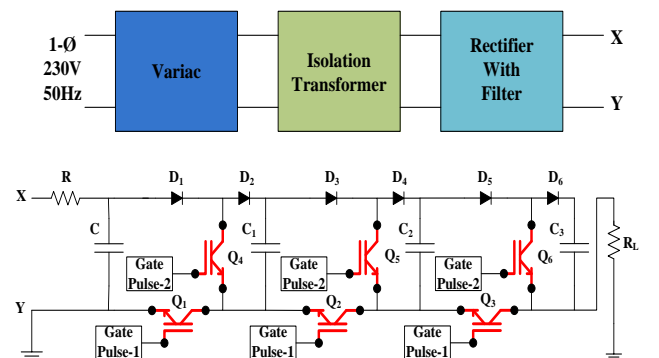


Fig. 2: Schematic diagram of developed prototype

The working of the prototype can be understood by capacitors charging schematic diagram (Fig. 3) and discharging schematic diagram (Fig. 4). Initially, when gate pulse-1 is applied to IGBTs (Q_1 to Q_3), all the capacitors (C_1 to C_3) are connected in parallel fashion to the DC voltage source and charged fully (Fig. 3). During this period load is connected to ground via IGBTs and so the output voltage is about zero. After charging, gate pulse-2 is applied with some delay to the IGBTs (Q_4 - Q_5), all the capacitors are connected in series and the voltage ($V_c+V_{c1}+V_{c2}$) is appeared across the connected load (Fig. 4). During series connection, capacitors discharge and in the next cycle again these are charged fully and so on. All the diodes are forward biased during charging time but during discharging only odd numbered diodes (D_1, D_3 & D_5) work, rest of the diodes (Even numbered: D_2, D_4 & D_6) are in reverse biased mode and prevent capacitor discharge by short circuit.

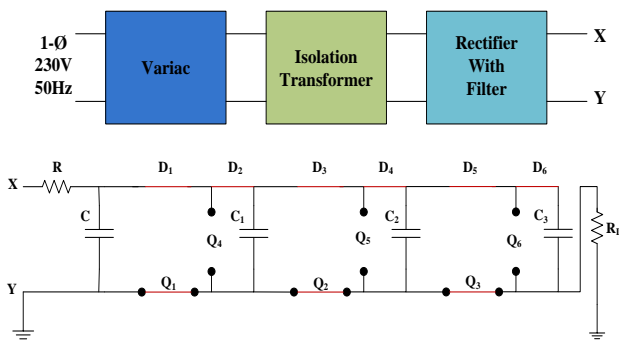


Fig. 3: Schematic diagram of capacitors charging

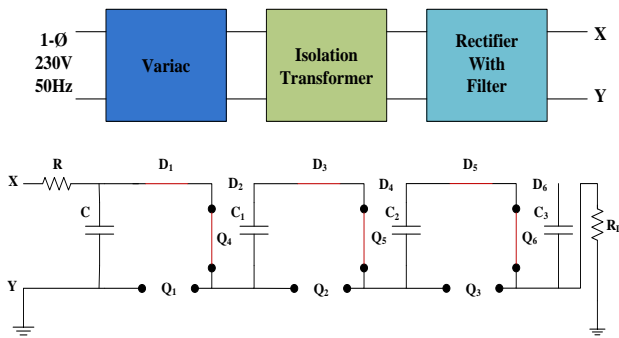


Fig. 4: Schematic diagram of capacitors discharging

Each IGBT has its own isolated gate pulse and gate drive supply. The gate pulses are applied using fiber optic. The gate pulse width of charging IGBTs is fixed but for series connecting IGBTs, it is variable and so the output pulse varies accordingly. The prototype is tested with resistive load. Moreover, no pulse transformer is required in this approach. Details of design calculation and construction of sub-systems are discussed in the following sub sections.

A. Design Calculations

Design Specifications:

- Input Voltage: up to 800V
- Output Voltage: up to 15kV
- Pulse width: up to 5µs
- Pulse Frequency: up to 10kHz
- Droop: 10%
- Maximum pulse current: 1A

$$No.of\ Modules = \frac{MaxoutputVoltage}{MaxInputVoltage} = \frac{15kV}{800V} = 18.75$$

$$C_{equ.} = \frac{MaxPulseCurrent \times MaxPulseWidth}{Droop} = \frac{1A \times 5\mu s}{10\% \text{ of } 15kV} = 3.3nF$$

$$SingleCapacitorValue = C_{equ.} \times (No.ofModules + 1) = 3.3nF \times 21 = 69.3nF$$

$$CapacitorVoltageRating > MaxInputDCvoltage(800V)$$

$$PeakDiodeCurrent > \frac{MaxInputDCvoltage}{R = 50\Omega} = \frac{800V}{50\Omega} = 16A$$

$$AverageDiodeCurrent >$$

$$PeakDiodeCurrent \times MaxPulsewidth \times MaxFrequency = 16A \times 5\mu s \times 10kHz = 0.8A$$

$$PeakInverseVoltage\ of\ Diode > MaxInputDCvoltage = 800V$$

$$Max(V_{CE})\ of\ IGBT > MaxCapacitorvoltage = 800V$$

So twenty modules are decided as per above calculation with resistance $R=50\Omega$, which is decided as per the required charging time of the capacitor. All the capacitors (C & C_1 to C_{20}), all diodes and all IGBTs are selected $1\mu F/2kV$, 6FMLR120 (6A/1200V) and IXGH15N120CD1 (30A/1200V) respectively with the reference of above calculations. The fixed gate pulse width of $80\mu s$ is decided for charging IGBTs.

B. Gate Pulse Generator

The optical coupling based open loop gate pulse generator has been designed to trigger the IGBTs [16].

Gate Pulse Generator Specifications:

- Pulse Frequency: up to 10kHz
- Pulse-1 (for charging IGBTs): $80\mu s$ (Fixed)
- Pulse-2 (for series Connecting IGBTs): up to $5\mu s$
- Delay (Pulse-1 to Pulse-2): $10\mu s$ (Fixed)

The above specified gate pulses details are generated using the concept as shown in Fig. 5 and realized by using NE555 and 4047BP as shown in Fig. 6, which has both pulse width and frequency control facilities. The generated gate pulses are transmitted optically by using transmitter HFBR1521. Since, same pulse is required by several IGBTs, so ULN2003 (Seven Darlington Array) is used with transmitters. The pulse generator system is shown in Fig. 7.

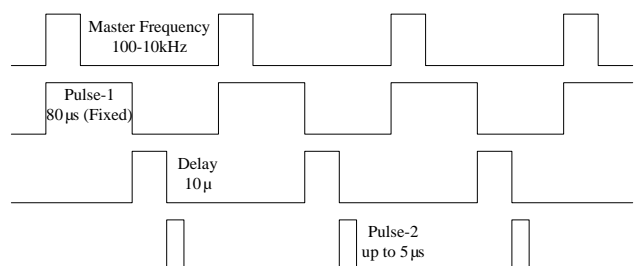


Fig. 5: Followed concept to generate of gate pulses

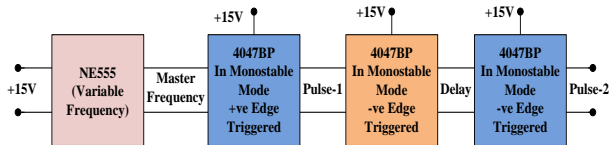


Fig. 6: Block diagram of pulse generator

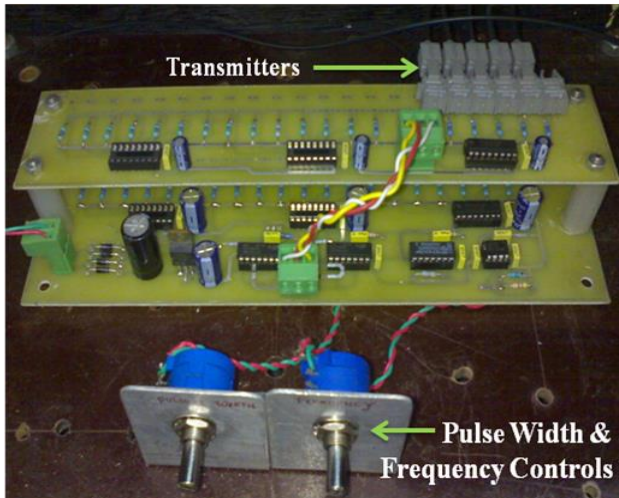


Fig. 7: Pulse generator system

C. Isolated Gate Driver

The required floating gate drive supply for all IGBTs is realized with simple arrangement as shown in Fig. 8 [16]. A high voltage insulated wire acts as primary of the transformer, which passes through the ferrite ring core behaving as secondary. It is driven by low voltage high frequency inverter (15V, 20kHz). The induced voltage in the secondary is rectified, filtered and regulated to generate isolated gate drive supply for each IGBT. The optically transmitted gate pulse is received and transferred into the electrical pulse using optical receiver HFBR2521. The gate driver IXDD414CI is used for fast switching of IGBTs. The inverter system, gate driver system with optical receiver, gate driver power supply and received gate pulses waveform are shown in Fig. 9, 10, 11, 12 and 13 respectively.

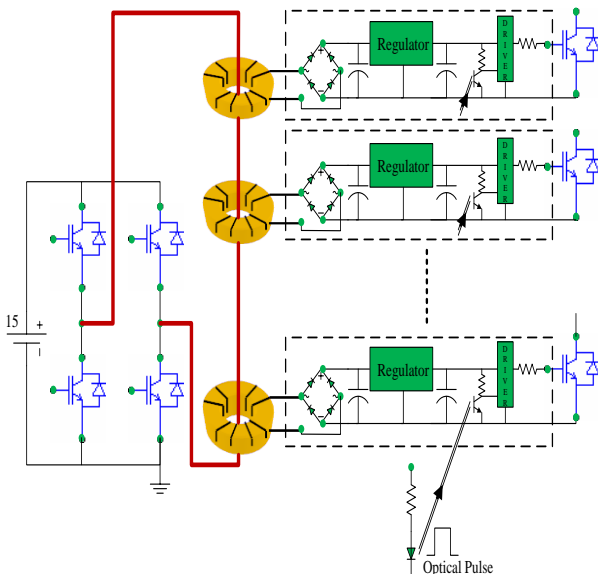


Fig. 8: Schematic diagram of floating gate drive supplies and controls

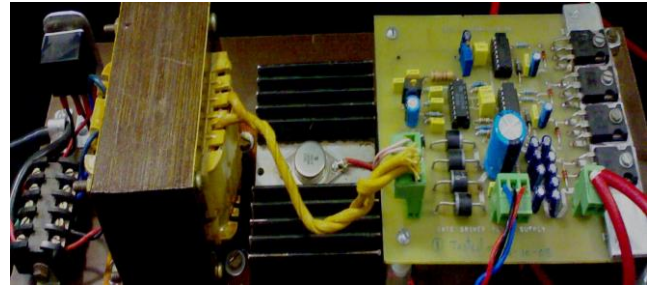


Fig. 9: Inverter of gate drive supplies

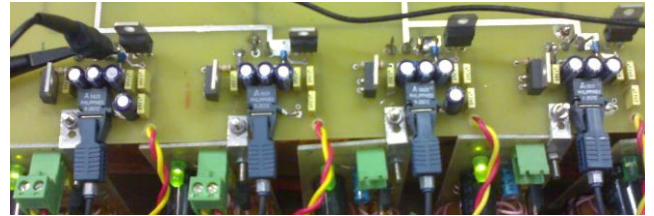


Fig. 10: Gate drivers with optical receiver



Fig. 11: Gate drivers power supply

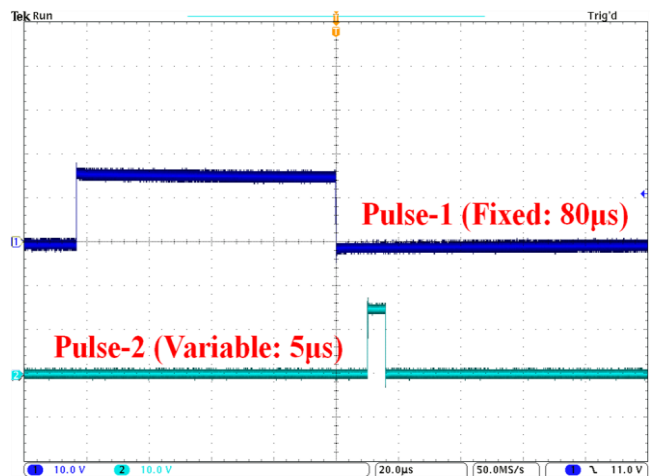


Fig. 12: Received gate pulses (Both waveforms: 10V/div, 20µs/div)

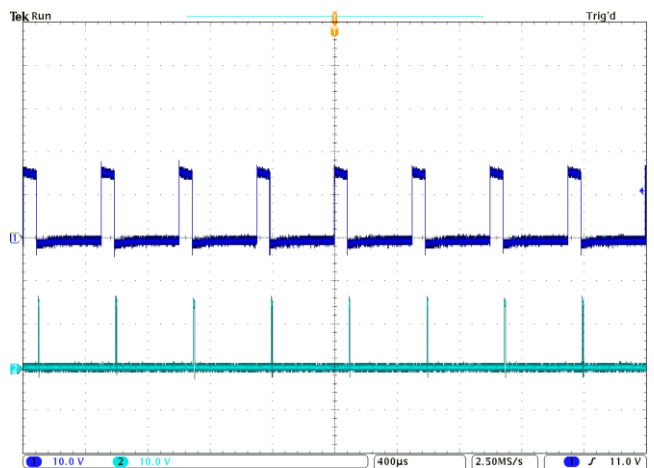


Fig. 13: Received gate pulses [Multiple Pulses- Upper: Pulse-1, Lower: Pulse-2 (Both waveforms: 10V/div, 400µs/div)]

III. TEST RESULT

Presently, the prototype is tested with only three modules as shown in Fig. 2 but design calculations are considered for twenty modules as shown in Fig. 1.

The test results are shown for the input DC voltage of 200V and output voltage is obtained 600V, which is as per the design. The developed prototype is tested successfully with resistive load for maximum rated pulse current at 600V pulse voltage, over the entire range of the pulse width and pulse repetition frequency (PRF).

The rise time of the output pulse is found about 30ns. However, the induced noise at the gate of the charging IGBTs at switching time of series connecting IGBTs is an issue to be rectified.

The test setup, developed prototype, top view of prototype and different waveforms are shown in the figures given below.



Fig. 14: Test setup

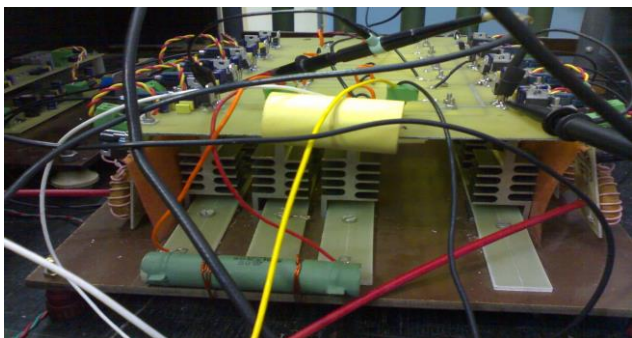


Fig. 15: Developed prototype

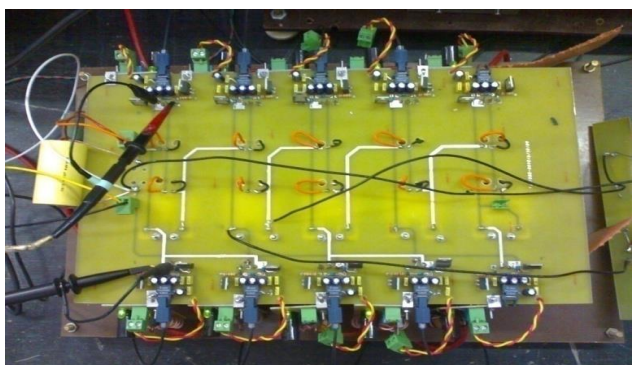


Fig. 16: Top view of developed prototype

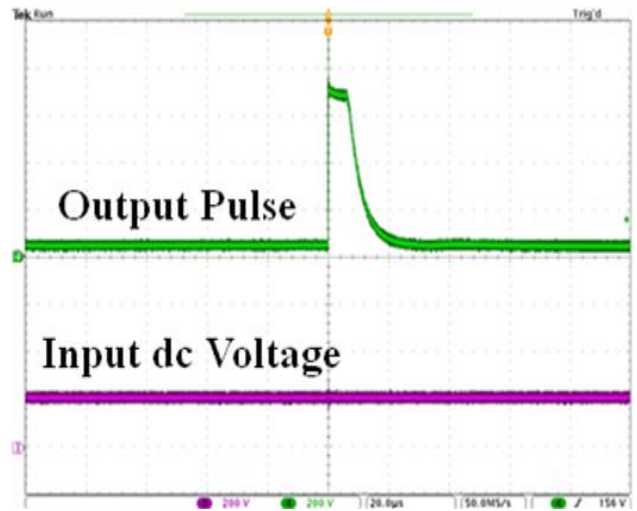


Fig. 17: Output pulse with input dc voltage (Both waveforms: 200V/div, 20 μ s/div)

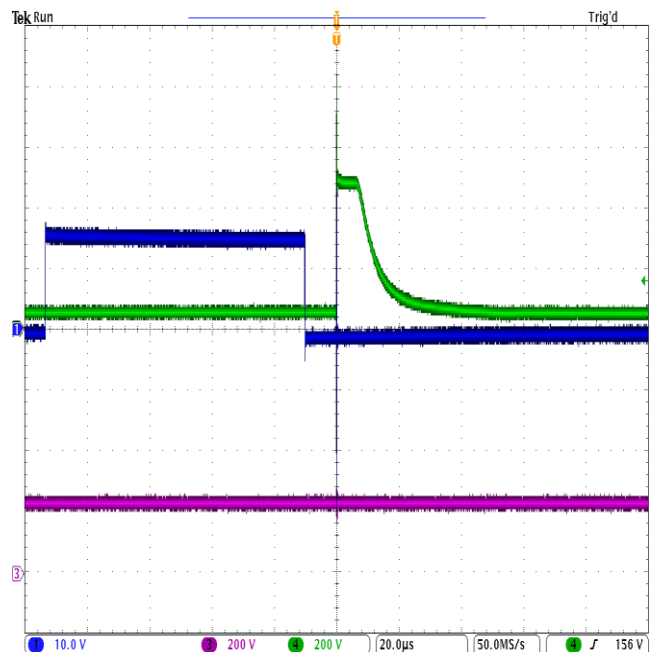


Fig. 18: Output pulse (Upper) with input dc voltage (Lower) and gate pulse-1 (Middle) (Both waveforms: 200V/div, 20 μ s/div)

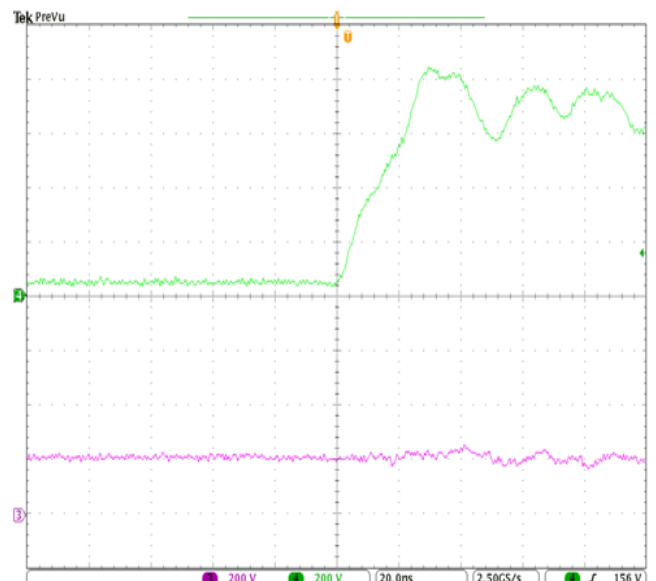


Fig. 19: Rise time of output pulse (about 30ns) (Upper: Output Pulse, Lower: Input DC voltage, Both waveforms: 200V/div, 20ns/div)

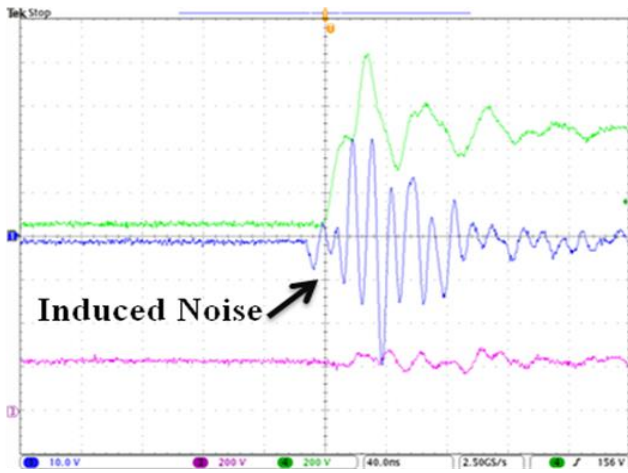


Fig. 20: Induced noise at the gate of charging IGBT (Upper: Output Pulse, Middle: Induced Noise, Lower: Input DC voltage, Upper & Lower waveforms: 200V/div, 40ns/div, Middle waveform: 10V/div, 40ns/div)

IV. CONCLUSION

In this paper, the design and development of the prototype of transformer-less pulse power supply based on “Marx Generator” are described. The design calculations are done for the following specification:

- Input Voltage: up to 800V
- Output Voltage: up to 15kV
- Pulse width: up to 5 μ s
- Pulse Frequency: up to 10kHz
- Droop: 10%
- Maximum pulse current: 1A

The optical coupling based open loop gate pulse generator has been designed to trigger the IGBTs, which has following specifications:

- Pulse Frequency: up to 10kHz
- Pulse-1 (for charging IGBTs): 80 μ s (Fixed)
- Pulse-2 (for series Connecting IGBTs): up to 5 μ s
- Delay (Pulse-1 to Pulse-2): 10 μ s (Fixed)

As per the design, twenty modules have been selected to achieve required output. The test results for the prototype with three modules have been presented and are found as per design and requirement.

REFERENCES

[1] Tian et. al., “Special modulator for high frequency, low-voltage plasma immersion ion implantation,” *Review of Scientific Instruments*, vol. 70, no. 3, pp. 1824-1828, Mar. 1999.

[2] M. P. J. Gaudreau, T. Hawkey, J. Petry and M. Kempkes, “A solid state pulsed power system for food processing,” in *Proceed. Pulsed Power Plasma Science*, vol. 2, pp. 1174-1177, 2001.

[3] E. L. Neau, “Environmental and Industrial Applications of Pulsed Power Systems,” *IEEE Transactions on Plasma Science*, vol. 22, no. 1, pp. 2-10, February 1994.

[4] E. G. Cook, “Review of Solid-State Modulators,” Presented at the XX International Linac Conference, Monterey, Aug. 2000.

[5] Willis, W. L.: “Pulse-Voltage Circuits”, Chapter 3 de “High Power electronics”, Editor Dollinger, R. E.; Sarjeant, W. James, Tab Books Inc., 1st Edition, 1989, ISBN 0-8306-9094-8.

[6] D. M. Goebel, “Pulse Technology”, Chapter 8 “Handbook of Plasma Immersion Ion Implantation & Deposition,” Editor Anders, Andr e 1st edition, John Wiley & Sons, New York, p.p. 760, ISBN 0-471-24698-0, 2000.

[7] J. O’Loughlin,; J. Lehr and D. Loree, “High repetition rate charging a Marx type generator,” in *Proceed. Pulse Power Plasma Science*, vol. 1, pp. 242- 245, June 2001.

[8] K. Okamura, S. Kuroda, M. Maeyama, “Development of the high repetitive impulse voltage generator using semiconductor switches,” *12th Pulsed Power Conference, Digest of technical Papers*, vol. 2, pp. 27-30, 1999.

[9] R. L. Cassel, “A Solid State High Voltage Pulse Modulator which is Compact and without oil or pulse transformer,” *Power Modulator Conf.*, May 23-26, San Francisco CA, 2004.

[10] L. M. Redondo, J. Fernando Silva, P. Tavares and E. Margato, “All Silicon Marx-bank topology for high-voltage, high-frequency rectangular pulses,” in *Proceedings of the 2005 IEEE 36th Annual Power Electronics Specialists Conference*, 12-16 June, Recife, Brasil, pp. 1170-1174.

[11] Jong-Hyun Kim et al., “High Voltage-Pulse Power Supply Using Marx Generator & Solid-State Switches,” in *Proceedings of the Industrial Electronics Society, 2005, IECON, 2005 32nd Annual Conference of IEEE Annual Conference of the IEEE*, pp. 1244-1247, 6-10 Nov., 2005.

[12] W. J. Carey, and, J. R. Mayes, “Marx generator design and performance,” *24th Power Modulator Symposium and High-Voltage Workshop*, pp. 625-628, 2002.

[13] J. R. Mayes and W. J. Carey, “Spark Gap Switching with Photoconductive Switches,” *12th IEEE International Pulse Power Conf. (Monterey, California)*, pp. 1203-1206, 1999.

[14] S. G. E. Pronko, M. T. Ngo, and R. F. K. Germer, “A solid-state Marx-type trigger generator,” *8th Power Modulator Symposium*, pp. 211 – 214, 1988.

[15] M. D. Grimes and T. E. Owen, “A High-Repetition Rate, Solidstage, Marx-Bank Pulse Generator for Geophysical Instrumentation”, *12th Power Modulator Symposium*, 1992, pp. 181.

[16] S K Rai, P Tandon, S Jangid and Rahul Varma, 2013. A Trigger System with High Voltage Isolation for Multiple Switching Devices. *International journal of Electronics and Communication Engineering &Technology (IJECET)*. Volume: 4, Issue: 7, Pages: 155-162.

ACKNOWLEDGMENT

The authors would like to thank CSIR-CEERI, Pilani and B K Birla Institute of Engineering & Technology (BKBIET), Pilani for supporting this work.

BIOGRAPHIES



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