A Soft-Transition Control Strategy of Multilevel Inverter for Three-Phase Induction Motor Drive

M. S. Ballal [1] H. M. Suryawanshi [2]

Abstract–This document presents a soft transition control strategy of 5-level inverter for low voltage application. The proposed strategy is realized by introducing RL resonance tank with two additional switches and obtaining the switching pattern and timing of the main switches and two auxiliary switches. This improvement in inverter eliminates the voltage spike caused by recovery diode and remove lossy RC snubber. Further it can be operated at higher frequency as compared to conventional two-level inverter. The soft transition for each phase is executed independently from the main controller. The operating principle for proposed control scheme is described in this paper. The circuit operation is verified by computer simulation and experimentation.

Keywords–Induction motor drive, multilevel inverter, soft switching

I. INTRODUCTION

Multilevel inverters are nowadays the preferred choice for high-voltage and high-power applications in industry and these inverters have changed the face of medium- and high-voltage drives. A zero-voltage transition (ZVT) soft-switching inverter for an induction motor drive is developed in [1]. The proposed soft-switching inverter is formed from the traditional pulse-width modulated (PWM) inverter by simply augmenting with auxiliary resonant circuits, and the soft switching is achieved through applying PWM switching control signals with suitable delays for the main and auxiliary switches. A zero-voltage-switching pulse width-modulation three-level (ZVS PWM TL) converter is described in [2] which introduce two clamping diodes to the basic ZVS PWM TL converter. The operation principle of the novel converter and the simplified converter are analyzed and are verified by a prototype converter. Zero-Current-Transition inverter topology that uses only three auxiliary switches is proposed in [3]. It reduces the number of auxiliary switches by half from the existing topologies and still achieves desirable soft-commutation performance. Its operation based on normal pulse width modulated (PWM) algorithms.

Different topologies for high efficient three-level half bridge-inverters were discussed and compared in [4]. The losses are calculated and measured over a wide range of load power factor from nearly purely inductive to capacitive. Several methods for the calculation of losses were compared and the selection of the components for a prototype was described. Three-level topologies as alternatives to two-level topologies in converters for low-voltage applications are evaluated in [5]. Topologies, semiconductor losses, filter aspects, part count, initial cost, are compared for a grid interface, a conventional drive application, and a high-speed drive application. Three-level topologies are highly attractive for low-voltage power converters, specifically for applications with medium to high switching frequencies. A multi-path harmonic elimination and sideband reduction scheme in SPWM signal processing has been presented with a view to improving efficiency in a dc to ac inverter application is discussed in [6].Work is carried out in Mat Lab simulation and harmonic cancellation approach is defined.

A five-level inverter scheme for the open-end winding induction motor drive is proposed in [7], with a reduced power circuit complexity when compared to the existing scheme. The five-level structure is realized by cascading two conventional two-level and three-level inverters. Efficiency analysis and comparison of three-phase and DTP induction motor drives fed by PWM VSI is described in [8]. The proposed comparison uses a high frequency, DTP induction motor prototype developed for low/medium power applications. The comparison should be performed at the same dc bus voltage and deliver the same power (three-phase currents about two times the DTP ones). However, the efficiency is not a discriminatory parameter in evaluating the performances and the advantage/disadvantages of three-phase and DTP induction motor drives fed by PWM VSI.

The performance of a novel multilevel six-switch (SS) three-phase inverter drive is examined in [9] for low-voltage high-speed motor applications. The multilevel inverter structure examined offers an increased number of output pulse width-modulated (PWM) voltage levels, higher frequency PWM output waveforms, reduced dead-time effects, and a significant reduction in harmonic content. A series connection of three-level inverters has been proposed in [10] for a medium-voltage sensor less vector control squirrel-cage induction motor (SQIM) drive with increased voltage capacity. The disadvantage of this topology is that it requires additional output transformers which introduce additional cost and losses. A comparison study for a cascaded H bridge multilevel DTC induction motor drive is discussed in [11]. The carried out experiments shows that an asymmetrical configuration provides nearly sinusoidal voltages with very low distortion, using less switching devices. DTC solution for high-power induction motor drives, not only due to the higher voltage capability provided by multilevel inverters, but mainly due to the reduced switching losses and the improved output voltage quality, which provides sinusoidal current without output filter.

Article [12] has presented SVM method for the dual-inverter five-phase open-end winding topology, which is

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relatively easy to implement. The scheme utilizes two standard five-phase two level SVM modulators, one for each inverter, and apportions the voltage reference unequally between the two inverters. However, it should be noted that, the principle of SVM is directly applicable to all vector control schemes, which operate with current control in the rotating reference frame so that the control system output is the stator voltage reference.

In this paper, new soft-switching control strategy for five levels diode-clamped inverter used for three phase induction motor drive is presented. This soft-switch inverter uses auxiliary circuit consisting of two auxiliary switches and resonant tank. Number of auxiliary component used in this strategy is significantly less than previous control strategies. Also thermal and current stresses are evenly distributed on auxiliary switches. The operating principles for proposed control scheme with different operating mode are described in this paper. The developed scheme is verified via detailed simulations and experimental results.

II. Soft Transition Control Strategy for Multiple Inverter

A soft transition control strategy for proposed one leg of three-phase multilevel inverter is shown in Fig. 1. The circuit arrangement consist of one phase leg of 5-level inverter, auxiliary circuit which includes resonant tank consisting inductor L and capacitor C and auxiliary pair of switches S_{x1} and S_{x2} . It means switch S_{x1} is consist of similar type of two switches to sustain the voltage stresses across it. Similarly, for this reason switch S_{x2} is also provided in pair. Operation of 5-level inverter is explained in [6]. Structure of 5-level inverter contains 4 complimentary switch pairs i.e. S_1-S_5, S_2-S_6, S_3-S_7, S_4-S_8. Since the bi-directional inverter load current I_L is conducted in a totem-pole manner, only one switch of these complimentary switch pair needs to be soft-switched for each phase during each half-load-current-line cycle. Instead of tracing load current I_L every time for its direction, a common scheme is develop to achieve soft transition of corresponding complimentary switch pair. Complimentary switch pair S_1-S_5 is consider for explaining proposed soft-transition strategy. Equivalent circuit diagram for proposed soft-transition scheme when switch S_1 and S_5 are involved is shown in Fig.2. Same explanation is applicable for other switch pairs.

Procedure for proposed method is divided in two part, first part consider soft transition of switch S_1 for positive load current ($I_L > 0$) and second part gives the soft-transition for switch S_5 for negative load current ($I_L < 0$). To simplify the analysis the circuit parasites, such as the semiconductor junction capacitors and stray inductors are ignore. I_L and dc bus voltage V_{dc} are assumed to be constant among the switching cycle.

A. Load current more than zero: Condition when $I_L > 0$, the positive half-load-current-line cycle

Current I_L is conducted through S_1 and clamping diode D_{C1}. Operation goes through five stages as shown in Fig. 4. The operating waveform in one switching cycle is shown in Fig. 3. The initial stage is that I_L is carried by D_{C1}. In steady state there is positive voltage $V_x = V_{dc}/4$ across resonant capacitor C.

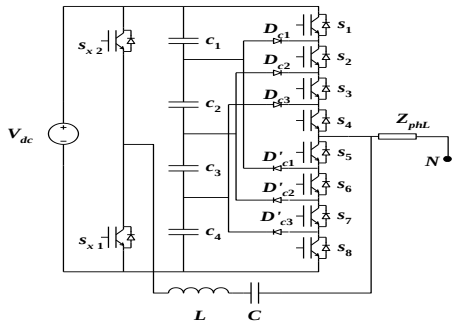


Fig.1. Proposed soft transition multilevel inverter (one leg) with auxiliary circuit

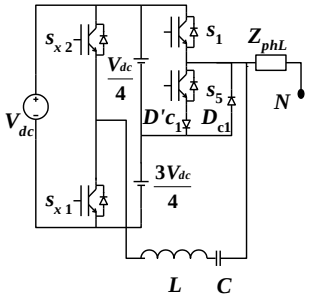


Fig. 2. Equivalent circuit diagram for soft-switch multilevel inverter when switches S_1-S_5 are involved.

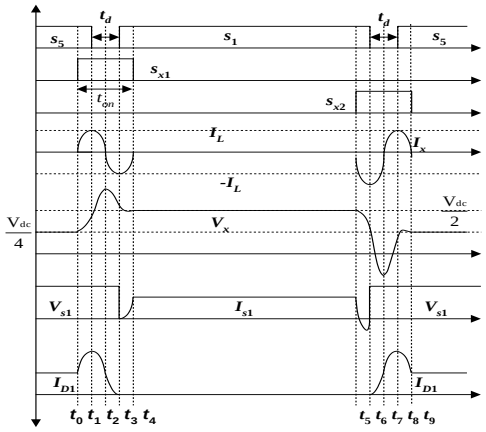


Fig. 3 Idealized waveform of the proposed soft-transition strategy for $IL > 0$.

1. *Mode*-I ($t_0 - t_2$): Fig.4 (a), S_{x1} is first turn on at t_0, with this auxiliary circuit start resonating and resonant current I_x starts increasing. I_x starts flowing through D_{c1} with load current I_L in same direction. Thus, effective current through D_{c1} starts increasing. I_x reaches to its peak value at t_1. After t_1, I_x starts decreasing and reaches to zero at t_2. At this instant voltage across capacitor V_c is at its peak value which is greater than $V_{dc}/2$. Since in this mode no current is flowing through switch S_5, it can be turn off without any switching losses. It is turn off at t_1.

2. *Mode*-II (t_2- t_4): Fig.4 (b), after t_2 I_x increases in opposite direction. As current in D_{c1} also starts decreasing, this negative I_x is carried by anti-parallel diode D_{sx1} of auxiliary switch S_{x1}. At t_3, I_x reaches to its negative peak value ($-I_L$), therefore effective current through D_{c1} become

zero. At this instant Switch S_1 is turn on and its turn-on is achieved with zero current and zero switching losses. After t_3 I_x goes on decreasing and at t_4 it reaches to zero value. Gating signal of S_{x1} is removed at this instant so that its turn-off is achieved with ZCS.

3. *Mode*-III (t_4 – t_5): Fig.4(c), during this mode PWM operation resume for switch S_1 and normal I_L flow through S_1.

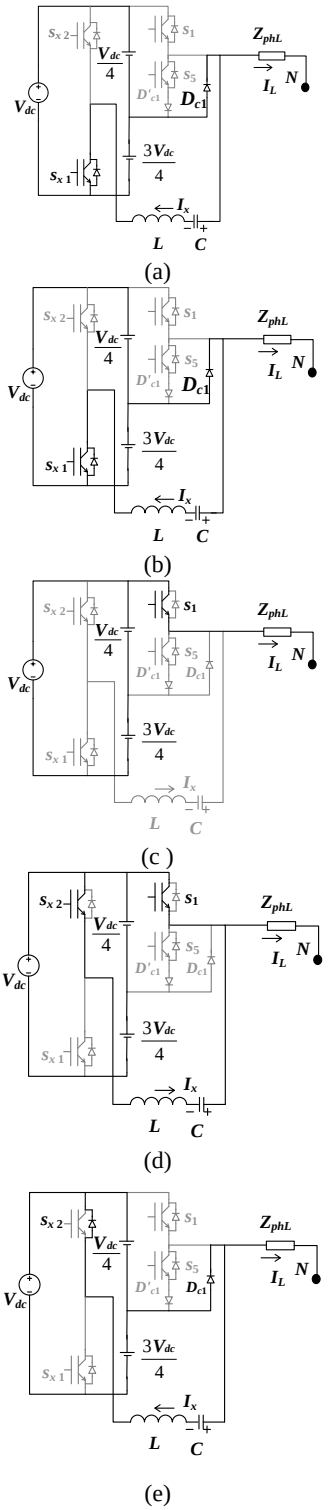


Fig. 4. Topological stages of soft switch multilevel inverter during time interval $t_1 - t_9$ for $I_L > 0$.

4. *Mode*-IV (t_5 – t_7): Fig. 4(d), before S_1 is turn off S_{x2} is turn on at t_5 and auxiliary circuit again starts resonating with increasing value of I_x in negative direction. I_x reaches to its peak value at t_6 which is greater than I_L. As I_x is flowing through S_1 with I_L , current through S_1 decreases to zero and surplus current is carried by anti parallel diode D_1. Gating signal to S_1 is removed at t_6 and turn off of S_1 is achieved with ZCS. After t_6, I_x and I_L is carried by clamping diode D_{c1}.I_x returns to zero at t_7, where V_c achieve its peak value which is less than V_{dc}/4.

5. *Mode*-V (t_7 – t_9): Fig.4 (e), after t_7, I_x starts increasing in opposite direction. This I_x is carried by anti-parallel diode D_{sx2}. As I_L and I_x flow in same direction through clamping diode D_{c1} effective current through it starts increasing. Current I_x reaches to its peak value at t_8 after which it decreases and reaches to zero at t_9. Gating signal to S_{x2} is removed at t_9, so its turn off is also achieve with ZCS.

B. Load current less than zero: Condition when $I_L < 0$ the negative half-load-current-line cycle.

In this case current I_L is conducted through S_5, clamping diode D_{c1}' and anti-parallel diode D_1 of switch S_1. To make explanation linked with case for $I_L > 0$, operation begins with turn off transition of S_5. The initial stage is that I_L flows through S_5. Assumption for this mode is same as that for $I_L > 0$ case. Operating waveform in this case is given in Fig. 5 and five mode of operation is given in Fig. 6.

1. *Mode*-I (t_0 – t_2): Fig 6(a), S_{x1} is turn on at t_0.With this auxiliary circuit starts resonating and I_x increases in positive direction. Before this S_5 is carrying load current I_L. With start of resonance, current through S_5 is sum of load current I_L and resonant current I_x. Hence, effective current through S_5 start decreasing. At t_1, I_x reaches to its peak value equal to I_L. As a result current through S_5 become zero and gating signal to S_5 is removed to achieve ZCS for S_5. After this I_L and I_X is carried by anti-parallel diode D_1 of switch S_1. At t_2, I_x become zero and voltage across capacitor C reaches to its peak value.

2. *Mode*-II (t_2- t_4): Fig. 6(b), after t_2 I_x star increasing in negative direction and carried by anti-parallel diode D_{sx1} of switch S_{x1}. I_x reaches to its peak value at t_3. Since during this mode negative load current I_L is carried by D_1, negligible voltage will appear across S_1. Hence, it can be turn-on with zero turn on losses. Switch S1 is turn on at t_3. After reaching to its peak value at t_3, I_x starts decreasing and become zero at t_4. At t_4, gating signal to S_{x1} is removed and S_{x1} is switch off with ZCS.

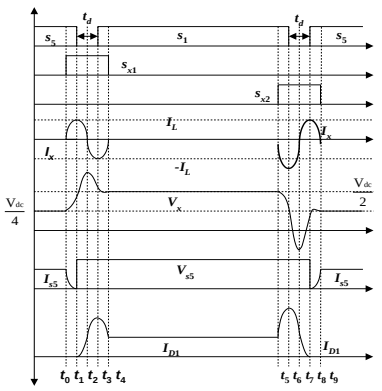


Fig. 5 Idealized waveform of the proposed soft-transition strategy for $I_L < 0$.

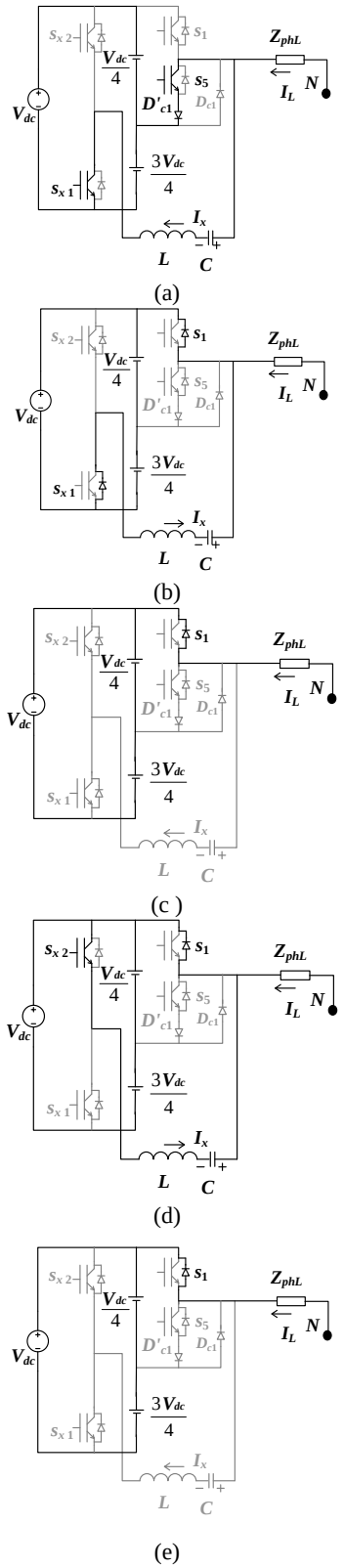


Fig.6. Topological stages of soft switch multilevel inverter during time interval $t_1 – t_9$ for $I_L < 0$.

3. *Mode*-III ($t_4 – t_5$): Fig. 6(c), in this mode normal load current ($I_L < 0$) is carried by D_{c1}.

4. *Mode*-IV ($t_5 – t_7$): Fig. 6(d), at t_5 S_{x2} is turn on. This will again start resonance in auxiliary circuit and I_x increases in negative direction. At this instant D_1 is carrying negative load current I_L and I_x, so effective current through D_1 start increasing. I_x reaches to its peak value which is greater than I_L. After this I_x start decreasing and reaches to zero at t_7. Gating signal to S_1 is removed at t_6.

5. *Mode*-V ($t_7 – t_9$): Fig. 6(e), after t_7 I_x start increasing in positive direction and it is carried by D_{sx2}. Since at this instant D_1 is carrying I_L and I_x both but in opposite direction, effective current through it starts decreasing and at t_8 when I_x reaches to its peak value equal to I_L, current through D_1 become zero. With this S_5 is turn on at t_8 with zero current and zero turn on losses. After t_8, I_x start decreasing and it reaches to zero at t_9. With this gating signal to S_{x2} is removed and its turn off is achieved with ZCS.

Though switch S_1 and S_5 are complimentary to each other; there exits dead time t_d between them at t_2 to t_3 and t_6 to t_8. Similar procedure is applied for other complimentary switch pair i.e. $S_2 – S_6$, $S_3 – S_7$, $S_4 – S_8$. To derive the value of resonant inductor L and capacitor C, equating resonant frequency to $2\pi/t_{on}$, where t_{on} is on-time for auxiliary switches S_{x1} and S_{x2} as shown in Fig. 3 and equating characteristic impedance of resonant tank with equivalent per phase impedance of three phase induction motor. To derive the value of resonant inductor L and capacitor C, equating resonant frequency to $2\pi/t_{on}$, where t_{on} is on-time for auxiliary switches S_{x1} and S_{x2} as shown in Fig. 1and equating characteristic impedance of resonant tank with equivalent per phase impedance of three phase induction motor.

$$\frac{2\pi}{t_{on}} = \frac{1}{\sqrt{LC}} \tag{1}$$

$$Z_o = Z_{phl} = \sqrt{\frac{L}{C}} \tag{2}$$

$$L = \frac{Z_{phl}\ t_{on}}{2\pi} \tag{3}$$

$$C = \frac{t_{on}}{2\pi\ Z_{phl}} \tag{4}$$

Thus the L and C values are determined by these equations.

III. Simulation and Experimental Results

The effectiveness of proposed soft switch multilevel inverter has been tested both by taking simulation and experimental results. All simulation studies were developed using MATLAB. A laboratory model of five level diode clamped three phase multilevel inverter with auxiliary circuit is build. The circuit parameters are tabulated in table 1. Fig.7 (a), (b), (c) illustrates the simulation result of soft-transition for switch S_1 and S_5. Fig. 8 shows the experimental result of soft-transition for switch S_1. Fig. 9 (a) gives soft-transition result for switch S_5, and Fig. 9 (b) shows output voltage and current of inverter. From Fig. 8 and Fig. 9, it is clear that for switch S_1 and S_5 both on and off transition are achieve with soft switching. Since all main switches are equivalently connected in series, to implement soft switching of one switch its effect is reflected in other switch which is on for maximum time. It is clear from Fig. 9, where current through S_5 shows spike which is effect of soft switching of switches S_1-S_5. Load current I_L is free forms such effect

which indicate that Soft-transition operation does not interfere with fundamental operation of motor drive system.

Table 1: Circuit Parameters

SN	Circuit Parameters	Ratings
1	DC Bus Voltage	560 V
2	Resonant Inductor *L*	16 μH
3	Resonant Capacitor *C*	6 *nF*
4	MOSFET	IRF 460
5	Diode	UF 5408
6	Gate Driver IC	UC 3708
7	Opto Coupler	6N 137
8	Load	3ph, 400 V, 3.75 kW, 1460 rpm induction motor.

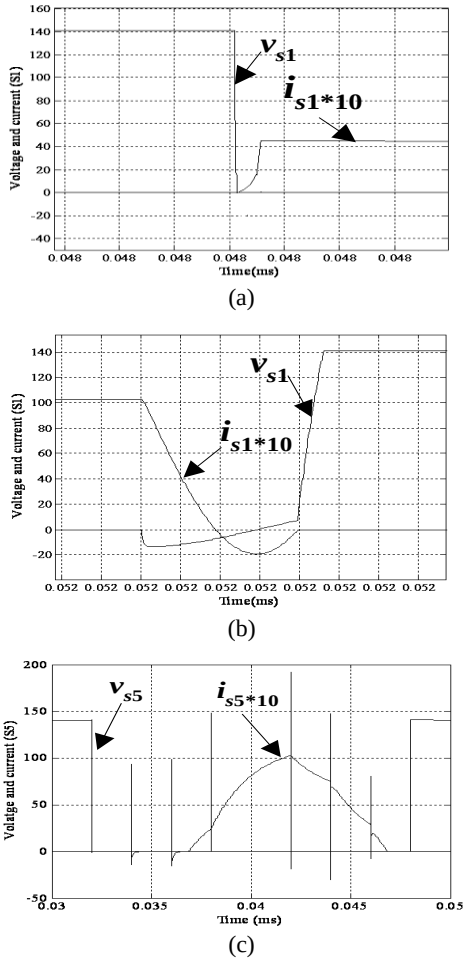
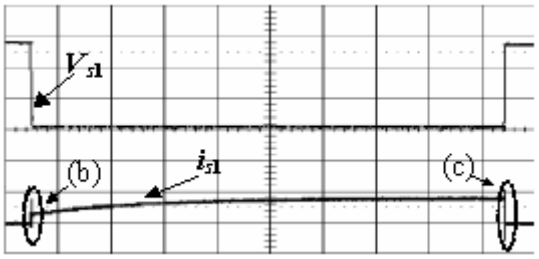


Fig.7. Simulation results (a) Turn-on and (b) turn-off transition of Switch S_1 (c) Voltage and current through S_5.

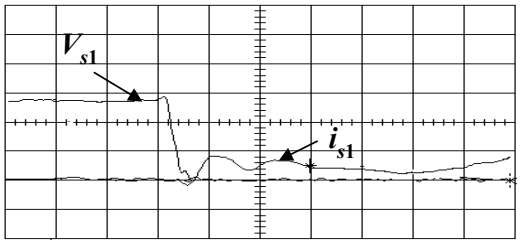
Since auxiliary switches operate alternatively in one switching cycle thermal and current stress are equally distributed over them. So from experimental and simulation result, it can be shown that proposed method achieve soft transition of all switches with reduced number of auxiliary components as compare to other method where relatively more number of components are use which adds reliability and efficiency contingencies.

IV. CONCLUSION

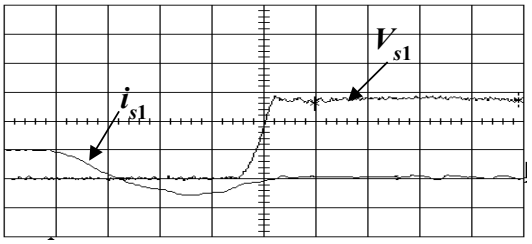
A new soft-switch multilevel inverter is proposed in this paper. The operating waveform and equivalent circuit were presented to explain the operation of the proposed inverter. Simulation and experimental results were presented to verify the validity of proposed control strategy. With this topology, soft switching is achieved for all main switches and auxiliary switches. Compared with existing soft switching inverter, numbers of auxiliary components are reduced.



(a) (Scale: 50V/Div, 10A/Div, 0.5mS/Div)

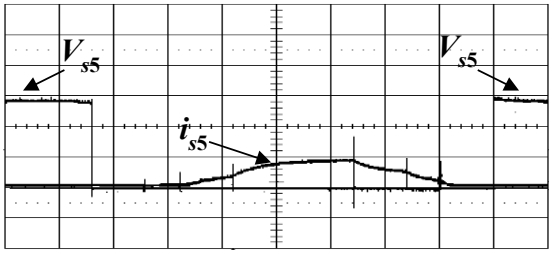


(b) (Scale: 50V/Div, 10A/Div, 0.2μS/Div)

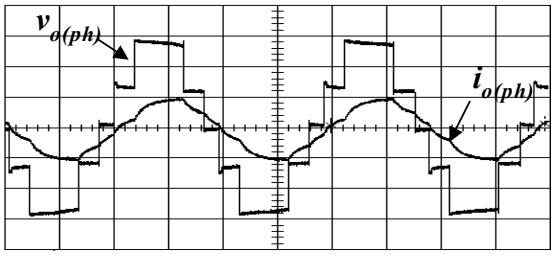


(c) (Scale: 50V/Div, 10A/Div, 0.5μS/Div)

Fig. 8 Experimental result of (a) Voltage across and current through S_1 (b) Turn-on transition of S_1 and (c) Turn-off transition of S_1



(a) (Scale : 50V/Div, 10A/Div, 2*m*S/Div)



(b) (Scale : 100V/Div, 10A/Div, 5*m*S/Div)

Fig.9. Experimental result (a) Voltage across and current through S_5 (b) Output phase voltage and current.

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