Novel Single-Phase Multilevel Inverter Topology Based on Cascaded Connection of Basic Units

R. Shalchi Alishah [1] D. Nazarpour [2] S. H. Hosseini [3] M. Sabahi [4]

Abstract–Recently, several numbers of multilevel inverter topologies have been presented that the numbers of power electronic devices have been reduced. This paper presents a novel single-phase topology for multilevel inverter. The proposed topology is based on cascaded connection of basic units. This topology uses minimum lumber of power electronic components such as IGBT, gate driver circuit and antiparallel diode. For proposed topology, two methods are presented for determination of dc voltage sources values. The propose topology is used in medium and high-voltage applications. The proposed topology is compared with other topologies which recently have been proposed. MATLAB/SIMULINK software is used for simulation.

Keywords–Multilevel inverter, classical topologies, modulation control, total harmonic distortion.

I. INTRODUCTION

Compared to two level inverter, Multilevel inverters can generate output voltage waveform with fewer total harmonic distortions (THD) and the value of voltage stress on power electronic devices is low [1, 2]. Multilevel inverters are used in more applications such as renewable energy sources, Electric/Hybrid electric vehicles, FACTS devices and so on [3-5]. There are three types of classical multilevel inverter topologies which have been named as follows:

- Diode Clamped Multilevel Inverter [6].
- Flying capacitors Multilevel Inverter [7].
- Cascade Multilevel Inverter [8].

The most important part of multilevel inverter is switches. Because increasing the number of switches is caused that the costs and circuit size increase and the control of switches will be a big problem [9, 10]. Cascade Multilevel Inverter utilizes the least number of power electronic components in comparison with diode clamped and flying capacitor inverters.

Cascade converter is divided into two configurations which are named symmetric and asymmetric configurations. The symmetric configuration uses the dc voltage sources of the same magnitude. In the asymmetric configuration, the values of the dc sources are non-equal. Asymmetric configuration can generate more number of output voltage levels in comparison with asymmetric configuration [11, 12]. The symmetric configuration has the advantage of modularity that makes them simple to design and extend. But, the number of power electronic switches increases.

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However, the asymmetric configuration has more complex design and providing the dc sources of various magnitudes can be a big difficulty. On the other words, the number of output voltage levels increases leading to reduction in the number of required power electronic elements.

Therefore, to reduce the number of power electronic devices a new topology for multilevel inverter has been presented in [13]. But, this topology needs more number of bidirectional switches.

In [14], a novel topology for multilevel inverter has been presented. Compared to proposed topology in [13], this topology needs less number of switches. But, this topology uses only one full-bridge converter and the switches of full-bridge converter require withstanding more voltage levels and it is restriction in high-voltage applications.

Several modulation technique have been improved for multilevel inverters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), fundamental frequency switching and so on [15]-[19]. This paper focuses on fundamental frequency switching strategy for trigger the power electronic switches for controlling and generating output voltage levels.

This paper presents a new topology for multilevel inverter which needs minimum number of power electronic elements.

II. PROPOSED TOPOLOGY

Fig. 1 shows the basic unit structure for proposed multilevel inverter. This structure consists of four unidirectional switches (T_1, T_2, T_3, T_4) and one bidirectional switch (S). The unidirectional switches include an antiparallel diode and an IGBT. For bidirectional switches several structures are used. In this structure, the common emitter structure is used which consists of two antiparallel and two IGBTs. This structure of bidirectional switch needs only one gate driver circuit. The dc voltage sources values are the same.

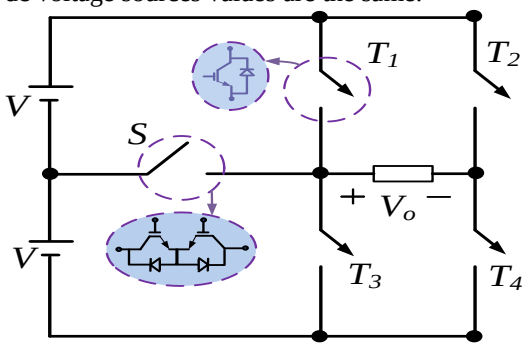


Fig. 1: Basic unit structure for proposed multilevel inverter.

This basic unit can generate five levels at the output voltage $(0,V,-V,2V,-2V)$ .Table I shows the switching states of proposed basic unit for generation five levels at the output voltage waveform.

Table 1: Switching States of Proposed Basic Unit

State	Switches					Output voltage
	S	T_1	T_2	T_3	T_4	
1	0	1	1	0	0	0
2	1	0	0	0	1	V
3	1	0	1	0	0	-V
4	0	1	0	0	1	2V
5	0	0	1	1	0	-2V

To generate an output voltage waveform with high quality and lower value of harmonic distortions, the number of output voltage waveform must be increased. Therefore, a cascade topology based on series connection of basic units is proposed. Fig. 2 shows the proposed cascade multilevel inverter. The output voltage of the proposed cascade inverter is obtained by:

$$V_o = V_{o1} + V_{o2} + \cdots + V_{on} \tag{1}$$

The number of IGBTs in proposed cascade topology is given by the following relationship:

$$N_{IGBTs} = 6n \tag{2}$$

In this topology, the bidirectional switches uses only one gate driver. Therefore, the number of gate driver circuits is given by:

$$N_{driver} = 5n \tag{3}$$

In this equations, N_{IGBT} and N_{driver} represent the number of required IGBTs and gate driver circuits. In this topology, the dc voltage sources values of each basic unit are the same. For proposed cascade converter two methods are presented to generate all levels (odd and even) in the output voltage.

A. First Method

In this method, the values of dc sources are the same. In the other words, we have

$$V_1 = V_2 = \cdots = V_n \tag{4}$$

Because the values of dc sources are the same, this topology is named symmetric topology. For this method, the number of output voltage levels is calculated by the following equation:

$$N_{level} = 4n + 1 \tag{5}$$

where n represents the number of basic units in the proposed cascade structure. From (2) and (5), we have

$$N_{level} = \frac{2}{3} N_{IGBT} + 1 \tag{6}$$

Considering (3) and (5), the relation between the number of output voltage levels and gate drivers will be:

$$N_{level} = \frac{4}{5} N_{deriver} + 1 \tag{7}$$

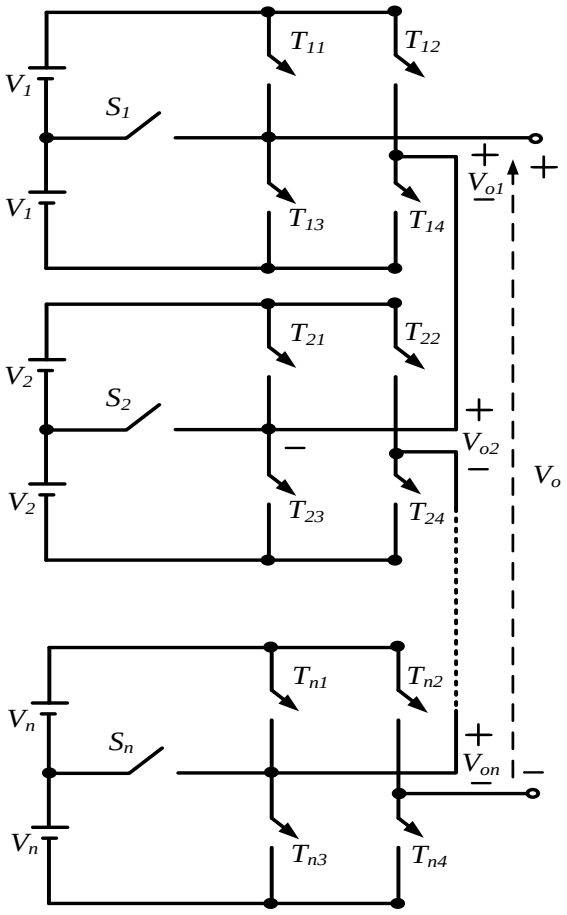


Fig. 2: Proposed cascade multilevel inverter structure.

B. Second Method

In this method, the magnitudes of dc voltage sources are obtained by:

$$V_1 = V \tag{8}$$

$$V_m = 5^{m-1} V \qquad m = 2,3,\cdots n \tag{9}$$

Using this method, the number of output voltage levels is calculated by:

$$N_{level} = 5^n \tag{10}$$

Using (2) and (10), the relation between the number of output voltage levels and IGBTs will be:

$$N_{level} = 5^{\frac{N_{IGBT}}{6}} \tag{11}$$

Considering (3) and (5), we have

$$N_{level} = 5^{\frac{N_{driver}}{5}} \tag{12}$$

In this method, the magnitudes of dc sources are non-equal. Hence, this method is named asymmetric configuration. It is noticeable that Instead of dc voltage sources, we can use capacitors, fuel cells and so on.

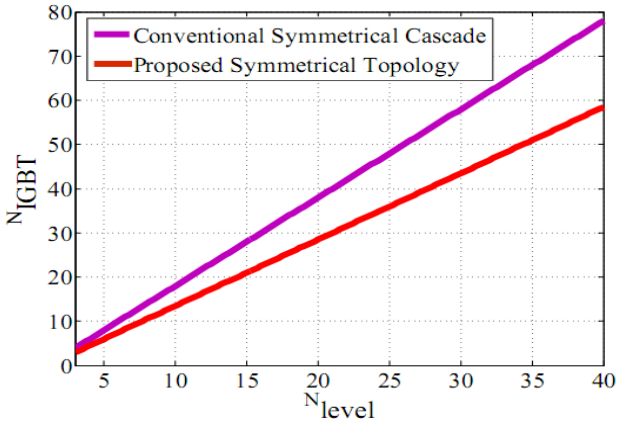
III. Comparison of Proposed Topology with Other Topologies

In this section, the proposed topology is compared with other topologies in terms of IGBTs, antiparallel diodes, gate drivers and the maximum voltage stress on switches.

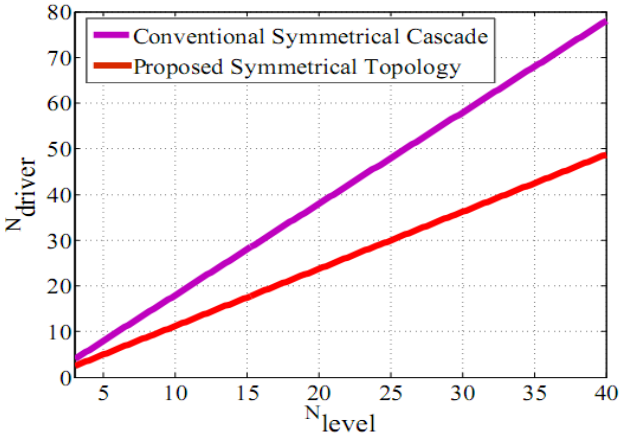
A. Comparison between proposed symmetric topology

(first method) and classical symmetric cascade topology. Fig. 3(a) and (b) compare the number of IGBTs and gate drivers versus the number of output voltage levels for proposed symmetric topology (first method) and classical symmetric cascade topology, respectively. This figures show that proposed symmetric topology needs less number of IGBTs and gate drivers.

It is noticeable that in the recommended structure and proposed topologies in [13] and [14], the number of antiparallel diodes and IGBTs are equal. Hence, recommended structure needs fewer numbers of anti-parallel diodes in comparison with other topologies.



(a)

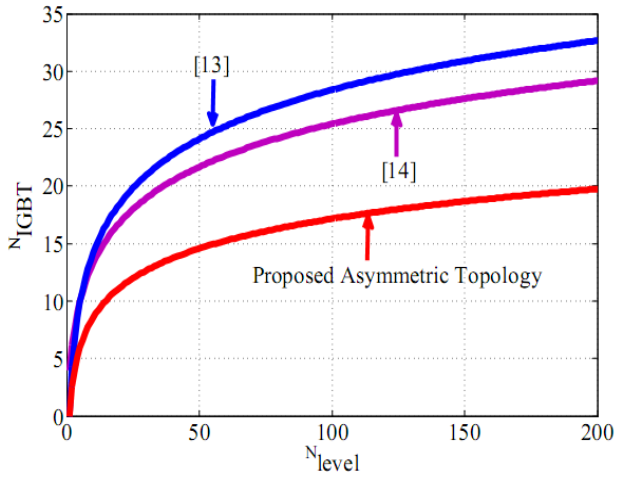


(b)

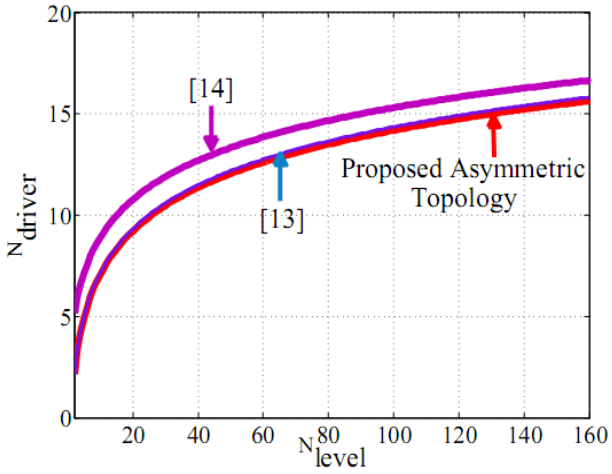
Fig. 3: Comparison between proposed symmetric topology (first method) and classical symmetric cascade topology in terms of (a) The number of IGBTs; (b) The number of gate drivers.

B. Comparison between proposed asymmetric topology (second method) and proposed topologies in [13] and [14]. It is important to note that in the presented topologies in [13] and [14] have been utilized bidirectional switches that are composed of two IGBTs and this bidirectional switch needs only one gate driver circuits. Fig. 4(a) and (b) compare the number of IGBTs and drivers versus the number of output voltage levels for proposed asymmetric topology (asymmetric method) and proposed topologies in [13] and [14].

It is obvious that the second method of proposed topology requires fewer numbers of IGBTs and drivers in comparison with proposed topologies in [13] and [14]. It results in the reduction of cost, losses, circuit size and simple control strategy. The gate driver circuits are the electronic part of the circuit and increasing the number of gate driver circuits is a considerable. Because increasing of the number of gate drivers cause increasing costs and control complexity.



(a)



(b)

Fig. 4: Comparison between proposed asymmetric topology and proposed topologies in [13] and [14] in terms of (a) The number of IGBTs; (b) The number of gate drivers.

It is noticeable that the proposed structure utilizes multiple cascaded full-bridges in the output side of the converter, while the presented structure in [14] utilizes one full-bridge in the output side and this full-bridge converter have to withstand a voltage equal to sum of all of dc sources. This leads to restriction on the high-voltage applications. However, the proposed cascade switched-diode converter can be used in high voltage applications.

For proposed cascade topology, with assumption that the value of voltages in the *jth* basic unit is equal to V_j, the maximum voltage stress of bidirectional and unidirectional switches will be V_j and $2V_j$, respectively. But, the maximum voltage stress of switches in the proposed topologies in [13] and [14] is high and it is an important advantage.

IV. Fundamental Frequency-Switching Strategy

To control of the switches of the proposed multilevel inverter topology, the fundamental frequency-switching strategy is utilized. Because the fundamental frequency-switching strategy has its low switching frequency in comparison with other strategies and it is an advantage [13, 20]. For power converters, the total harmonic distortion (THD) is a popular performance index, which evaluates the quantity of harmonic contents in the output waveform. For sinusoidal waveform, the THD is defined as follows:

$$THD = \frac{\sqrt{\sum_{n=3,5,7,\ldots}^{\infty} V_{o,n}}}{V_{o,1}} = \sqrt{\left(\frac{V_{o,rms}}{V_{o,1}}\right)^2 - 1} \quad (13)$$

In this equation, n represents the order of the corresponding harmonic, while the sub-index 1 corresponds to the fundamental frequency. Therefore, V_{o_n} and V_{o_1} are the rms of the n order harmonic and fundamental of the output voltage waveform, respectively. Also, $V_{o_{rms}}$ represents the rms magnitudes of the output voltage. In above equation, the magnitude of V_{o_1} and $V_{o_{rms}}$ can be calculated using the following equations, respectively:

$$V_{o,1} = \frac{2\sqrt{2}V}{\pi} \times \sum_{j=1}^{N_{level}} \cos\left(\theta_j\right) \quad (14)$$

$$V_{o,rms} = \frac{2\sqrt{2}V}{\pi} \times \sqrt{\sum_{n=1,3,5,\ldots}^{\infty} \left(\sum_{j=1}^{N_{level}} \frac{\cos\left(n\theta_j\right)}{n}\right)^2} \quad (15)$$

In this equation, N_{level} is the number of levels and the values of $\theta_1, \theta_2, \theta_3, \ldots, \theta_{N_{level}}$ represent switching angles and is calculated by:

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{level}}\right) \quad j = 1, 2, 3, \ldots, N_{level} \quad (16)$$

In this equation, N_{level} represents the number of generated levels at the output voltage waveform. Using (13-16), it is obvious that the magnitude of THD depends on the number of levels and switching angles. It is clear that increasing the number of levels leads to the multilevel inverter produces near-sinusoidal output voltage waveform and as a result, very low harmonic distortion. The objective of this paper is not the calculation of the optimal switching angles in order to the elimination of selected harmonics and reducing the total harmonic distortion (THD).

V. Simulation Results

In order to validate the proposed multilevel inverter, MATLAB-Simulink software has been utilized. The simulation studies are carried out for a structure that the first and second methods of determination of dc voltage sources are applied. Fig. 5 shows the proposed cascade structure, which consists of two basic units. The selected parameters for testing are:

(a) An *R-L* load with L =50mH and R=100 Ω

(b) Load frequency=50Hz.

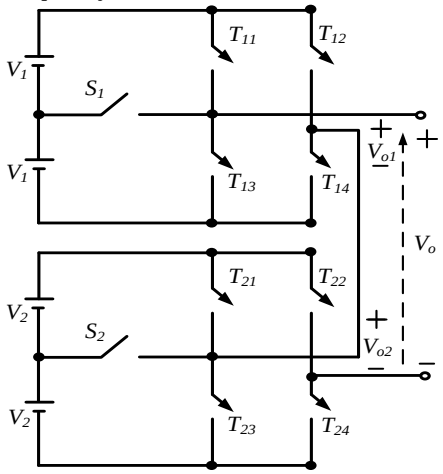


Fig. 5: Proposed cascade structure.

A. Simulation results based on the first method:

In this method, the values of dc voltage sources are equal and have been considered 60 volts ($V_1 = V_2 = 60V$) . Therefore, using this method, this structure can generate nine levels at the output voltage waveform.

The output voltage and current waveforms and their corresponding Fourier spectrums are shown in Fig. 6 and 7, respectively. THD of the output voltage and current based on simulations are 8.14% and 3.26%.

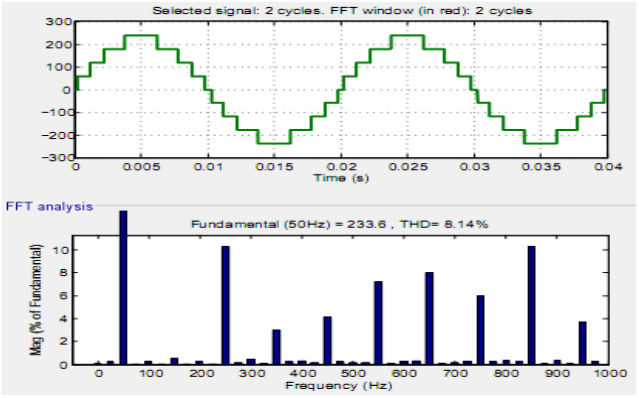


Fig. 6: Output voltage and harmonic spectrum of 9-level inverter (THD=8.14%).

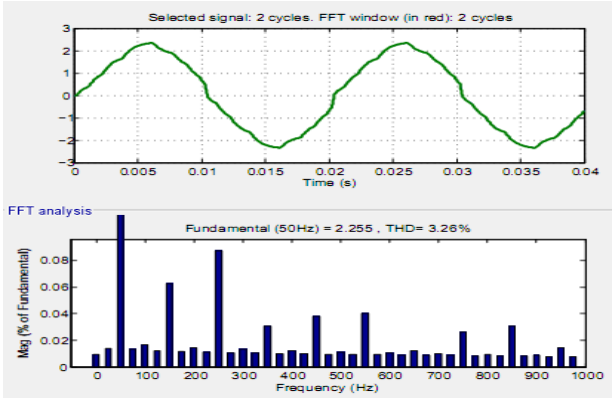
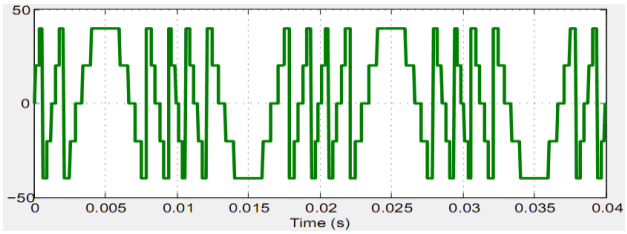


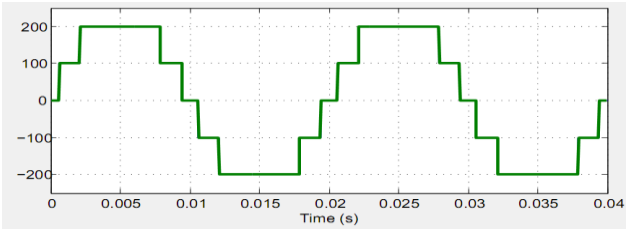
Fig. 7: Output current and harmonic spectrum of 9-level inverter (THD=3.26%).

B. Simulation results based on the second method:

In this method, the dc voltage sources values are selected ($V_1 = 20V$) and ($V_2 = 100V$) . Therefore, using this method, this structure can generate 25 levels at the output voltage waveform. Fig. 8(a) and (b) show the output voltage of (V_{o1}) and (V_{o2}) . Fig. 8 (c) and (d) show output voltage and currents waveforms. THDs of the output voltage and current based on simulations are 2.44% and 0.43%, respectively.



(a)



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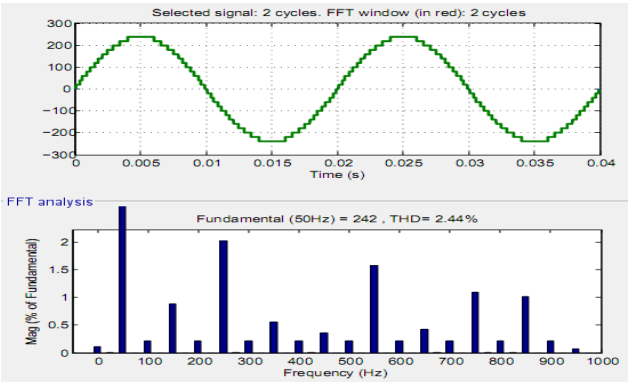

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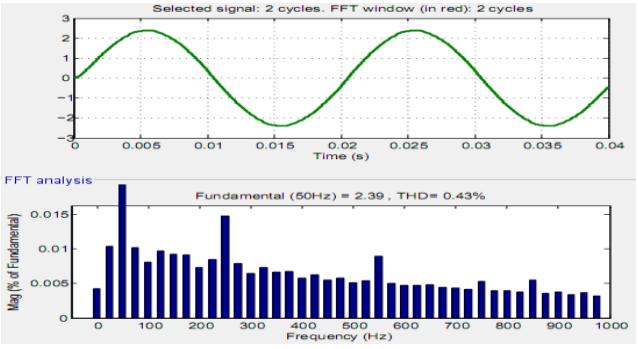

(d)

Fig. 8: Simulation results for 25-level cascade inverter. (a) Output voltage of the first stage (V_{o1}) ; (b) Output voltage of the second stage (V_{o2}) ; (c) Output voltage and harmonic spectrum (THD=2.44%); (d) Output current and harmonic spectrum (THD=0.43%).

The comparison of THDs of output voltage and current in the two simulated methods show that increasing the number of levels leads to the multilevel inverter produces output voltage waveform with very low THD. For increasing high power quality and desired output voltage waveform, other switching strategy should be applied to the converter or the number of voltage levels should be increased. Based on this figure and the value of THD for current, it is clear that the load current is almost sinusoidal. Because, the R-L load of the converter (R-L) behaves as a low-pass filter for the current.

VI. Conclusion

In this paper, a new structure for multilevel inverter with reduced number of IGBTs and gate drivers, antiparallel diodes was presented. Less number of the IGBTs and drivers leads to the reduction of size, simple control strategy and high efficiency. Two methods for determination of dc voltage source values were suggested. This technique provides more voltage levels without increasing number of power electronic components. Comparison among the proposed converter with other similar topologies has been provided. It is shown that the proposed topologies, has many levels with fewer components. Fundamental frequency-switching method was applied to the new topology to trigger the power switches for controlling the voltage levels generated on the output.

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BIOGRAPHIES

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