Novel Scalar PWM algorithm for Four-Level Asymmetrical Dual Inverter Fed Induction Motor Drive

M. Harsha vardhan Reddy[1],T. Brahmananda Reddy[2],B. Ravindranath Reddy[3],M. Suryakalavati[4]

Abstract–This paper presents a novel scalar based pulse width modulation (PWM) algorithm for four-level asymmetrical dual inverter fed induction motor drive. In the conventional carrier based PWM algorithms for dual inverter fed induction motor drive, both inverters will be operated at all modulation indices. But, the proposed PWM algorithm operates only one inverter at lower modulation indices and other inverter will be clamped to the dc bus. Hence, the proposed PWM algorithm results in reduced switching losses at lower modulation indices. At modulation index between the range 0.33 to 0.66, the proposed algorithm will operate both inverters such that the common mode voltage will be reduced. At higher modulation indices (>0.666), the proposed algorithm results in same common mode voltage when compared with the conventional algorithm. To validate the proposed algorithm, the numerical simulation studies have been carried out and results are presented and compared.

Keywords–Dual inverter, induction motor, SVPWM

I. INTRODUCTION

The voltage source inverter (VSI) plays a key role in variable speed drive applications. In order to achieve the controllable voltage and frequency from the VSI, the pulse width modulation (PWM) algorithms are becoming popular in recent years. The comparison of various PWM algorithms is discussed in detailed in [1]. Among the various possible PWM algorithms, the space vector PWM (SVPWM) is popular due to high dc bus utilization and reduced harmonic distortion when compared with sinusoidal PWM (SPWM) technique. Conventional SVPWM algorithm constructs the reference voltage vector by using the active and zero states in an average manner [2]. The dwell times can be calculated by using (1)-(3).

$$T_1 = \frac{2\sqrt{3}}{\pi} M_i \sin\left(60^0 - \alpha\right) T_s \quad (1)$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M_i \sin(\alpha) T_s \quad (2)$$

$$T_z = T_s - T_1 - T_2 \quad (3)$$

For the real time implementation of SVPWM algorithm, there are two well-known approaches namely, triangular comparison and space vector approaches. The correlation between these two approaches has discussed in detailed in [3]. The carrier comparison approach is simple for the real time implementation and hence became popular in various applications. As the calculation of dwell times requires angle information and reference magnitude information, the complexity involved is more. To reduce the complexity, a simplified approach has been proposed in [4-5] by using the concept of effective time. The switching times are calculated by using the imaginary switching times, which are proportional to the instantaneous phase voltages.

The harmonic distortion and common mode voltage is more in two-level inverters. The harmonic distortion can be reduced by increasing switching frequency. But, the increment in switching frequency will increase the switching losses of the inverter. In order to achieve the reduced harmonic distortion at low switching frequency and to reduce common mode voltage, the multilevel inverters are presented in [6-8]. The harmonic distortion can be reduced by increasing the number of levels, which increases the complexity also. Moreover, the diode clamped inverter requires clamping diodes and also exhibits the neutral point oscillations. In order to nullify the neutral point oscillations, the H-bridge inverters became popular. But, H-bridge topologies require more number of dc sources.

To overcome the drawbacks of diode clamped and H-bridge multilevel inverters, dual inverter fed open-end winding induction motor drive is presented in [9-11]. The dual inverter configuration can also be extended to higher levels [11] by using unequal source voltages on both sides of the drive as shown in Fig. 1.

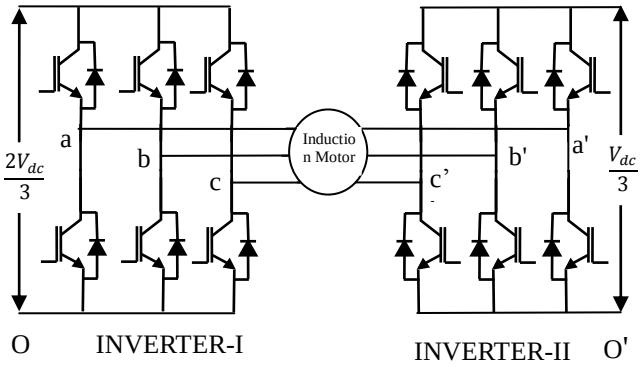


Fig.1: Dual inverter circuit configuration with unbalanced source voltages

The PWM algorithm, which is presented in [11-13] for open end winding induction motor drive results in higher switching losses, large common mode voltage variations and increased harmonic distortion at lower modulation indices.

The paper first received 29Dec2013 and in revised form 10 May 2014.
Digital Ref:APEJ-2013-10-0429

[1,2]Department of Electrical and Electronics Engineering, G. Pulla Reddy Engineering College (Autonomous),Kurnool, Andhra Pradesh, India.
E-mail: maramreddyharsha@gmail.com, tbnr@rediffmail.com
[3,4]Department of Electrical and Electronics Engineering, JNTUH, Kukatpally, Hyderabad, Andhra Pradesh, India.

time implementation and hence became

This paper presents a simplified SVPWM algorithm for open-end winding induction motor drive. The proposed carrier based PWM algorithm results in reduced common mode voltage, switching losses and harmonic distortion at lower modulation indices. Between the modulation index ranges 0.3 to 0.6, the proposed algorithm gives reduced common mode voltage variations with slightly increased harmonic distortion.

II. SIMPLIFIED SVPWM ALGORITHM

The proposed SVPWM algorithm calculates the dwell times by using the instantaneous phase voltages only. Assume a set of three-phase balanced ac voltages as given in (4)

$$\begin{aligned} V_a &= V_m \cos(\omega t) \\ V_b &= V_m \cos(\omega t - 120) \\ V_c &= V_m \cos(\omega t - 240) \end{aligned} \quad (4)$$

Then, a unique zero sequence signal is calculated as

$$V_{zs} = \frac{V_{dc}}{2}(2a_0 - 1) - a_0 V_{\max} + (a_0 - 1)V_{\min} \quad (5)$$

$$V_{ref}^{*} = V_{ref} + V_{zs} \quad (6)$$

The modulating waves of SVPWM algorithm can be generated by adding this zero sequence signal to the instantaneous phase voltages, which are given in (6). By varying the constant a_0 between zero to one various PWM algorithms can be generated. In order to achieve modulating signal similar to the conventional SVPWM algorithm this constant is taken as 0.5.

III. CONTROLSTRATEGIES FOR PROPOSED INVERTER

The dual inverter fed induction motor with unequal source voltages is shown in Fig.1., where V_{dc} represents the DC input voltage,$V_{ao,}V_{bo,}V_{co}$are the corresponding pole voltages of inverter-I and $V_{a'o'},V_{b'o'},V_{c'o'}$are the corresponding pole voltages of inverter-II.$V_{aa'},V_{bb'},V_{cc'}$ are the effective pole voltages which can be calculated as given in (7). $V_{ab,}V_{bc,}V_{ca}$are the line voltages.$V_{oo'}$is the common mode voltage given by (8)

$$\begin{aligned} V_{aa'} &= V_{ao} - V_{a'o'} \\ V_{bb'} &= V_{bo} - V_{b'o'} \\ V_{cc'} &= V_{co} - V_{c'o'} \end{aligned} \quad (7)$$

$$Voo' = \frac{V_{ao} - V_{a'o'} + V_{bo} - V_{b'o'} + V_{co} - V_{c'o'}}{3} \quad (8)$$

In this paper, for the implementation of SVPWM algorithm, the carrier comparison approach has been considered. The multi-level carrier comparison approach requires *N-1*level shifting triangles to generate *N-l*evel output voltage. The proposed inverter configuration [12] is capable of generating four-level output voltage and hence, the carrier comparison approach requires three level shifting triangles. The magnitude of level shifting triangular signal is given in (9)

$$V_c = \frac{1}{N-1} \quad (9)$$

As *N*=4, the three level shifting triangular signals is having a magnitude of 1/3. These three level shifting triangles are shown in Fig. 2 dividing the modulating plane in to three different regions (R_1–R_3). Based on value of modulation index, the operation of inverters will be decided. If the modulating signal is not present any of three regions, mean that both inverters are not in operation and output voltage obtained is zero. This condition is only possible when modulation index is zero. For modulation index greater than zero modulating signals are present in any of the three regions.

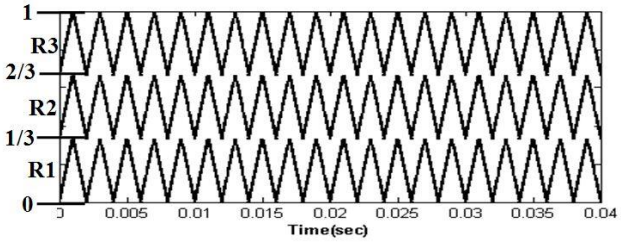


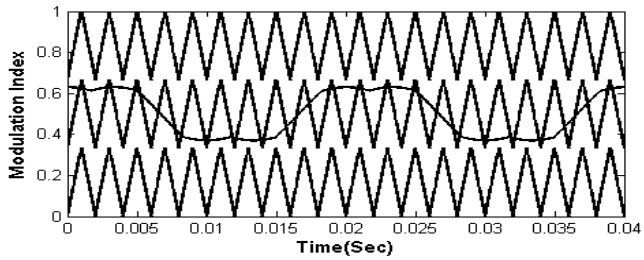
Fig. 2:Different regions in carrier based modulation approach

For the generation of pulses for the proposed inverter topology two possible approaches are considered in this paper. One is the conventional approach and other one is the proposed approaches. The comparison of triangular and modulating signals for these two approaches is as shown in Fig. 3 and Fig.4. From Fig.3(a) and Fig. 4(a), it can be observed that during the lower modulation indices (from 0 to 0.3), the modulating wave falls in the region R2 in the conventional approach where as it falls in R1 in the proposed approach. Hence, in the conventional approach, both inverters will operate. But, in the proposed approach only inverter-II will operate and inverter-1 will be clamped to the dc bus. Hence, the proposed approach will give reduced switching losses. Moreover, in the proposed approach, the inverter-II produces an output voltage of 0 and $V_{dc}/3$ which results in two-level output voltage.

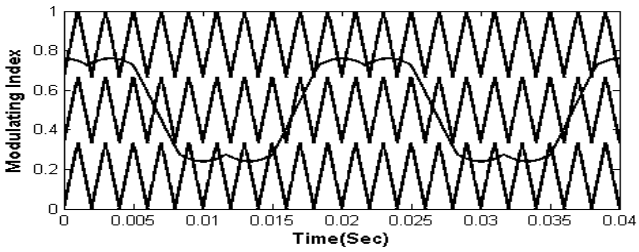
During the medium values of modulation indices (from 0.3 to 0.6), in the conventional approach the modulating wave falls in all three regions whereas in the proposed approach it will be in R1 and R2 regions.

Due to this reason the effective or combined pole voltage of dual inverter configuration with conventional approach is four-level and with proposed approach is three-level. In the proposed approach, two inverters will operate and generates three level output voltage of ($0,V_{dc}/3, 2V_{dc}/3$). Even though the effective pole voltages are different, these two approaches generate same output phase and line voltages. But, with the proposed approach, the common mode voltage variations are reduced as the effective pole is low when compared with conventional approach. In the proposed approach, at higher modulation indices (greater than 0.6), the operation of the inverters with conventional

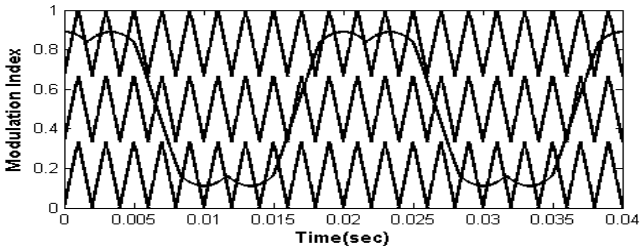
and proposed approaches will show the same effect on load. In the proposed approach, the modulating signal is present in all the three regions as shown in Fig. 4 both inverters are in operation and the inverters will be operated such that these generate four level output voltage of $0, V_{dc}/3, 2V_{dc}/3, V_{dc}$.



(a)

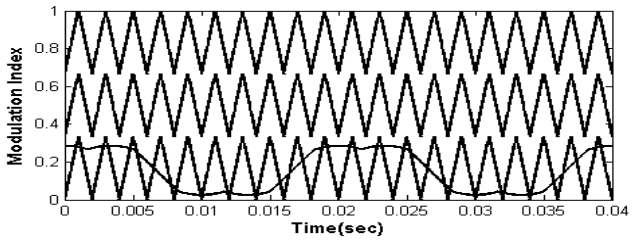


(b)

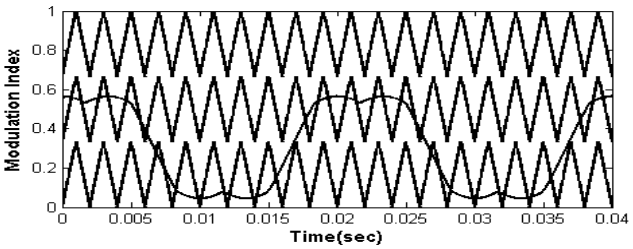


(c)

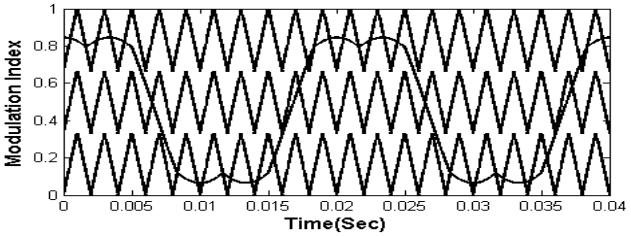
Fig. 3 conventional carrier based approach (a) at low modulation indices (b) at medium modulation indices (c) at high modulation indices



(a)



(b)



(c)

Fig. 4: Proposed carrier based approach (a) at low modulation indices (b) at medium modulation indices (c) at high modulation indices

IV. Simulation results and discussion

To evaluate the proposed scalar based (carrier comparison based) control strategy, numerical simulation studies have been carried out by using the MATLAB. For the simulation studies the induction motor parameters given in Table 1.

Table 1: Induction motor parameters

Rated speed	1440 *RPM*		
frequency	50*Hz*	Rotor resistance	1.21Ω
Stator resistance	1.57Ω	Mutual inductance	170*mH*
Stator inductance	183*mH*	Rotor inductance	183*mH*

Dc link voltage is taken as 540 *V* and switching frequency is taken as 3*kHz*. The simulation results for two approaches during no load and loaded (30*N*-*m*)conditions are shown in Fig. 5-Fig. 12 at different modulation indices.

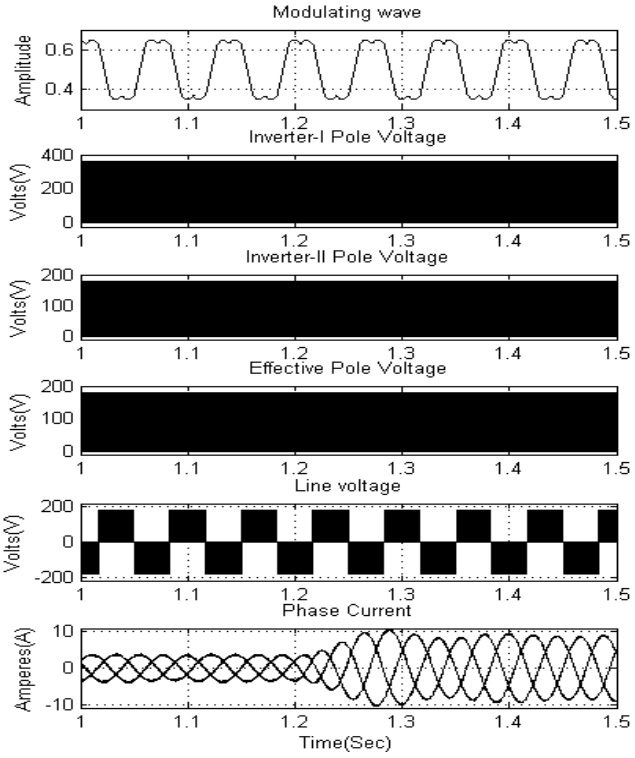


Fig. 5: Simulation results for conventional approach at M=0.27

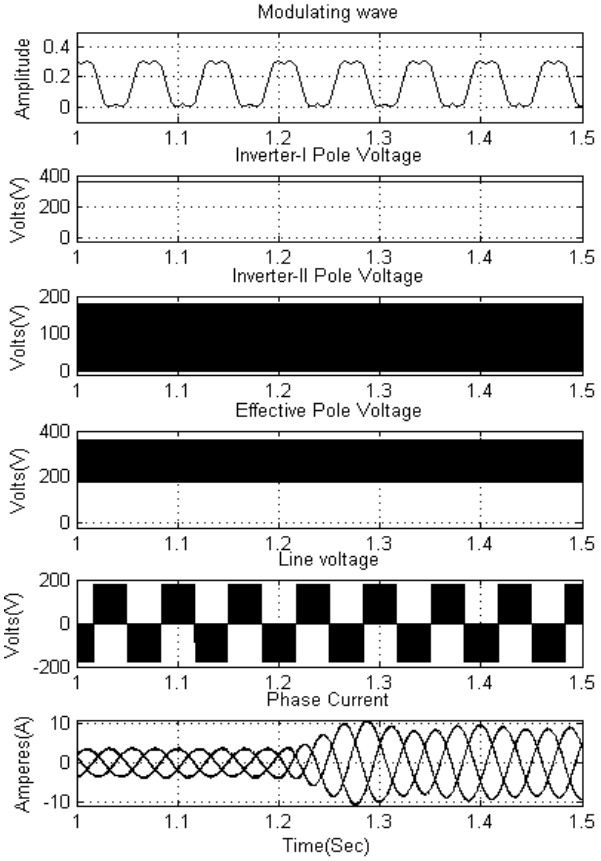


Fig. 6: Simulation results for proposed approach at M=0.27

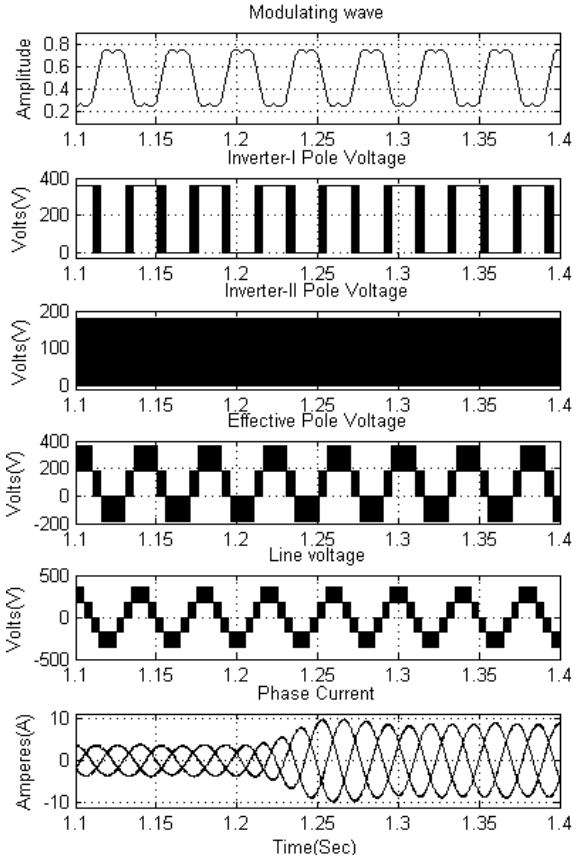


Fig. 7: Simulation results for conventional approach at M=0.45

From Fig.5 and Fig.6, it can be observed that as one of the inverters is being clamped in the proposed approach, it results in reduced switching losses.

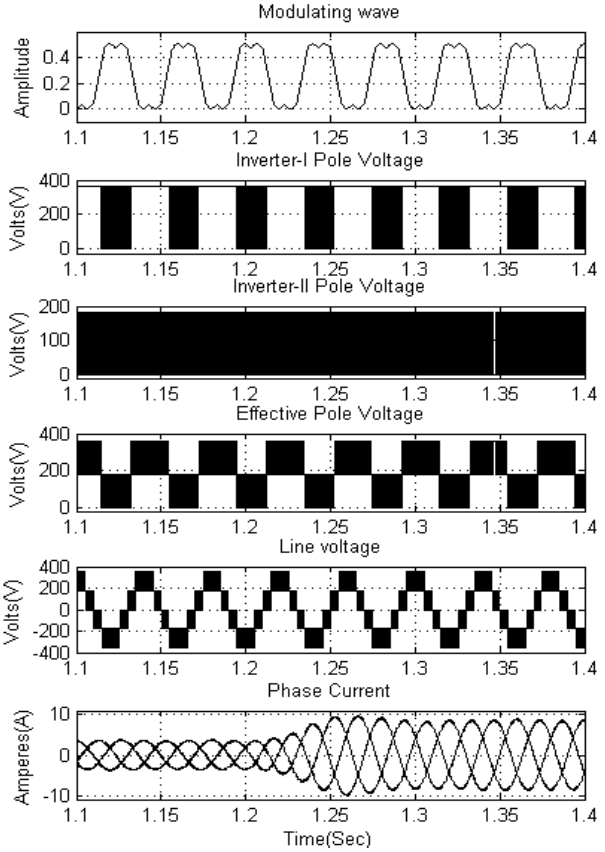


Fig. 8: Simulation results for proposed approach at M=0.45

From Fig. 7 and Fig. 8, it can be observed that the effective pole voltage in the conventional approach has four levels of voltage and whereas in the proposed approach has three levels of voltage. Conventional approach has high effective pole voltage when compared with proposed approach. Hence, the proposed approach results in reduced common mode voltage. The common mode voltage variations of two approaches are as shown in Fig. 9 and Fig. 10. From Fig. 9, it can be observed that the conventional approach will give the common mode voltage variations between -60*V* and 240*V*. Whereas, the proposed approach will give the common mode voltage variations between 60*V* and 300*V* as shown in Fig. 10.

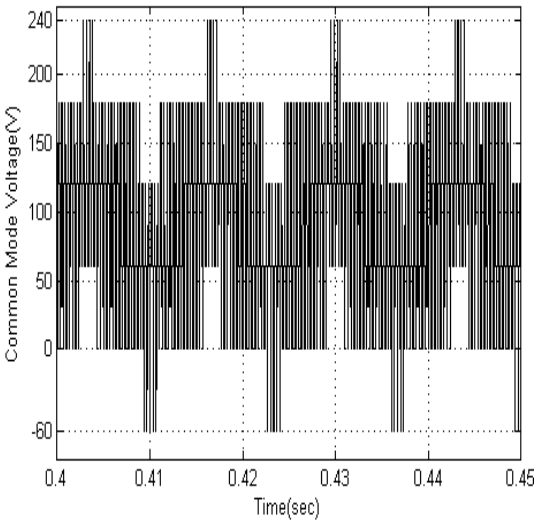


Fig. 9: Common mode voltage plot at modulation index M=0.45 with the conventional approach.

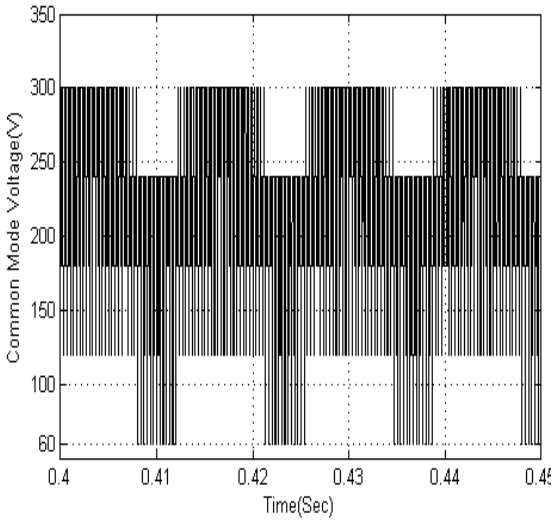


Fig. 10:Common mode voltage plot at modulation index M=0.45 with the proposedapproach.

The simulation results at higher modulation indices are shown in Fig. 11 and Fig. 12. During the higher modulation indices these two approaches will give similar results.

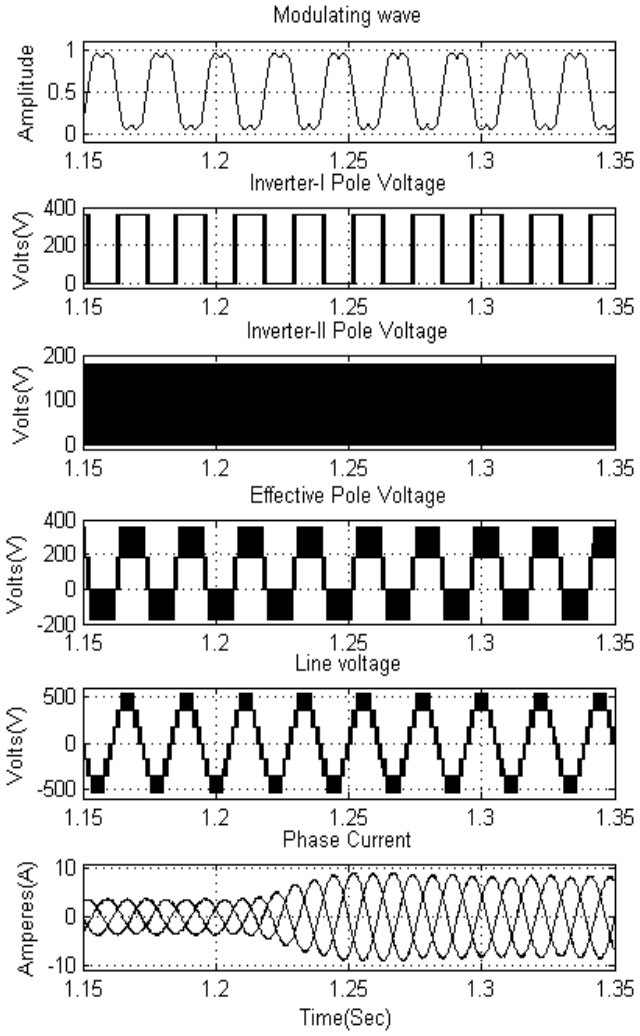


Fig. 11: Simulation results for conventional approach at M=0.815

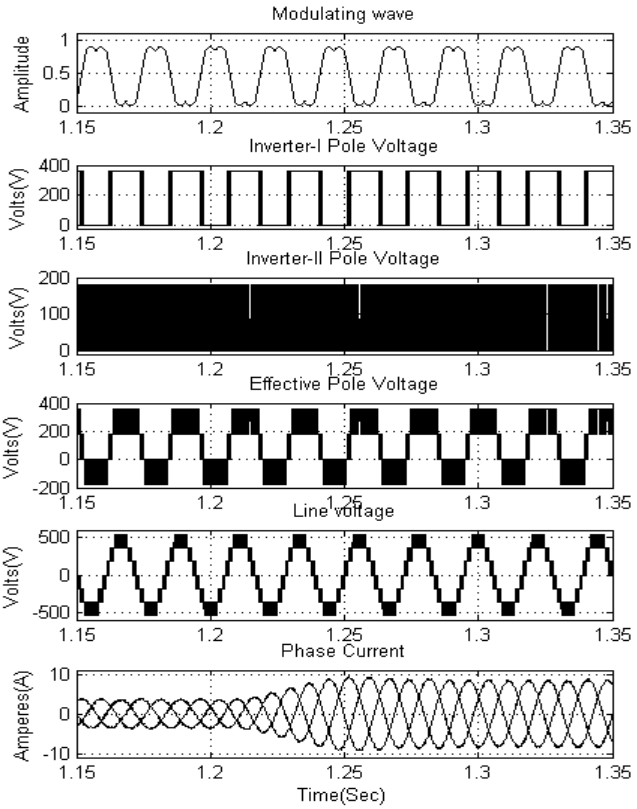


Fig. 12: Simulation results for proposed approach at M=0.815

The harmonic spectra of line currents at different modulation indices are as shown in Fig. 13 and Fig. 14.

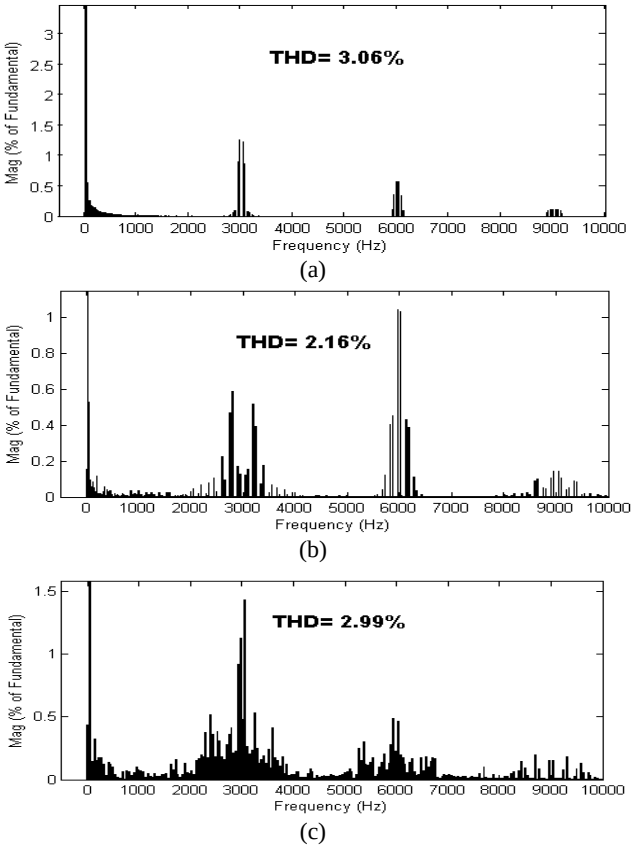


Fig.13: Harmonic spectra of line current at various modulation indices with the conventional approach (a) M=0.27 (b) M=0.45 (c) M=0.815

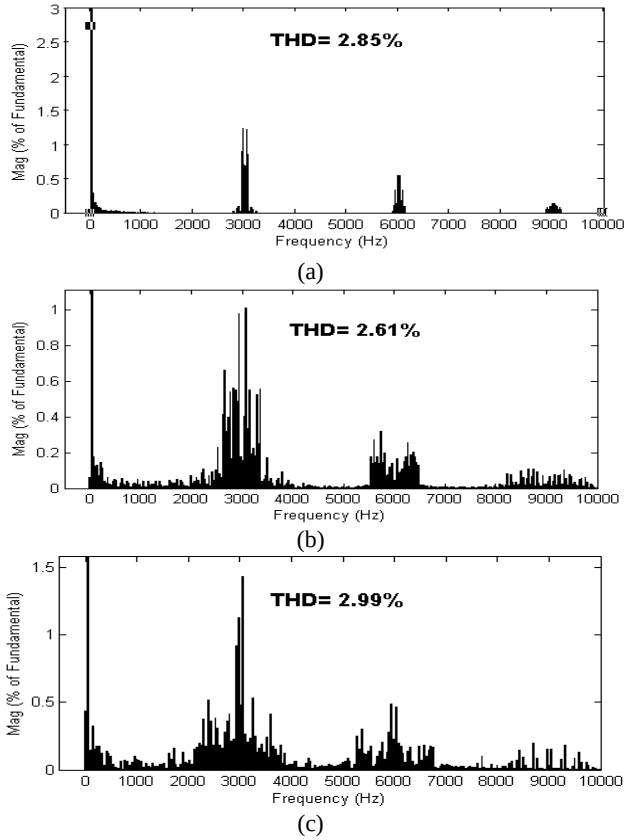


Fig.14: Harmonic spectra of line current at various modulation indices with the proposed approach (a) M=0.27 (b) M=0.45 (c) M=0.815

From Fig. 13 (a) and Fig. 14 (a), it can be observed that the proposed approach results in reduced harmonic distortion when compared with the conventional approach. Moreover, it can be observed that during the medium values of modulation indices the proposed algorithm results in reduced common mode voltage variations with slightly increased ripple in line current

V. CONCLUSION

The dual inverter configuration with unbalanced input voltage is presented in this paper, which is having less complexity when compared to other diode clamped or H-bridge multilevel inverter topologies. With the convention carrier comparison approach at low modulation indices (less than 0.3), the dual inverter configuration will give high switching losses because of operation of both inverters. But with the proposed control strategy nearly 50% of switching losses are reduced as only one inverter is in the operation. Moreover, the proposed approach results in reduced harmonic distortion during the lower modulation indices. In the modulation index range from 0.3 to 0.6 common mode voltage variations can be reduced with the proposed approach with slightly increased ripple in line current because of low effective pole voltage. At high modulation index (greater than 0.6) both control strategies have same effects.

REFERENCES

[1] J. Holtz, "Pulsewidth Modulation – A Survey", ***IEEE Trans. Ind.Electron.***, vol. 39, no.5, pp. 410-420,Dec. 1992.

[2] Heinz Willi Van Der Broeck, Hans-ChristophSkudelny and Georg Viktor Stanke, "Analysis and realization of a Pulsewidth Modulator based on Voltage Space Vectors,"*IEEE Trans. Ind. Appl.*, vol. 24, no. 1, pp. 142-150, Jan/Feb 1998.

[3] G. Narayanan and V. T. Ranganathan, "Triangle comparison and space vector approaches to pulse width modulation in inverter-fed drives," *J.Indian Inst. Sci.*, vol. 80, pp. 409–427, Sep/Oct, 2000.

[4] D-W. Chung, J-S. Kim, S-K Sul, "Unified Voltage Modulation Technique for Real-Time Three-Phase Power Conversion," *IEEETrans. Ind. Appl.*, vol. 34, no.2, pp 374-380. 1998.

[5] M. R. Reddy, T. B. Reddy, J. Amarnath and D. S.Rayudu, "Space Vector Based Novel and Simple Unified Pulsewidth Algorithm for Induction Motor Drives" *IJJEC*,vol2, no.1, pp. 9-32,2010.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral point clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–522, Sep.1981.

[7] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo,B. Woo and P. Enjeti, "Multilevel converters — A survey," in Proc.European Power Electronics Conf. *(EPE'99)*, Lausanne, Switzerland,1999.

[8] Jos é Rodr ǵuez, J-S. Lai, *"* Multilevel Inverters: A Survey of Topologies,Controls, and Applications*"* *IEEE Trans.Ind. Electron.*, vol. 49, no. 4, pp 724-737,Aug 2002.

[9] E.G.Shivakumar, KGopakumar, S.K. Sinha, AndrePittet, V.TRanganathan: "Space vector PWM control of dual inverter fed openend winding induction drive," IEEE-APEC-2001, pp. 399-405, 2001.

[10] E.G. Shivakumar, K. Gopakumar, and V.T. Ranganathan, "Space vector PWM control of dual inverter-fed open-endwinding induction motor drive", *EPE J.*, col. 12, no. 1, pp. 9–18, 2002.

[11] V. T. Somasekhar and B. V. Reddy, "A New Four-level Dual Inverter fed Open-end Winding Induction Motor Drive," IEEE PEDS 2011, pp.167-170, 5 - 8 Dec, 2011.

[12] B. V. Reddy, V. T. Somasekhar, and Y. Kalyan, "Decoupled space vector PWM strategies for a four-level asymmetrical open-end winding induction motor drive with waveform symmetries," *IEEE Trans. Ind.Electron.*, vol. 58, no. 11, pp. 5130–5141, Nov. 2011.

[13] B. V. Reddy, V. T. Somasekhar, and Y. Kalyan, "A Dual Inverter Fed Four level Open-end Winding Induction Motor Drive With a nested Rectifier -Inverter," *IEEE Trans. Ind. informatics*, vol. 9, no. 2, pp. 938–946, May. 2013.

BIOGRAPHIES

M.Harshavardhanreddyreceived B.Tech degree from Rajeev Gandhi Memorial college of Engineering and Technology, Nandyal, Andhra Pradesh in 2009. He received M.Tech degree in power electronics and drives from Karunya University, Coimbatore in 2011. Currently, he is with G. Pulla Reddy Engineering College, kurnool, as an Assistant Professor. His areas of interests are power electronic control of drives.

Dr. T. Brahmananda Reddy graduated from Sri Krishna Devaraya University, Anantapur in the year 2001. He received M.E degree from Osmania University, Hyderabad, India in the year 2003 and Ph.D from J.N.T.University, Hyderabad in the year 2009. He is presently working as Professor and Head of Electrical and Electronics Engineering Department, G. Pulla Reddy Engineering College (Autonomous), Kurnool, India. He presented more than 100 research papers in various national and international conferences and journals. His research areas include PWM techniques, DC to AC converters and control of electrical drives

B.Ravindranath Reddy obtained his B.Tech degree in Electrical & Electronics Engineering from the J.N.T.U. College of Engg.,Anantapur in the year 1991. He obtained his M.Tech degree in Energy Systems from IPGSR of J.N.T.University Hyderabad in the year 1997. He obtained his doctoral degree from JNTUA, Anantapur University in the field of Electrical Power Systems. He is presently working as Executive Engineer in JNTUH. He has more than 12 research papers. His areas of interests are Power Systems, High Voltage Engineering and Control Systems. His research interests include Simulation studies on Transients of different power system equipment.

M.Suryakalavathiwas born on 8t^{h}july 1966. She obtained B.Tech degree from S.V.University in the year 1988 and M.Tech degree from same university in the year 1992. Obtained her doctoral degree from JNTU, Hyderabad and post doctroal from CMU, USA. She is presently the professor of in JNTU college of Engg. Hyderabad. She has published 30 research papers. Her research area includes simulation studies on transients of different power system equipment.