A Single Sensor, Single Switch Integrated PFC Buck-Boost Buck Converter Fed BLDC Motor Drive

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Abstract–This paper presents an integrated power factor correction (PFC) buck-boost buck converter based voltage source inverter (VSI) fed brushless DC motor (BLDC) drive using a single voltage sensor. The speed is controlled by controlling the DC bus voltage of the VSI. An electronic commutation of the BLDC motor is used which utilizes a fundamental frequency switching (FFS) of VSI which in-turn offers low switching losses; hence an efficient configuration is realized. A PFC integrated buck-boost buck converter is used as a front-end converter for its operation in a dual-discontinuous conduction mode (DCM) for DC link voltage control and PFC operation. An advantage of fast voltage regulation, with high power factor for wide range of voltage conversion and a zero current switching (ZCS) at turn-on is achieved in this configuration. The proposed drive is designed to achieve an improved power quality at the AC mains for a wide range of speed control with power quality indices under acceptable limits by international power quality standards such as IEC 61000-3-2.

Keywords–BLDC motor drive, buck-boost buck converter, PFC, power quality.

I. INTRODUCTION

Brushless DC (BLDC) motors are becoming popular due to advantages such as high efficiency, high torque/inertia ratio, ruggedness, high energy density, low electro-magnetic interference (EMI) and low maintenance requirement [1, 2]. This motor covers a wide range of applications in household, industrial and medical appliances. The BLDC motor consists of a three phase windings in the stator and permanent magnets on the rotor [3]. It is also known as electronically commuted motor (ECM) as electronic commutation based on the rotor position sensed by Hall Effect position sensor is required for its operation [4, 5]. This motor when fed by a diode bridge rectifier (DBR) with high value of DC link capacitor draws peaky current with crest factor (CF) as high as 3-5. This results in supply current distortion with total harmonic distortion (THD) of the supply current as high as 60-70% and power factor (PF) of the order of 0.8-0.85. These power quality (PQ) indices are not under the acceptable limits by international PQ standards such as IEC 61000-3-2 [6].

Single stage PFC (Power Factor Corrected) converters have been widely used for power quality improvement in BLDC motors [7]. An advantage of reduced losses in the converter stage is achieved due to use of single stage and single switch [8, 9].

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Moreover, simple control scheme is required for single stage as compared to multi-stage converter systems which require two different controls for PFC and voltage regulation [10]. An integrated PFC buck-boost buck configuration is used in this paper which utilizes a single switch and has following advantages [11]:

1.Low losses in single stage, single switch configuration.
2.Fast voltage regulation for improved dynamic performance.
3.PFC and improved power quality at AC mains over a wide voltage conversion ratio.
4.Switch turn on at zero current (ZCS- Zero Current Switching) for reduced losses in switch.

Total losses in a BLDC drive system consists of losses in PFC converter (P_{loss_conv}), losses in VSI (P_{loss_inv}) and losses in BLDC motor (P_{loss_motor}) itself as shown in equation (1). The inherent losses in BLDC motor can't be minimized due to the finite resistance of the stator's windings, frictional and magnetic losses. Moreover, the switching losses in AC-DC converter depends on the switching frequency which has to be kept high of the order of 50kHz for the effective operation of converter and reducing the size of inductors. Hence switching frequency of converter also can't be modified. But, the switching losses in the VSI can be reduced by using an electronic commutation of the BLDC motor which utilizes a fundamental frequency switching of the VSI.

$$P_{loss} = P_{loss\_conv} + P_{loss\_inv} + P_{loss\_motor} \quad (1)$$

$$P_{loss\_inv} = P_{loss\_switching} + P_{loss\_conduction} \quad (2)$$

As shown in equation (2) the switching losses and conduction losses of IGBT's in the VSI combines to give overall losses. Switching losses, which shares a major portion of total losses in the VSI, are proportional to the square of switching frequency which is reduced from 10-20kHz (for PWM operation) to few Hz's and the corresponding reduction in switching losses.

The PFC converter can be operated in CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode) of operation [8, 9]. A CCM operation uses a current multiplier approach which requires sensing of input voltage, input current and DC link voltage, hence requires three sensors. A reduced sensor configuration of BLDC motor drive is achieved by DCM operation of PFC converter which uses a voltage follower scheme for a single voltage sensor operation for PFC and DC link voltage control. But these advantages are achieved at the cost of higher stresses on the PFC converter switch; hence the evaluation of current and voltage stress become essential to determine the feasibility of the proposed BLDC motor drive.

II. PROPOSED INTEGRATED PFC BUCK-BOOST BUCK CONVERTER FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed BLDC motor system using an integrated PFC converter which is a combination of a PFC buck-boost and a buck converter. The speed control of BLDC motor is achieved by controlling the DC link voltage of the VSI [12]. This type of control provides a freedom to operate VSI in fundamental frequency switching mode for achieving an electronic commutation of the BLDC motor. This also reduces the switching losses many times as compared to the PWM (Pulse Width Modulation) switching. The performance of the proposed drive is evaluated for speed control over a wide range with improved power quality (i.e. high power factor and low supply current distortion) at the AC mains, satisfying the guidelines of IEC 61000-3-2. Performance is also evaluated for varying supply voltage to demonstrate the behavior for practical supply conditions. Moreover, voltage and current stress on the switch are also evaluated to determine the feasibility of proposed BLDC motor drive.

III. OPERATING PRINCIPLE OF AN INTEGRATED PFC BUCK-BOOST BUCK CONVERTER

The integrated PFC buck-boost buck converter is designed to operate in dual DCM such that currents in input inductor L_i and output inductor L_o become discontinuous in a switching period. Figs. 2 (a-d) and Fig. 2(e) show four different modes of operation and waveform of inductor currents and capacitor voltages during a single switching period respectively. Different modes of operation are described below.

Mode I: In this mode, switch S_w is turn on to charge the input inductor L_i with diode D_1 remaining in forward biased position to close the input side circuit as shown in Fig. 2(a). The current in input inductor L_i increases which rate of increase depends upon the instantaneous input voltage applied. The energy stored in intermediate capacitor C_1 starts discharging through switch S_w via output inductor L_o and diode D_3 to charge the DC link capacitor, C_d. Diodes D_2 and D_4 remain reversed biased during this mode and hence no current flows through them. As shown in Fig. 2(e), inductor's currents i_{Li} and i_{Lo} increase and the voltage across intermediate capacitor V_{C1} decreases in this mode.

Mode II: In this mode of operation as shown in Fig. 2(b), switch S_w is turned off; hence inductors L_i and L_o discharge their stored magnetic energy to charge the intermediate capacitor C_1 and DC link capacitor C_d. Diode D_3 remains in reverse blocking while diodes D_1, D_2 and D_4 conduct for achieving a required closed loop for energy transfer between inductors and capacitors. Voltage across intermediate capacitor (V_{C1}) starts increasing till the energy stored in inductor L_i becomes zero. At the end of this mode, input inductor current i_{Li} becomes zero and enters into DCM while still some energy is left in output inductor L_o due to its higher value of time constant ($\tau_o=L_oC_d$).

Mode III: In this mode, switch S_w remains in off position and input side is not supplying any energy to the converter

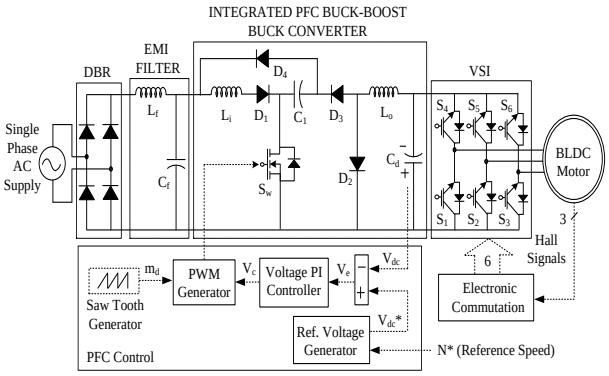

Fig. 1: Proposed Integrated PFC buck-boost buck converter fed BLDC motor Drive

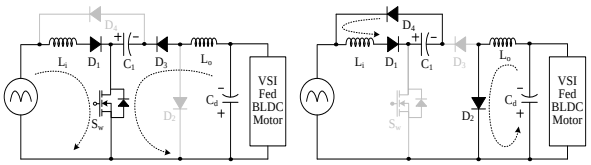

Fig. 2(a): Mode I

Fig. 2(b): Mode II

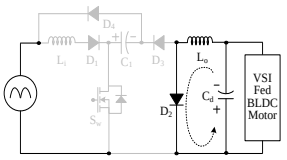

Fig. 2(c). Mode III

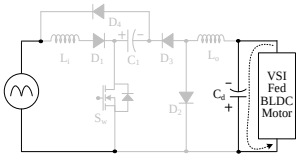

Fig. 2(d). Mode IV

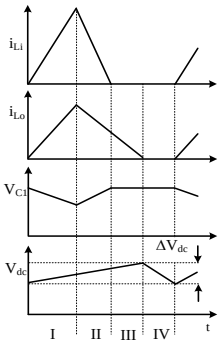

Fig. 2(e). Waveforms

Fig. 2: Different modes of operation of integrated PFC buck-boost buck converter

as shown in Fig. 2(c). Only output side inductor L_o transfers all of its energy to charge the DC link capacitor, hence the voltage V_{dc} continues to increase, while the voltage across the intermediate capacitor C_1 remains constant in this mode. At the end of this mode, inductor L_o is completely discharged and current i_{Lo} becomes zero.

Mode IV: As shown in Fig. 2(d) there is no energy left in input inductor L_i and output inductor L_o and hence converter enters into a dual DCM operation. The DC link capacitor supplies the required energy to the load and voltage across it reduces as shown in Fig. 2(e). The intermediate capacitor C_1 remains charged with its highest possible voltage. This mode is completed with the end of switching period and the complete cycle is repeated for the next switching state.

IV. DESIGN OF AN INTEGRATED PFC BUCK-BOOST BUCK CONVERTER

The design of integrated PFC buck-boost buck converter consists of designing and selection of optimum values of boost inductor (L_i), output filter inductor (L_o), intermediate

(bulk) capacitor (C_1) and DC link capacitor (C_d). The design of converter is based on the following specifications with BLDC motor rating given in Appendix.

P_m (Rated Power of BLDC motor) = 377W, P_o (Rated power of converter to be designed) = 450W, V_S (Supply RMS voltage) = 220V, V_{dcmax} (Rated DC link voltage) = 310V, V_{dcmin} (Minimum DC link voltage) = 70V, V_{dc} (Designed Value of DC link voltage which is average of maximum and minimum DC link voltage) = 190V, ΔV_{C1} (Permitted ripple voltage in intermediate capacitor) = 10% of V_{C1}, ΔV_{dc} (Permitted ripple voltage in DC link capacitor) = 1% of V_{dc}, f_S (Switching frequency) = 45kHz, f_L (Power frequency) = 50Hz.

The input average voltage after the DBR (rectified voltage) is calculated as [10],

$$V_{in} = \frac{2\sqrt{2}V_S}{\pi} = \frac{2\sqrt{2}\times 220}{\pi} = 197.98V \approx 198V \quad (3)$$

The output voltage, V_{dc} of given integrated PFC converter which is of buck-boost type is given as [9],

$$V_{dc} = \frac{D}{(1\text{-}D)} V_{in} \quad (4)$$

where D is the duty ratio.
From equation (3), the nominal duty ratio, D_{nom} corresponding to designed value of DC link voltage is calculated as,

$$D_{nom} = \frac{V_{dc}}{V_{dc}+V_{in}} = \frac{190}{190+198} = 0.4896 \quad (5)$$

The critical value of input inductor L_{icrit} to operate at boundary of CCM and DCM is given and calculated as [9],

$$L_{icrit} = \frac{V_{in}D_{nom}}{2f_S I_{in}} = \frac{198\times 0.4896}{2x45000\times(450/198)} = 473.93\mu H \quad (6)$$

The value of input inductor L_i is to be selected such that $L_i < L_{icrit}$ for DCM operation. Hence value of L_i is selected as 200 µH.
Similarly the critical value of output inductor L_{ocrit} is expressed as [9],

$$L_{ocrit} = \frac{V_o(1\text{-}D_{nom})}{2f_S I_o} = \frac{190\times(1\text{-}0.4896)}{2x45000\times(450/190)} = 454.94\mu H \quad (7)$$

Hence the value of magnetizing inductance L_o to operate in DCM is selected such that $L_o < L_{ocrit}$, hence a value of L_o is chosen as 200 µH.
The value of intermediate (bulk) capacitor C_1 is calculated as [9],

$$C_1 = \frac{V_{dc}D_{nom}}{f_s R_L \Delta V_{C1}} = \frac{190\times 0.4896}{45000\times(190^2/450)\times 0.1\times(398)} = 664.4nF \quad (8)$$

where the voltage V_{C1} across capacitor C_1 is sum of input and DC link voltage (i.e. $V_{C1} = V_{in} + V_{dc}$). Hence, value of intermediate (bulk) capacitor C_1 is selected as 500nF.
The value of DC link capacitor is calculated as [9],

$$C_d = \frac{I_{dc}}{2\omega_L \Delta V_{dc}} = \frac{(P_o/V_{dc})}{2\omega_L \Delta V_{dc}} = \frac{(450/190)}{2\times 314\times 0.01\times 190} = 1985\mu F \quad (9)$$

where I_{dc} is DC link current.

Hence the value of DC link capacitor is taken as 2200 µF.
To avoid the EMI problems due to high switching frequency reflection in the supply, an EMI filter is designed which is a LC filter with maximum value of filter capacitance C_{max} is given as [13],

$$C_{max} = \frac{I_{peak}}{\omega_L V_{peak}} \tan(\theta) = \frac{(P_o/V_s)}{\omega_L V_{peak}} \tan(\theta) = \frac{(450\sqrt{2}/220)}{314\times 311} \tan(3^\circ) = 341.5nF \quad (10)$$

where I_{peak} and V_{peak} are the peak input current and peak input voltage respectively and θ is the displacement angle.

The value of filter capacitance C_f is selected lower than C_{max}, hence the value of C_f is selected as 330nF.

The expression for the calculation of filter inductance L_f is given as [13],

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} = \frac{1}{4\pi^2 (4500)^2 \; ?\; 30?\; 0^{-9}} = 3.79mH \quad (11)$$

where f_c is the cut-off frequency such that $f_c = f_s/10$ [13].

Hence an inductance L_f of the order of 4mH is selected for input EMI filter.

V. CONTROL OF PROPOSED PFC CONVERTER FED BLDC MOTOR DRIVE

The control of an integrated PFC buck-boost-buck converter fed BLDC motor drive is classified into two controls of PFC converter and BLDC motor as follows.

A. Control of PFC Converter

A voltage follower approach for PFC and DC link voltage control is utilized for an integrated PFC buck-boost buck operating in dual DCM. In this mode of operation, it acts as an inherent power factor pre-regulator utilizing a single voltage sensor. The reference voltage V_{dc}* is obtained by multiplying the reference speed (N*) with the motor's voltage constant (k_v) as,

$$V_{dc}^* = k_v N^* \quad (12)$$

Now, this reference DC link voltage (V_{dc}*) is copmpared with sensed DC link voltage (V_{dc}) to generate a voltage error which is to be given to the voltage PI (Proportional-Integral) controller for necessary control action. The error voltage (V_e) is at any time instant '*k*' is given as,

$$V_e(k)=V_{dc}^{*}(k)-V_{dc}(k) \quad (13)$$

The voltage error obtained in equation (13) is given to the PI controller whose controlled output V_c is given as,

$$V_c(k)=V_c(k-1)+K_p\{V_e(k)-V_e(k-1)\}+K_iV_e(k) \quad (14)$$

where $V_c(k)$ and $V_c(k-1)$ represent the controller output at k^{th} and $k\text{-}1^{th}$ sampling instant and K_p and K_i are the proportional and integral gains of the PI controller.

The controlled output V_c as given in equation (14), is compared with a high frequency saw-tooth waveforms to generate PWM signals to be given to the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) of the PFC converter for the required voltage control.

B. Control of BLDC Motor: Electronic Commutation

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical DC current is drawn from the DC link capacitor for 120^0 and placed symmetrically at the centre of each phase. A Hall-Effect position sensor is used to sense the rotor position on a span of 60^0; which is required for the electronic commutation of BLDC motor. The conduction states of two switches (S_1 and S_4) are shown in Fig. 3. A line current i_{ab} is drawn from the DC link capacitor which magnitude depends on the applied DC link voltage (V_{dc}), back emfs (e_{an} and e_{bn}), resistances (R_a and R_b) and self and mutual inductance (L_a, L_b and M) of the stator windings. Table 1 shows the different switching states of the VSI feeding a BLDC motor based on the Hall Effect position signals (H_a-H_c).

VI. PERFORMANCE EVALUATION OF THE PROPOSED BLDC MOTOR DRIVE

The performance of the proposed BLDC motor drive is evaluated on the basis of PQ indices such as PF (Power Factor), DPF (Displacement Power Factor), DF (Distortion Factor), CF (Crest Factor) and THD (Total Harmonic Distortion) of supply current at AC mains. Various performance indices such as supply voltage (V_s) and supply current (i_s) are analyzed for power quality assessment. Indices such as DC link voltage (V_{dc}), speed (N), electromagnetic torque (T_e), stator current (i_{sa}), inductors current (i_{Li} and i_{Lo}) and intermediate capacitor's voltage (V_{C1}) are evaluated for demonstrating the proper functioning of BLDC motor and PFC converter. An improved power quality over a wide range of speed control of BLDC motor is achieved. The proposed drive is also evaluated for supply voltage variation to demonstrate the performance for practical supply situations. Moreover, switch stresses (v_{sw} and i_{sw}) are also analyzed for proper selection of switch and heat sink design.

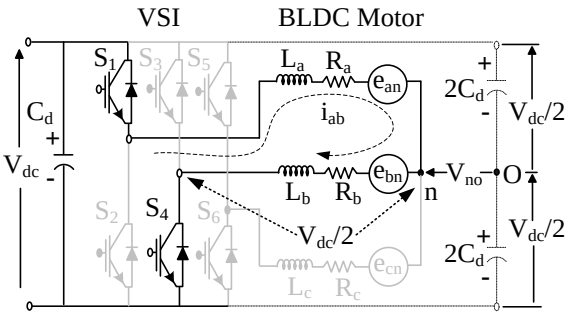

Fig. 3: A BLDC motor fed by a VSI showing the current flow when two switches S_1 and S_4 are in on state

Table 1: Switching states of VSI based on hall effect position sensor signal

θ^o	*Hall Signals*			*Switching States*					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

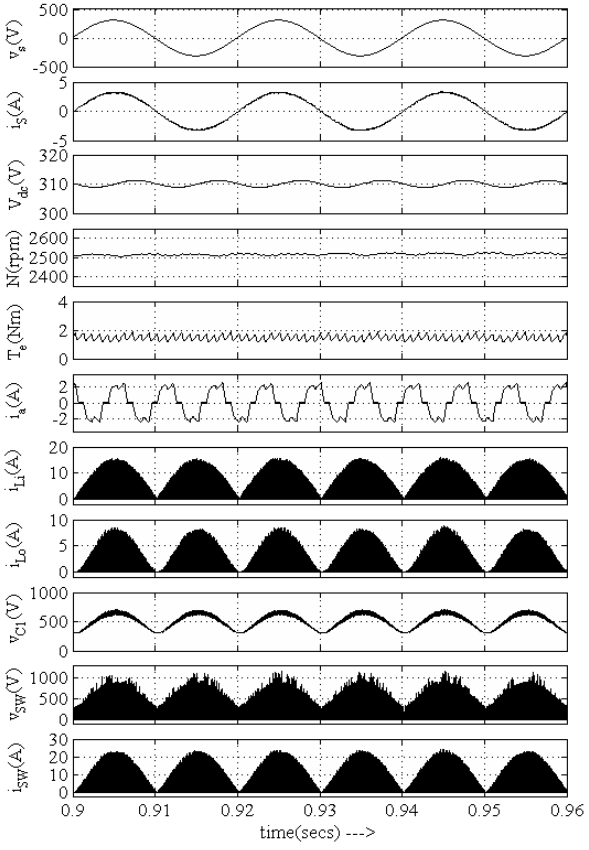

Fig. 4: Steady state behavior of the proposed drive at rated load on BLDC motor.

Fig. 4 shows the steady state behavior of the proposed drive system on a magnified scale. As shown in the figure, supply current (i_s) is in phase with supply voltage (v_s) and is sinusoidal in nature which shows a near unity DPF and near unity DF, hence a near unity PF (PF=DF*DPF) is obtained at the AC mains. The DC link voltage (V_{dc}) is maintained at the rated value of 310 V which corresponds

to the speed of 2500 rpm (N) of BLDC motor. An electromagnetic torque of the order of 1.7 Nm is achieved with a limited ripple in the torque (T_e) and stator current (i_a) showing the proper operation of BLDC motor. A discontinuous current is achieved in input and output inductor (i_{Li} and i_{Lo}), whereas the intermediate capacitor's voltage (V_{C1}) remains in continuous conduction for a switching period. This verifies the dual DCM operation of an integrated PFC buck-boost buck converter. As shown, in this figure, the peak voltage (v_{sw}) and current (i_{sw}) stress of the order of 900 V/22 A is achieved on the PFC converter switch. Table 2 shows the various performance indices for speed control of BLDC motor by controlling the DC link voltage from 70V (buck mode) to 310V (boost mode). A high power factor of the order of 0.99 and THD of supply current below 5% is obtained for a wide voltage conversion ratio (wide speed control) satisfying the acceptable limits of international PQ standard IEC 61000-3-2. A zero current switch turn on phenomena (ZCS turn on) is obtained as shown in Fig. 5. This is achieved to due to operation of PFC converter such that the switch voltage (V_{sw}) becomes zero during the turn-on of PFC converter switch as shown in Mode-III and Mode-IV in Fig.2. This reduces switching losses in a PFC converter due to zero current appearing across the switch during the turn-on.

Table 2: Performance of integrated PFC buck-boost buck converter fed BLDC motor drive under speed control

V_{dc} (V)	Speed (rpm)	THD of I_s (%)	DPF	PF	I_s (A)
70	260	3.31	0.9999	0.9994	0.5118
90	440	3.05	1	0.9995	0.643
110	640	2.94	1	0.9996	0.7758
130	820	2.82	1	0.9996	0.9115
150	1030	2.77	0.9999	0.9995	1.048
170	1200	2.56	0.9998	0.9995	1.192
190	1460	2.43	0.9997	0.9994	1.339
210	1610	2.39	0.9997	0.9994	1.478
230	1780	2.37	0.9995	0.9992	1.63
250	1970	2.14	0.9993	0.9991	1.767
270	2100	1.78	0.9992	0.999	1.926
290	2350	1.74	0.9988	0.9986	2.087
310	2520	1.64	0.9985	0.9984	2.218

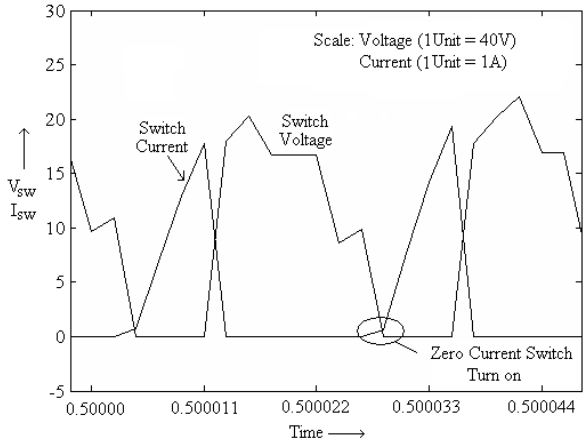

Fig. 5: Switch voltage and current showing the zero current switch turn on phenomenon.

Fig. 6 shows the dynamic behavior of the proposed BLDC motor drive system during speed control. As shown in this figure, the BLDC motor is started at DC link voltage of 100V and the speed is varied corresponding to change in DC link voltage from 100V to 300V at 0.35s. A smooth control of DC link voltage (V_{dc}) is achieved i.e. smooth control of speed limited transients in supply and stator current; which demonstrates the proper functioning of control loop. A rate limiter is used to limit the sudden change in parameters like voltage or current. Table 3 shows the evaluated performance for supply voltage variation from 170V-270V to demonstrate the behavior of proposed drive for practical supply condition. PQ indices obtained are within the recommended limits of IEC 61000-3-2.

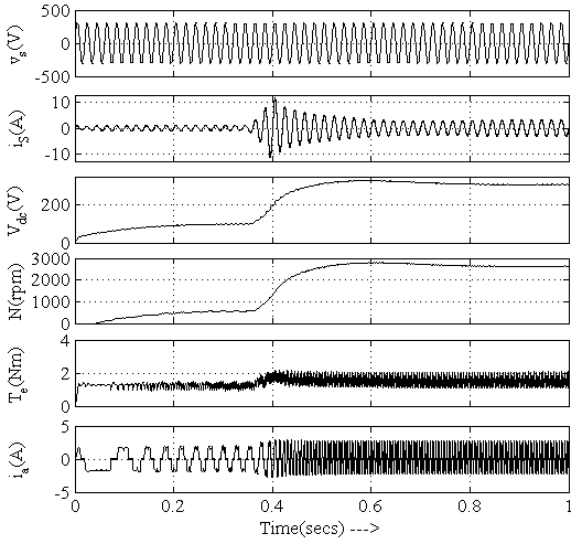

Fig. 6: Dynamic behavior of proposed drive during starting and speed control

Table 3: Performance of proposed BLDC motor drive under varying supply voltage

V_s (V)	THD of I_s (%)	DPF	PF	I_s (A)	CF
170	1.41	0.9999	0.9953	2.805	1.414
180	1.47	0.9999	0.9964	2.634	1.414
190	1.52	0.9999	0.9971	2.505	1.414
200	1.58	0.9999	0.9978	2.383	1.414
210	1.61	0.9999	0.9982	2.305	1.414
220	1.64	0.9999	0.9984	2.218	1.414
230	1.72	0.9999	0.9987	2.14	1.414
240	1.85	0.9998	0.9991	2.08	1.414
250	1.94	0.9998	0.9992	1.985	1.414
260	2.11	0.9998	0.9993	1.892	1.414
270	2.34	0.9997	0.9993	1.844	1.414

Table 4: Voltage and current stresses under different loading

Load (%)	v_{sw} (V)	i_{peak} (A)	i_{rms} (A)
10	900	13	0.3974
20	900	14	0.53
30	900	15	0.6647
40	900	16	0.7954
50	900	17	0.981
60	900	18	1.16
70	900	19	1.215
80	900	20	1.27
90	900	21	1.374
100	900	22	1.52

Harmonic spectra of supply current for DC link voltage of 310V and 70V are shown in Fig. 7(a) and Fig. 7(b) respectively. The THD of supply current obtained is well maintained below 5% for both cases. Stresses on the PFC converter's switch in term of peak voltage stress (V_{sw}), peak current stress (i_{peak}) and rms value of current (i_{rms}) flowing through switch are evaluated for different loading on BLDC motor and is tabulated in Table 4. Fig. 8 (a) and Fig. 8 (b) show the PF and THD of supply current with respect to DC link voltage and supply voltage respectively. A unity power factor for both mentioned cases and THD of supply current below 5% are obtained for the complete range of DC link voltage and supply voltage variation. Peak current and voltage stress are used for proper rating selection of switch, whereas rms current is used for heat sink design. The performance of the proposed drive seems to be satisfactory in all aspects and is a good solution for a low cost, high efficiency BLDC motor drive system.

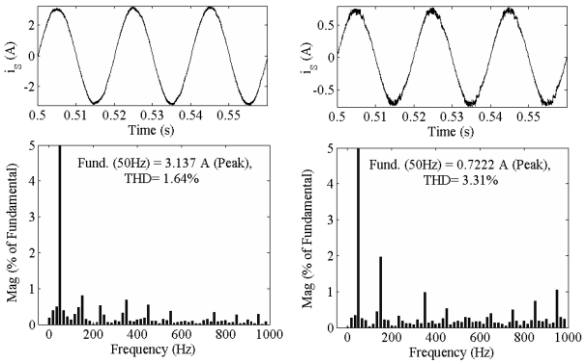

Fig. 7(a) Fig. 7(b)

Fig. 7: Harmonic spectra of supply current at rated conditions with DC link voltage as (a) 310V and (b) 70V.

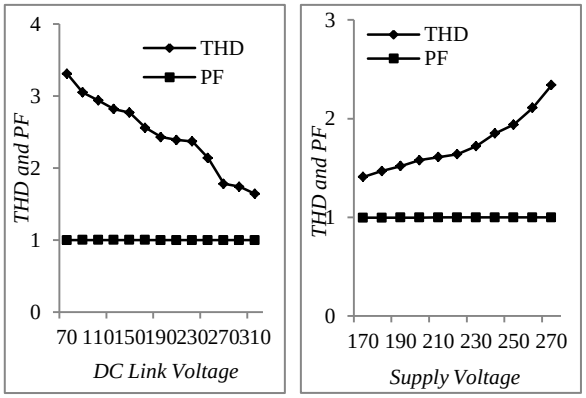

Fig. 8(a) Fig. 8(b)

Fig. 8: Variation of THD of supply current and PF at AC mains with (a) DC link voltage and (b) supply voltage.

VII. Conclusion

An integrated PFC buck-boost buck converter has been proposed for BLDC motor drive. The speed of BLDC motor has been controlled by varying the DC link voltage of VSI using a single voltage sensor. The PFC converter has been designed to operate in dual DCM operation for PFC and DC link voltage control. A zero current switch turn-on of PFC converter has been implemented for enhancing the efficiency of proposed drive. A fundamental frequency switching of VSI has been used for reducing the switching losses in VSI. The performance of the proposed drive has been evaluated for a wide range of speed control and supply voltage variation with PQ indices obtained within the acceptable limits by international PQ standard IEC 61000-3-2. The proposed BLDC motor drive is a recommended solution for many low power applications with speed control and improved power quality at the AC mains.

Appendix

BLDC Motor Rating: 4 poles, P_{rated} (Rated Power) = 0.5 hp (377W), V_{rated} (Rated DC link Voltage) = 310 V, T_{rated} (Rated Torque) = 1.2 Nm, ω_{rated} (Rated Speed) = 3000 rpm, K_b (Back EMF Constant) = 78 V/krpm, K_t (Torque Constant) = 0.74 Nm/A, R_{ph} (Phase Resistance) = 14.56 Ω, L_{ph} (Phase Inductance) = 25.71 mH, J (Moment of Inertia) = 1.3x10-4 Nm/s^2.

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