Hardware Enactment for Sagacious Compensation by Single Phase Dynamic Voltage Restorer

R. J. Satputaley [1] V. B. Borghate [2] M. A. Chaudhari [3] B.H. Naik [4]

Abstract–This paper discusses the hardware implementation of single phase dynamic voltage restorer for the mitigation of voltage sag. The contribution of dynamic voltage restorer for mitigation of voltage sag is first tested by simulation in PSCAD software. The simulated results are validated by an experimental prototype in laboratory. A low power dynamic voltage restorer is built for experimental verification. d-SPACE RTI-d1104, is used for providing gating pulses to the inverter in DVR. Dynamic voltage restorer is implemented for mitigating the sag in open loop control mode as well as close loop control mode. Selected experimental results are reported with analytical findings which show the effectiveness of proposed dynamic voltage restorer for voltage sag mitigation. The proposed DVR is also able to keep total harmonic distortions of load voltage within permissible THD voltage limit.

Keywords–Dynamic voltage restorer (DVR), voltage sag, sinusoidal pulse width modulation (SPWM), power quality, total harmonic distortion (THD).

I. INTRODUCTION

Power quality issues are one of the major concerns in this modern era of industrial power consumer. It is due to increase use of sensitive and critical equipments in the system such as communication system, process industries precise manufacturing process etc. Among the entire power quality disturbances, voltage sag is most common and frequently occurring phenomenon in distribution system [1]. In electrical grid system it is not possible to avoid voltage sag because of finite clearing time of faults that cause the voltage sag and propagation of sags from the transmission and distribution system to the low voltage load. Voltage sag is the common reasons for interruption in production plants and for end user equipment malfunction in general. Most of the research work is concentrated on voltage sag analysis and its mitigation [2].

In order to overcome this problem, the concept of custom power devices is introduced [3-4]. Custom power devices are mainly of three categories such as series connected compensator i.e. dynamic voltage restorer (DVR), shunt connected compensator (DSTATCOM) and a combination of series and shunt connected compensator known as unified power quality conditioner (UPQC). Among all these DVR is found to be a cost effective solution for voltage sag mitigation [5]. The DVR can regulate the load voltage from the problems such as sag, swell and harmonics in the supply voltage. Hence, it can protect the critical consumer loads from tripping and consequent losses. Implementation of the DVR have been proposed at a low voltage (LV) level as well as a medium voltage (MV) level and serves to protect the high power sensitive loads from voltage sags. DVR is made up of solid state switching devices. It is power converter that injects the a.c. voltage in series and synchronism with the distribution feeder voltage. The amplitude and phase angle of injected voltages are variable, thereby allowing control of real and reactive power exchange between the DVR and distribution system.

In this research work, a single phase DVR operation for voltage sag mitigation in open loop as well as close loop is presented. To verify theoretical performance, the simulation is carried out in PSCAD software and then hardware prototype model of DVR is developed in laboratory. d-SPACE RTI-d1104 is used for providing the gate pulses in open loop as well as close loop control modes. Finally simulation results followed by experimental results are presented.

This paper is organized as: Principle operation of DVR is explained in section II. The details of compensation technique which is used for sag mitigation is discussed in section III. The simulated and experimental results for open loop and closed loop control of DVR are illustrated in section IV. The conclusion is given in section V.

II. PRINCIPLE OF OPERATION OF DVR

The schematic diagram of a typical single phase DVR used for voltage correction is shown in Fig. 1. The DVR consist of voltage source converter, an injection transformer, passive filter and energy storage [6-7]. In this research work rectifier is used for D.C. link. When the supply voltage V_s changes, the DVR injects a voltage V_{inj} in such a way that the desired load voltage magnitude can be maintained. The DVR is simply a voltage source inverter that produces an ac output voltage and injects in series with supply voltage through injection transformer. Fig. 2 shows the equivalent diagram of DVR and principle of series injection for voltage sag compensation. From Figs. 1, 2 and 3 neglecting Z_{line} and Z_{dvr}

$$\vec{V}_L = \vec{V}_s + \vec{V}_{inj} \quad (1)$$

where $\vec{V}_L$ is load voltage, $\vec{V}_s$ is supply voltage and $\vec{V}_{inj}$ is the injected voltage by DVR. Depending on the injection control scheme used, explained in section 3 the injected voltage of DVR can be calculated using equation (1).

III. COMPENSATION TECHNIQUE FOR DVR

Voltage injection or compensation methods by means of a DVR depend upon the factors such as; DVR power rating, various conditions of load and different types of voltage sag. Some loads are sensitive towards phase angel jump, some are sensitive towards change in magnitude and others are tolerant to these. Therefore the control strategies depend upon the type of load characteristics. There are different methods of DVR voltage injection [5], [8-10] which are

- In-phase compensation method

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- Pre-sag compensation method
- Phase advanced compensation method

A. In-Phase Compensation

In this method, the DVR voltage is injected in phase with the supply voltage [10]. When the load voltage drops due to sag, DVR will inject voltage depending on the dropped voltage magnitude in phase with the sag voltage regardless of load current and pre-sag voltage. Thus for load terminal, voltage during sag and pre-sag is same. This is the simplest way to mitigate voltage sag without phase angle jump. The advantage of this method is that the magnitude of injected DVR voltage is minimized for constant load voltage magnitude. Because in this method the load voltage is algebraic sum of sag voltage and injected voltage. For compensating the sag with phase angle jump generally pre-sag compensation technique is used.

Fig. 3 shows the phasor diagram of different voltage injection schemes of DVR. $V_{L(pre\text{-}sag)}$ is a voltage across the critical load prior to the voltage sag condition. During the sag condition supply voltage is reduced to V_{sag} with angle θ. Now, the DVR injects a voltage such that the load voltage magnitude is maintained at the pre-sag condition. V_{inj1} in Fig. 3 represents the voltage injected in phase with supply voltage.

B. Pre-Sag Compensation

The pre-sag compensation method tracks the supply voltage continuously and compensates load voltage during sag to restore the pre-sag condition. V_{inj2} in Fig. 3 shows the single-phase vector diagram of the pre-sag compensation. In this method the injected active power cannot be controlled and it is determined by external conditions such as type fault and load conditions. The injected voltage requirement is more compared to in-phase injection scheme.

C. Phase-Advanced Compensation

In pre-sag compensation and in-phase compensation methods the DVR must inject the active power to the load almost all the time. But in phase advanced compensation the injected voltage phasor is perpendicular to load current phasor, because of which active power supplied by DVR is zero. V_{inj3} in Fig. 3 represents the phase advanced compensation. Injection voltage magnitude is larger in phase advanced compensation as compared to pre-sag and in- phase compensation. But all the sags cannot be restored without real power; as a consequence, this method is only suitable for a limited range of sag.

From the phasor diagram shown in Fig. 3 it is clear that a minimum possible rating of converter is achieved with in-phase injection scheme. So in this paper, in-phase compensation control scheme for DVR is implemented to reduce the rating of DVR. In in-phase compensation method th**e** rating of DVR can be given as [8]

$$S_{DVR} = V_{DVR} \times I_L^* \quad (2)$$

$$I_L = \frac{(P_L + jQ_L)}{V_L} \quad (3)$$

For this research work sensitive load is resistive load

$$S_{DVR} = V_{DVR} \times I_{DVR} \quad (4)$$

where

$$I_{DVR} = I_L \quad (5)$$

V_{DVR} is the maximum voltage injected by the DVR in phase with supply voltage and I_L is the load current. The active power consumption of DVR should not exceed a certain value, since it increases the power rating of DVR. If the injected voltage of DVR exceeds a certain value, the active power consumption of the DVR violates the power limit. Hence the maximum injection of DVR voltage should not go beyond a value 0.5 *p.u.* Hence the maximum voltage injected by DVR is 50 % of supply voltage.

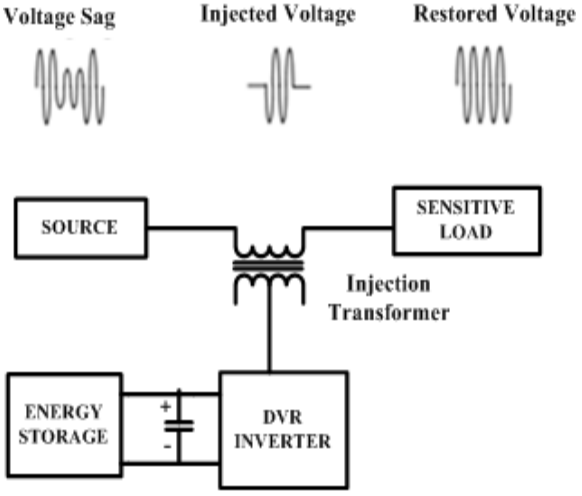

Fig. 1: Schematic diagram of DVR

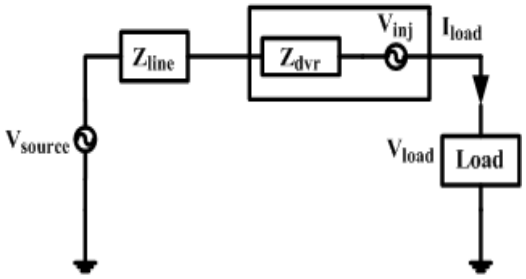

Fig. 2: Single phase equivalent circuit of DVR

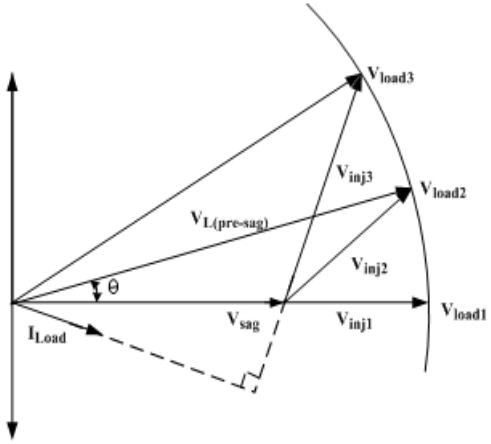

Fig. 3: Phasor diagram of DVR voltage injection scheme

IV. Simulated and Hardware Results

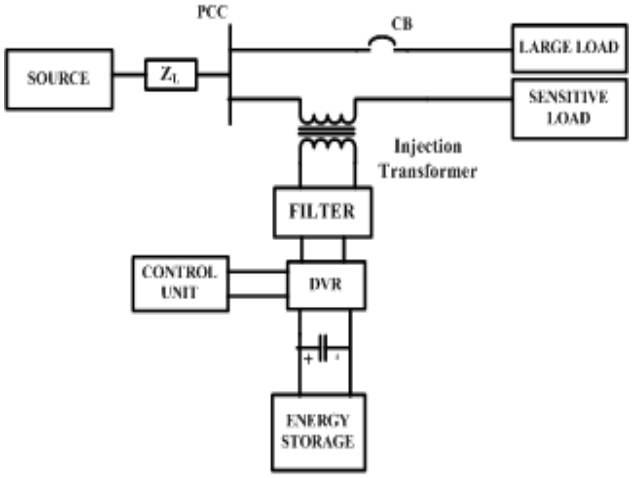

Fig. 4: Study case

A. Open Loop Performance

Fig. 4 shows the test system under consideration to carry out the transient modeling of DVR for software and hardware analysis [11]. The test system comprises of 115 volt a.c. transmission systems. A heavy load is connected at the PCC through circuit breaker which is in parallel with the sensitive load. A single phase VSI based DVR is connected in series with the sensitive load to provide instantaneous voltage support at the load point and during voltage sag. The voltage sag is occurred at PCC and load points due to sudden switching of heavy load due to presence of source and transmission line impedance.

a. Simulation Result

The above study case is first simulated in PSCAD for open loop control of DVR. The system parameters for simulation and hardware are given in Table 1. Fig. 5 shows the study case implemented in PSCAD. The sag is created by switching on heavy load during a period of 0.3 to 0.6 sec. Fig. 6 shows the waveform of source voltage and load voltage without DVR. The source voltage is 162 V peak to peak. The pre-sag load voltage is 155 V peak to peak and during sag it reduced to 122 V. The PCC and load voltage will experience sag but source voltage remains unaffected. Fig. 7 shows the rms value of source voltage and load voltage without DVR. The source voltage is 115 V, and the load voltage without sag is 110 V and during sag is 88 V. It is seen that the voltage at load point experiences the sag of 22 V with respect to pre-sag load voltage

At the point of sag, DVR is turned on. The load voltage during sag is measured and compared it with the reference voltage and generated as an error signal to operate the VSI to produce the required voltage, which is injected in series with sag voltage i.e. nothing but the PCC voltage in this case to mitigate the sag. Fig. 8 shows the instantaneous waveform of source and load voltage with DVR. The output of DVR which is injected is without filter. Fig. 9 shows rms value of source and load voltage with DVR. From the Fig. 9, it is clear that the load voltage is maintained constant to pre-sag value of 110 V with the operation of DVR.

Table 1: System parameters

Parameter	Specification
Source Voltage	115V
Load Voltage	110 V
Sensitive Load	40 W
Heavy load	1000 W
Switching Frequency	1 kHz
Injection Transformer	110/110 V, 1 kVA
Filter Inductance	10 mH
Filter capacitor	105 µF, 250 V
Transmission line impedance	3 Ω

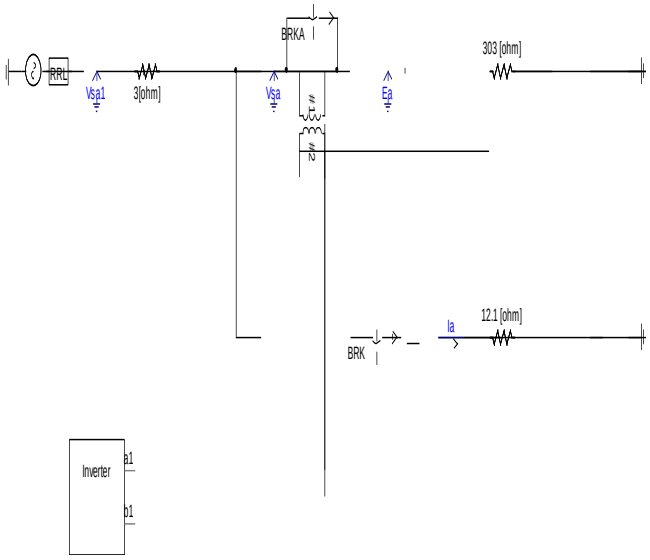

Fig.5: Test system implemented in PSCAD

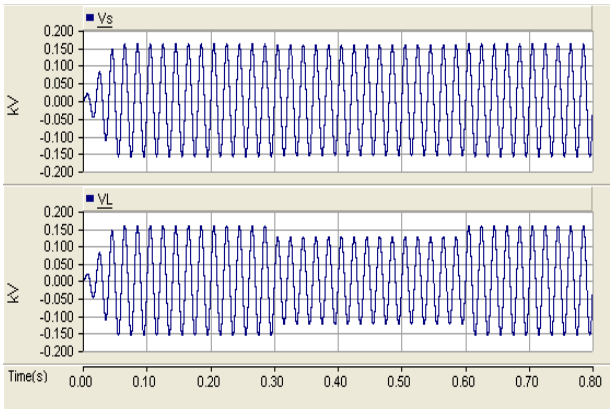

Fig. 6: V_s- source voltage and V_L- load voltage without DVR

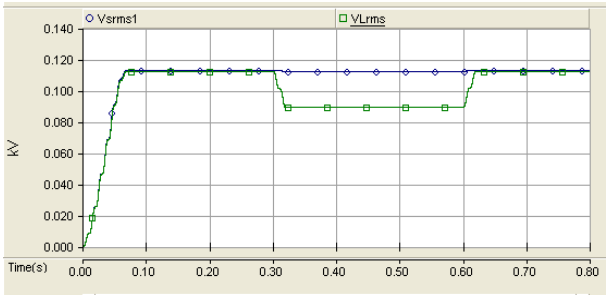

Fig. 7: RMS value of V_s- source voltage and V_L-load voltage without DVR

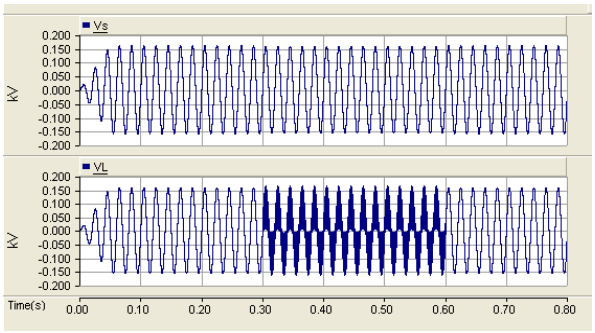

Fig.8: V_s- source voltage and V_L-load voltage with DVR

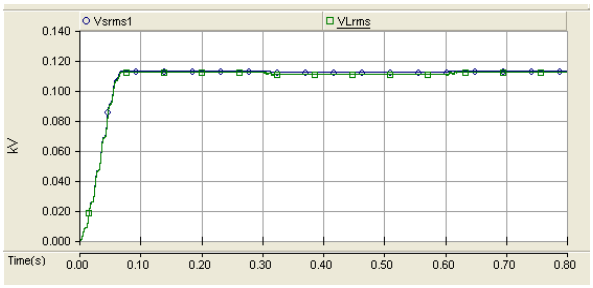

Fig. 9: RMS value of V_s-source voltage and V_L-load voltage with DVR

b. Experimental Results

A real time hardware set up has been implemented to explore the function of DVR to mitigate the voltage sag. The complete hardware setup circuitry of DVR is shown in Fig. 10. It shows the source, sensitive load, heavy load, injection transformer, LC filter of DVR and d-SPACE RTI d-1104. The MOSFET IRF460 is used as switches for power circuitry of voltage source inverter. Gate driver IC MIC4425, Opto-coupler 6N137 and buffer IC 74Ls07 are used for gate driver circuit. Voltage sensors are used to sense the load voltage and reference voltage.

Intentionally sag has been induced by switching on a heavy load suddenly, which is connected in parallel to the sensitive load at PCC. DVR is connected in series with the sensitive load and gate pulses provided for the inverter through d-SPACE system. The load voltage is continuously measured by using voltage sensor. A differential probe has been used with a multiplying factor of '20X' for every measurement throughout the tenure of the project. The experimental waveforms of source voltage, load voltage, injected voltage and inverter output voltage without DVR operation are shown in Fig. 11. The source voltage is 16 *V* peak to peak (i.e. *rms* 115 *V*) is shown in channel 1. The load voltage is shown in channel 2, pre-sag load voltage is 15.6 $V_{p\text{-}p}$ (i.e. 110 V_{rms}) and during sag it dips to 88 V_{rms}. The voltage across DVR is shown in channel 3 and across inverter is shown in channel 4. It is observed that the voltage across the inverter is zero since no gate pulses have been provided to the inverter; that is DVR is not injecting the voltage.

Fig. 12 shows all above four voltage waveforms when DVR is injecting the voltage in open loop. Point A on channel 2 of Fig. 12 indicates the occurrence of sag due to switching on heavy load which dips the sensitive load voltage to 88 V_{rms} value. It means that sag has occurred by 22 V_{rms}. Now the contribution of DVR comes into picture. Area B indicates the time period when DVR is in operation. Channel 3 shows the injected voltage of DVR which is 22 V_{rms}. So it is observed that load voltage has been recovered to 110 V_{rms} with injection of DVR voltage. The point C shows the time when DVR is turned OFF. To have a clear understanding regarding the operation of DVR, the sag is continued even after point C. Channel 4 shows the inverter output voltage during operation of DVR. The DVR output is filtered and then it is injected to the supply voltage i.e. PCC voltage to carry out in phase injection. THD analysis of load voltage after injecting the voltage through DVR is carried out for open loop condition and it is as shown in Fig. 13. The THD of load voltage during DVR operation is 4.22%, which is within permissible limit. The comparison of source and load voltage during sag and pre-sag condition for open loop system is given in Table 2.

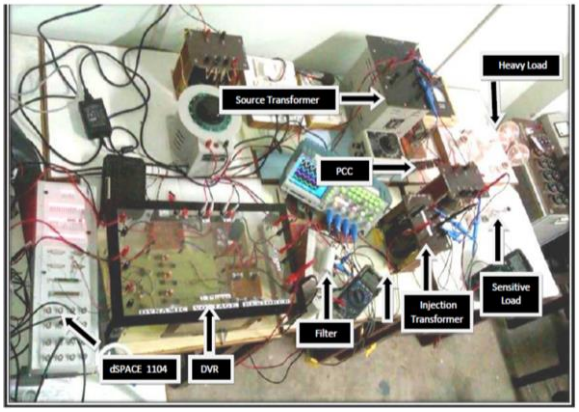

Fig.10: Complete hardware setup for DVR operation

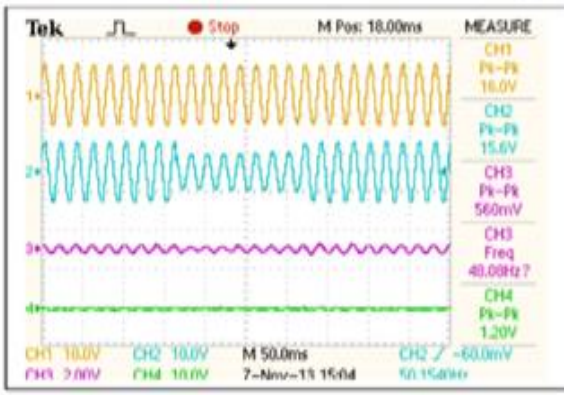

Fig. 11: Experimental waveforms without DVR Ch.1- source voltage, Ch.2- load voltage, Ch.3- injected voltage and Ch.4- voltage across inverter

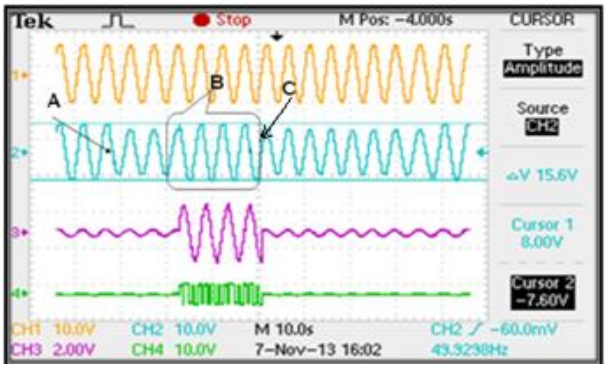

Fig. 12: Experimental waveforms with DVR Ch.1- source voltage, Ch.2 -load voltage Ch. 3- injected voltage and Ch. 4- inverter output voltage

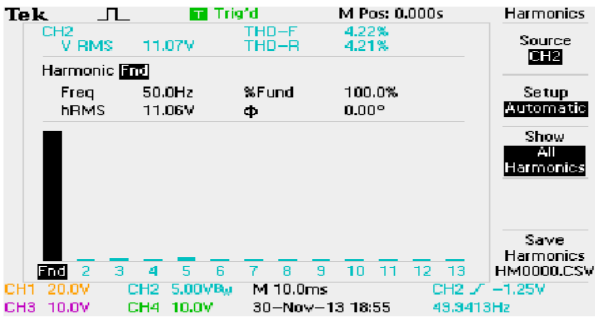

Fig. 13: Harmonic spectrum of load voltage

Table 2: Comparison of different voltages

Measured Voltage (Peak–Peak)	RMS Voltage
Vs = 16.0	115 V
V_L= 15.6	110 V (pre-sag voltage)
V_L= 12.4	88 V (During sag without DVR injection)
Sag Voltage =3.2	22 V (drop in voltage)
DVR = 3.2	22 V (injected voltage)
V_L= 15.5	110 V (with DVR)

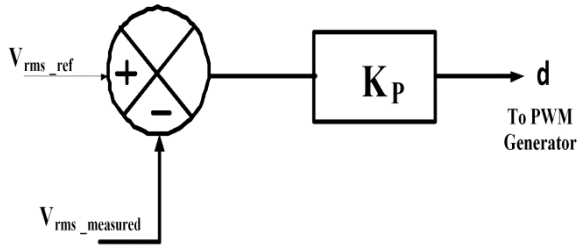

Fig. 14: Basic control scheme for DVR

B. Closed loop Performance

a. Simulation Results

A block diagram for control scheme for DVR is shown in Fig. 14. P controller is used in this research work as it is simple to design. It is based on measurements of the *rms* voltage (V_{rms}) at the load point. The voltage error signal is obtained by comparing measured V_{rms} against reference voltage, $V_{rms\text{-}ref}$ [12-13]. The difference between these two signals is processed by P controller, and the P-controller output is use to generate the pulses through PWM generator for triggering voltage source inverter. The value of K_p is calculated to keep the error minimum and to maintain modulation index 0.8.

For better observation the source voltage is increased to 125 V (i.e. 177 V_{peak}). The load voltage without sag is 123V (i.e.174 V_{peak}). Dip sag has been created by connecting heavy load during 0.3 to 0.6 s. The load voltage dips to 88 V_{rms} (i.e.121 V_{peak}). Fig. 15 shows the waveforms of load voltage without and with DVR. The *rms* value of source and load voltage with DVR is shown in Fig. 16. From Fig. 15 and 16 it is clear that with the operation of DVR value of load voltage is also restored to its pre-sag value.

b. Experimental Results

Fig. 17 shows the source and load voltage without DVR in close loop operation. Channel 1 shows 17.6 $V_{p\text{-}p}$ (i.e. 125 V_{rms}). Channel 2 shows the load voltage. Voltage across the load under pre-sag condition is 17.5 V (i.e.123 V_{rms}). When the heavy load is suddenly switched on sensitive load voltage is suddenly dips to 85 V_{rms}. It means that sag has been occurred for 39 V_{rms}. Fig. 18 shows the source voltage (Channel 1), load voltage (Channel 2) and injected voltage of DVR (Channel 3) during DVR operation. Point A on waveform 2 indicates the occurrence of sag. Area B indicates the time period of operation of DVR. The injected voltage of 36 V_{rms} by DVR has been observed in channel 3. The load voltage is maintained nearly constant as that of pre-sag value during the sag condition the comparison of load voltage during pre-sag and sag condition is given in Table 3.

The THD analysis of the load voltage during DVR operation is carried out as shown in Fig. 19. The THD value is 3.79% which is slightly reduced as compared to THD in open loop. Thus the DVR maintain the sensitive load voltage during sag condition with low THD.

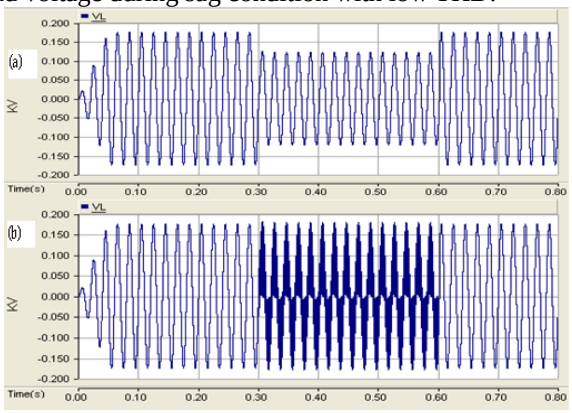

Fig. 15: (a) load voltage without DVR (b) load voltage with DVR

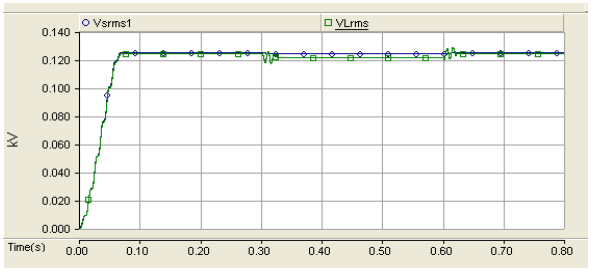

Fig. 16: RMS value of V_s- source voltage and V_L- load voltage with DVR

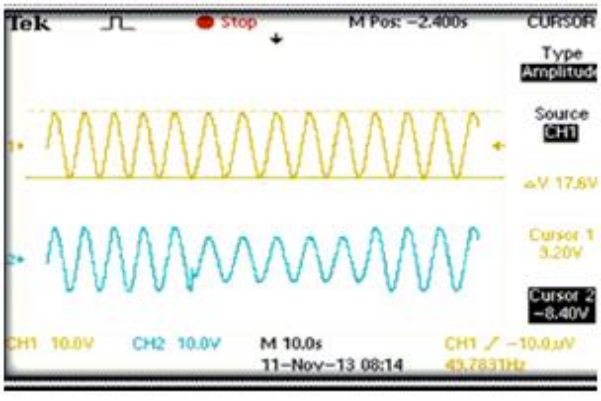

Fig. 17: Experimental waveforms without DVR Ch.1- source voltage Ch.2 -load voltage

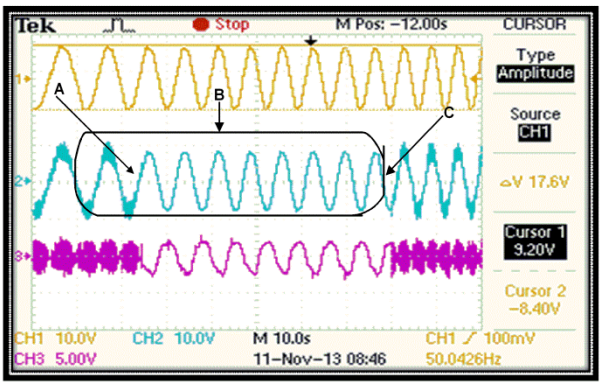

Fig.18: Experimental waveforms with DVR Ch.1 source voltage, Ch. 2 -load voltage and Ch.3- injected voltage

Table 3: Comparison of different voltage

Measured Voltage ($V_{p\text{-}p}$)	RMS (Volts)
V_s = 17.6	125
V_L= 17.5	123 (Pre-sag)
V_L= 12.0	85 (during sag)
Sag = 5.6 $V_{p\text{-}p}$	39 (drop in voltage)
DVR injection = 5	36 (injected voltage)
V_L=17.2	121(with DVR)

Fig. 19**:** Harmonic Spectrum of load voltage under close loop operation

V. CONCLUSION

VSC based single-phase DVR is lighter, cheaper and expandable to multilevel version to enhance the performance with lower switching frequency and it is popular in UPS based application. In this research work capability of single phase VSC based DVR for voltage sag mitigation in open loop as well as close loop is tested by actual prototype of DVR for study case. The operation of DVR is demonstrated in in-phase injection control scheme to reduce the rating of DVR. The simulation of DVR for mitigation of voltage sag is first carried out in PSCAD software. The simulated results are confirmed by experimental results. From the results, it is observed that the proposed DVR mitigates the voltage sag. It is found that the THD of sensitive load voltage is within permissible limit with the use of DVR under both open loop as well as close loop control.

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