Asian Power Electronics Journal, Vol. 11, No. 1, July 2017

Mitigation of PQ Disturbances using Unit-Template Control Algorithm based DSTATCOM

J.Bangarraju[1] V.Rajagopal[2] A.Jayalaxmi[3]

Abstract–This paper presents unit-template based control algorithm for Distributed Static Compensator (DSTATCOM) to mitigate Power Quality (PQ) disturbances in the three phase distribution system. The proposed DSTATCOM can be operated in Power Factor Correction (PFC) and Zero Voltage Regulation (ZVR) modes to mitigate PQ disturbances such as elimination harmonics, load balancing, unity power factor at the source and terminal voltage regulation. The main feature of this unit template control Algorithm is it requires only five sensors whereas conventional control algorithm requires ten sensors which reduces the cost of DSTATCOM. In this paper, four-leg VSC based DSTATCOM is used for neutral current compensation. The main advantage of four-leg VSC is eliminating transformer at Point of Common Coupling (PCC) which also reduces cost of DSTATCOM. The unit template based control algorithm for DSTATCOM is modeled in MATLAB environment using Simulink and Sim Power System (SPS) toolboxes and results are validated.

Keywords–DSTATCOM, Unit Template Control Algorithm, Power Quality, neutral current compensation.

I. INTRODUCTION

The use of power electronic converters is increasing in day to day life because they are energy efficient, compact and reliability compared to other systems [1]-[2].But main disadvantage of these power electronic converter are generates harmonic currents at source as well as load which effects performance of distribution system. These harmonic currents are responsible for drawing more reactive power from AC source and which causes voltage distortion and loss in the three-phase distribution system [3]. Power Quality (PQ) problems are defined in terms of deviation in voltage/current waveforms, unbalance, distortion, reactive power drawn [4].Many standards and guidelines are used in the design of power systems with nonlinear loads [5]-[6].

The performance of shunt connected device namely DSTATCOM depends upon control algorithm and design of its power circuit [7]-[9]. The performance of DSTATCOM depends on the selection of interfacing of ac inductor, DC bus capacitor and IGBTs [10].The various control algorithms reported in the literature are sinusoid-tracking algorithm [11], parallel neural network based algorithm [12],ABC theory based control algorithm [13],repetitive control algorithm [14],delta modulation based control [15], Icosφ control algorithm[16] and simulation study of EPLL-based control has been reported for power factor correction in single phase ac system[17].These control algorithms require ten feedback sensors whereas proposed unit-template control algorithm requires five feedback sensors. Kasal et al [18] proposed voltage and frequency controller for isolated asynchronous generators feeding three-phase four-wire loads using reduced feedback sensors.

In this paper, a unit-template control algorithm is proposed for the control of a four-leg VSC based DSTATCOM for Power Factor Correction (PFC) and Zero Voltage Regulation (ZVR) modes of operation. During PFC and ZVR modes of proposed algorithm PQ problems such as elimination of harmonics, load balancing, and unity power factor at source, reactive power control and neutral current compensation are mitigated [19]. The proposed algorithm reduces the number of feedback sensors which reduces cost of DSTATCOM. The four-leg VSC based DSTATCOM is used for neutral current compensation which eliminates transformer connection at PCC. The computer simulation results of unit-template control algorithm for four-leg VSC based DSTATCOM are validated under MATLAB environment using Simulink and Simpower System (SPS) toolboxes.

II. SYSTEM CONFIGURATION AND PRINCIPLE OF OPERATION

The schematic diagram of four-leg VSC based DSTATCOM feeding three-phase four-wire linear/non-linear load along with unit-template control algorithm is shown in Fig.1.The distribution system linear loads consist of three- phase star-connected resistive load and non-linear loads consist of three single-phase diode bridge rectifiers with R-C load. These non-linear loads in the distribution system will create PQ problems at the source without DSTATCOM. To mitigate PQ problems a DSTATCOM is connected at Point of Common Coupling (PCC). The proposed DSTATCOM consists of four-leg IGBT based voltage source converter (VSC), four interface inductors and a dc bus capacitor. The four-leg VSC based DSTATCOM will inject compensating currents (i_{ca}, i_{cb}, i_{cc}) in such a way that source current (i_{sa}, i_{sb}, i_{sc}) is pure sinusoidal and maintains unity power factor at source. A ripple of Resistance (R_f) and Capacitor (C_f) is connected at PCC to filter voltage harmonics at three phase source voltages (v_{sa}, v_{sb}, v_{sc}).

III. PROPOSED UNIT-TEMPLATE CONTROL ALGORITHM

The performance of DSTATCOM depends upon quick and accurate extraction of fundamental of source current harmonic components. All basic control algorithms of custom power devices require ten feedback sensors whereas proposed control algorithm requires only five feedback sensors. The basic control algorithms require three feedback

The paper first received 13 February 2015 and in revised form 08 April 2017.
Digital Ref: APEJ-2015-02-0461

[1]**Department of Electrical Engineering, B V Raju Institute of Technology, Narsapur, Medak(Dist),Telangana,India,Pin-502313.**
E-mail: rajujbr@gmail.com
[2]**Department of Electrical Engineering, Stanley College of Engineering and Technology for Women, Abids, Hyderabad, Telangana, India,Pin-500001.**
E-mail: rajsarang@gmail.com
[3]**Department of Electrical Engineering, Jawaharlal Nehru Technical University College of Engineering, Kukatpally, Hyderabad, Telangana, India,Pin-500085 E-mail: aj11994@gmail.com**

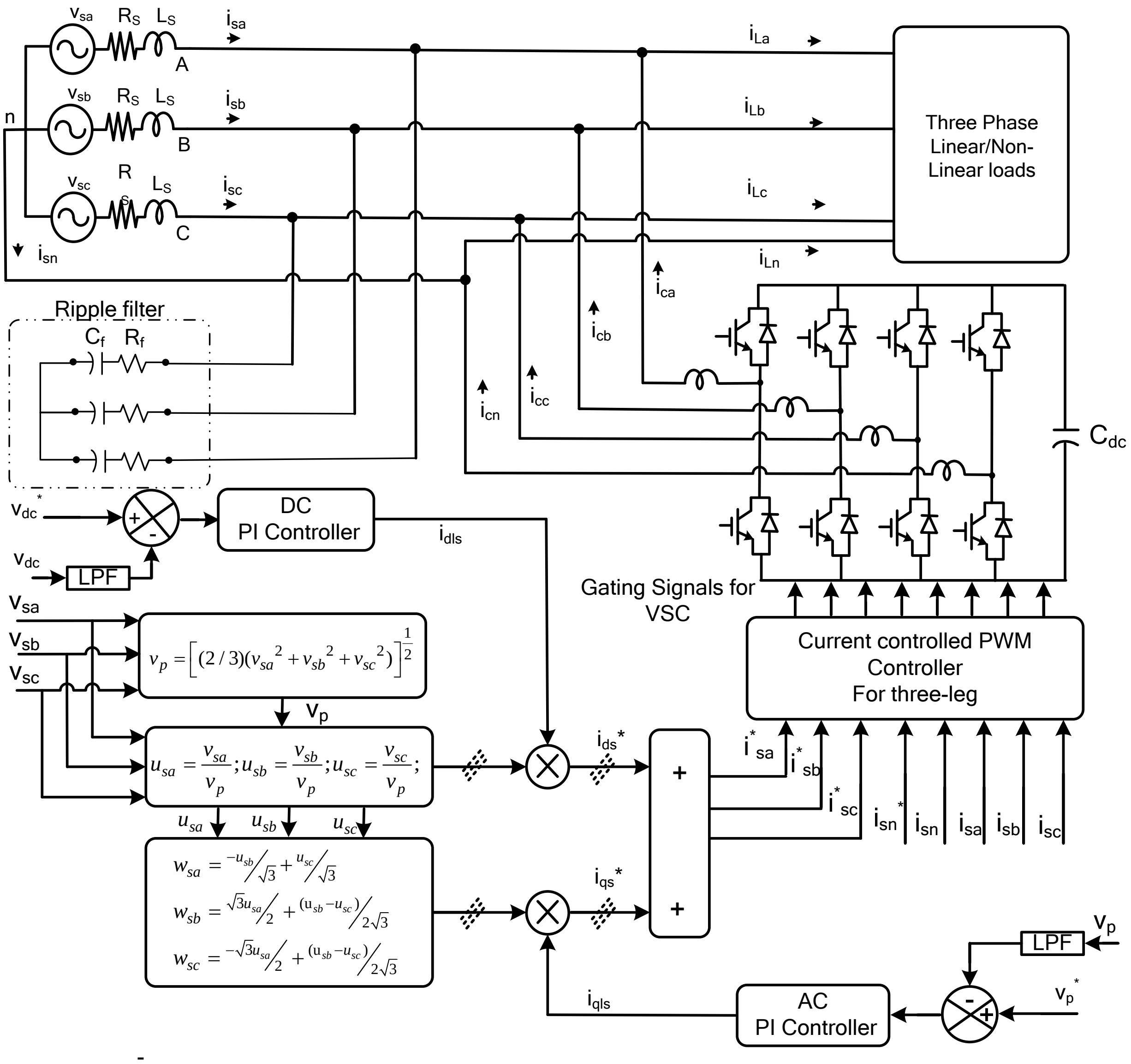

Fig.1Unit-template control algorithm of four-leg VSC based DSTATCOM

sensors for load currents, three feedback sensors for source voltages, one feedback sensor for dc bus voltage and three feedback sensors for source currents. The unit-template control algorithm requires two feedback sensors for source voltages (v_{sa}, v_{sb}), one feedback sensor for dc bus voltage (v_{dc}) , two feedback sensors for source currents(i_{sa},i_{sb}) and the third phase voltage v_{sc}(-(v_{sa}+v_{sb})) & current i_{sc}(-(i_{sa}+i_{sb})).The main feature of unit template control algorithm is to reduce number of feedback sensors which will improve performance of DSTATCOM. The proposed unit-template control algorithm based DSTATCOM is the effective solution to mitigate harmonics, power factor correction, load unbalancing, reactive power control and neutral current compensation.

The supply voltages (v_{sa}, v_{sb}, v_{sc}) of three-phase system can be represented as

$$v_{sa} = v_{mp}\sin(wt) \tag{1}$$

$$v_{sb} = v_{mp}\sin(wt - 120^o) \tag{2}$$

$$v_{sc} = v_{mp}\sin(wt - 240^o) \tag{3}$$

The magnitude of three phase voltages (v_{sa}, v_{sb}, v_{sc}) at PCC is given by

$$v_p = \sqrt{\frac{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}} \tag{4}$$

A. Power Factor Correction operation of Unit Template based DSTATCOM

The in-phase component of unit templates (u_{sa},u_{sb},u_{sc}) are calculated from (v_{sa},v_{sb},v_{sc}) which are given by

$$u_{sa} = \frac{v_{sa}}{v_p}; u_{sb} = \frac{v_{sb}}{v_p}; u_{sc} = \frac{v_{sc}}{v_p}; \quad (5)$$

The dc bus voltage error (v_{edc}) is the difference between reference dc bus voltage (v_{dc}^*) and sensed dc bus voltage (v_{dc}) under PFC mode. This dc voltage error is given to dc bus Proportional Integral (PI) controller and its output of PI is considered as active component of current loss (i_{dls}).

$$i_{dls(k)} = i_{dls(k-1)} + K_{dp}(v_{edc(k)} - v_{edc(k-1)}) + K_{di} v_{edc(k)} \quad (6)$$

where K_{dp} and K_{di} are proportional and integral gain constants of DC bus PI controller.

The reference active component source currents (i_{dsa}^*,i_{dsb}^*,i_{dsc}^*) are determined as

$$i_{dsa}^* = u_{sa} i_{dls}; i_{dsb}^* = u_{sb} i_{dls}; i_{dsc}^* = u_{sc} i_{dls}; \quad (7)$$

B. Zero Voltage Regulation operation of Unit Template based DSTATCOM

The quadrature phase component of unit templates (w_{sa},w_{sb},w_{sc}) are calculated from (u_{sa}, u_{sb}, u_{sc}) which are given by

$$w_{sa} = \frac{(-u_{sb} + u_{sc})}{\sqrt{3}}; \quad (8)$$

$$w_{sb} = \frac{(\sqrt{3}u_{sb} + u_{sb} - u_{sc})}{2\sqrt{3}}; \quad (9)$$

$$w_{sc} = \frac{(-3u_{sa} + u_{sb} - u_{sc})}{2\sqrt{3}}; \quad (10)$$

The ac bus voltage error (v_{ep}) is the difference between reference ac bus voltage (v_p^*) and sensed ac bus voltage at PCC (v_p) under ZVR mode. This ac voltage error is given to ac bus Proportional Integral (PI) controller and its output of PI is considered as reactive component of current loss (i_{qls}).

$$i_{qls(k)} = i_{qls(k-1)} + K_{qp}(v_{ep(k)} - v_{ep(k-1)}) + K_{qi} v_{ep(k)} \quad (11)$$

where K_{qp} and K_{qi} are proportional and integral gain constants of AC bus PI controller.

The reference reactive component source currents (i_{qsa}^*,i_{qsb}^*,i_{qsc}^*) are determined as

$$i_{qsa}^* = w_{sa} i_{qls}; i_{qsb}^* = w_{sb} i_{dls}; i_{qsc}^* = w_{sc} i_{qls}; \quad (12)$$

C. *Generation of Reference source currents*

The total reference source currents (i_{sa}^*,i_{sb}^*,i_{sc}^*) are the sum of the reference in-phase source current (i_{dsa}^*,i_{dsb}^*,i_{dsc}^*) and reference quadrature source currents(i_{qsa}^*,i_{qsb}^*,i_{qsc}^*)are

$$i_{sa}^* = i_{dsa}^* + i_{qsa}^* \quad (13)$$

$$i_{sb}^* = i_{dsb}^* + i_{qsb}^* \quad (14)$$

$$i_{sc}^* = i_{dsc}^* + i_{qsc}^* \quad (15)$$

D. Current Controlled PWM Generator

In a current controlled PWM Generator, the difference between reference source currents (i_{sa}^*, i_{sb}^*, i_{sc}^*) and sensed source currents (i_{sa}, i_{sb}, i_{sc}) are taken as error source currents in each of the three phases. In addition to error source currents in three phases, the source neutral currents(i_{sn}) are compared with triangular waveform to generate switching pulses for four-leg VSC based DSTATCOM.

IV. Results and Discussion

MATLAB/SIMULINK is used for development of proposed DSTATCOM and results are carried out with ode23tb solver (stiff/TR-BDF-2) in discrete mode at fixed step size of 4×10^{-6}.The performance of unit-template control algorithm based DSTATCOM is simulated in PFC and ZVR modes of operation at three phase time-varying linear/nonlinear loads.

A. Performance of unit template control algorithm

Fig.2shows the various intermediate signals of unit template control algorithm which include three phase source voltage (v_s), three phase load current (i_L), three phase reference source current (i_s^*), reference active component source currents (i_{dsa}), reference reactive component source currents (i_{qsa}), active component of current loss (i_{dls}), reactive component of current loss (i_{qls}), DC bus voltage error (v_{edc}), AC bus voltage error (v_{ep}) and three phase sensed source (i_s) respectively. The waveforms of unit template control algorithm shows that fast and accurate extraction of control signals occurs at three phase non-linear loads in ZVR mode.

B. Performance of DSTATCOM in PFC Mode

The performance of four-leg VSC based DSTATCOM for PFC mode with three phase linear load is shown in Fig.3.The dynamic performance of DSTATCOM is analyzed on the basis of three phase source voltages (v_s), three phase source currents (i_s), three phase load currents (i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents (i_c), load neutral current (i_{Ln}), source neutral current (i_{sn}), sensed dc link voltage (v_{dc}) & reference dc link voltage (v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC (v_p*) are shown in Fig.3 under a time varying load at t=0.62sec to 0.78 sec condition. The waveforms show that satisfactory operation of DSTATCOM in PFC mode operation under linear loads.

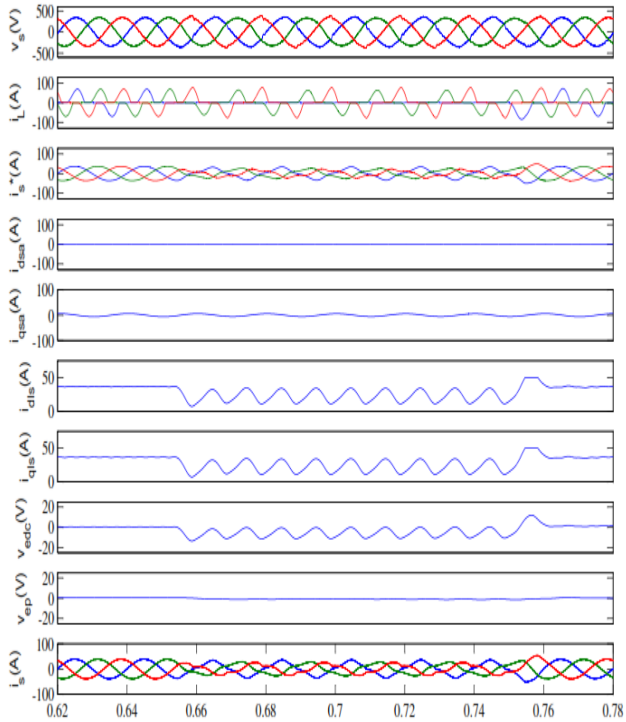

Fig. 2.Various intermediate signals of unit template control algorithm

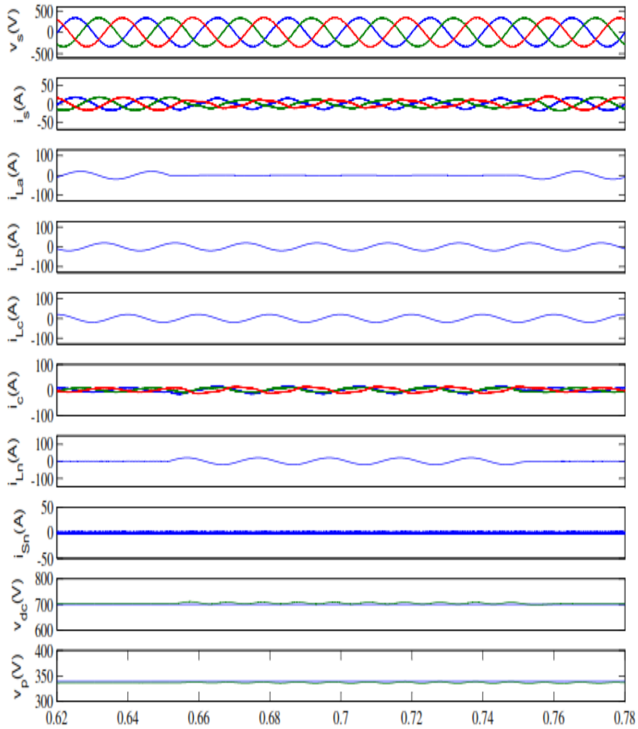

Fig. 3.Dynamic performance of DSTATCOM under linear loads in PFC mode

Similarly the performance of four-leg VSC based DSTATCOM for PFC mode with three phase non-linear loads/(diode bridge rectifier with parallel connected resistive and capacitive load) considered in the distribution system is shown in Fig.4. The waveforms of three phase source voltages (v_s), three phase source current (i_s), three phase load currents(i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents (i_c), load neutral current (i_{Ln}), source neutral current (i_{sn}), sensed dc link voltage(v_{dc}) & reference dc link voltage(v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC(v_p*) are shown in Fig.4. The harmonic spectra waveforms of phase 'a' source voltage(v_{sa}), source current (i_{sa}) and load current harmonic(i_{La}) with three phase non-linear R-C loads are shown in Fig.5(a)-5(c).The waveforms shows that the %THD of phase 'a' load current (i_{La}) is 70.74% whereas %THD of source voltage(v_{sa}) and source current(i_{sa}) are 2.23%,4.96% respectively. The performance results of DSTATCOM in PFC modes operation are shown in Table.1. It is observed that the proposed DSTATCOM shows give satisfactory results in PFC mode operations under non-linear loads.

C. Performance of DSTATCOM in ZVR Mode

In ZVR modes operation, the amplitude of reference terminal voltage at PCC is regulated to the reference terminal voltage by injecting extra reactive power. The dynamic performance of DSTATCOM is analyzed on the basis of three phase source voltages(v_s), three phase source current (i_s),three phase load currents(i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents(i_c), load neutral current (i_{Ln}), source

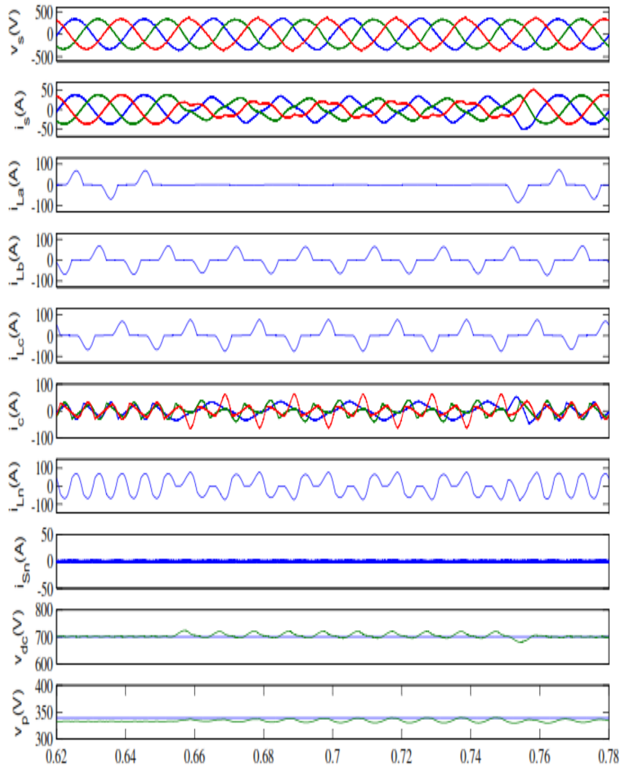

Fig.4 Dynamic performance of DSTATCOM under non-linear loads in PFC mode

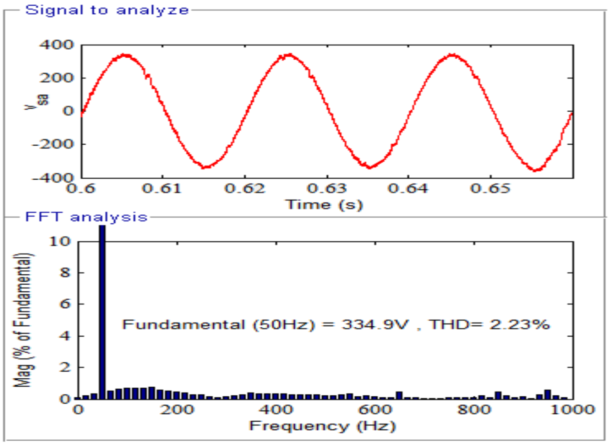

Fig. 5(a) Harmonic Spectrum of phase ‘a’ source voltage in PFC mode

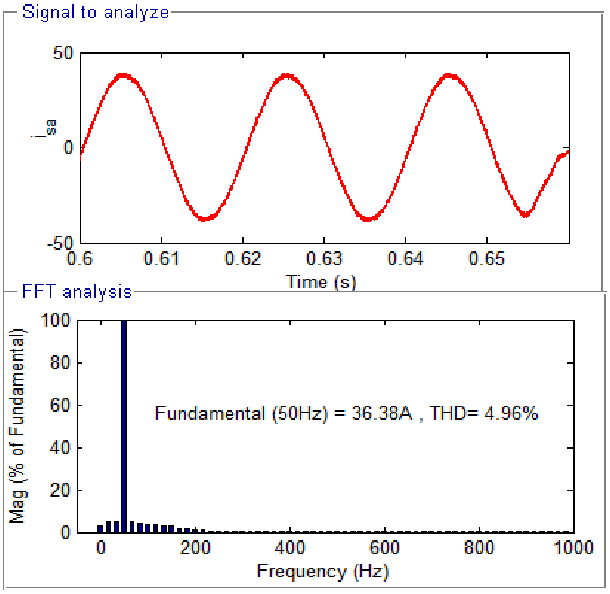

Fig. 5(b) Harmonic Spectrum of phase ‘a’ source current in PFC mode

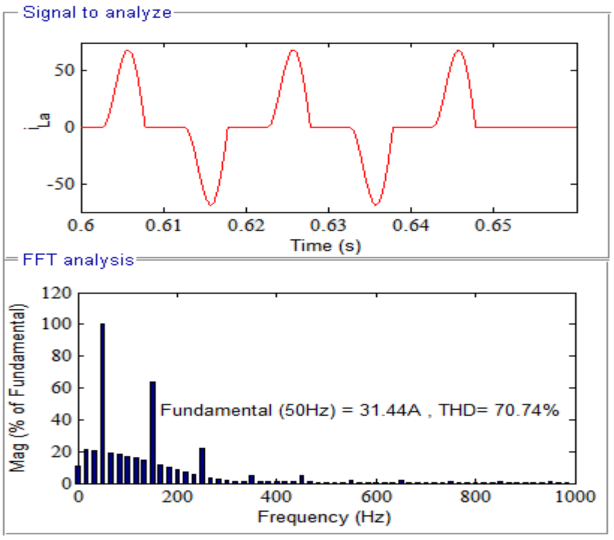

Fig. 5(c) Harmonic Spectrum of phase ‘a’ load current in PFC mode

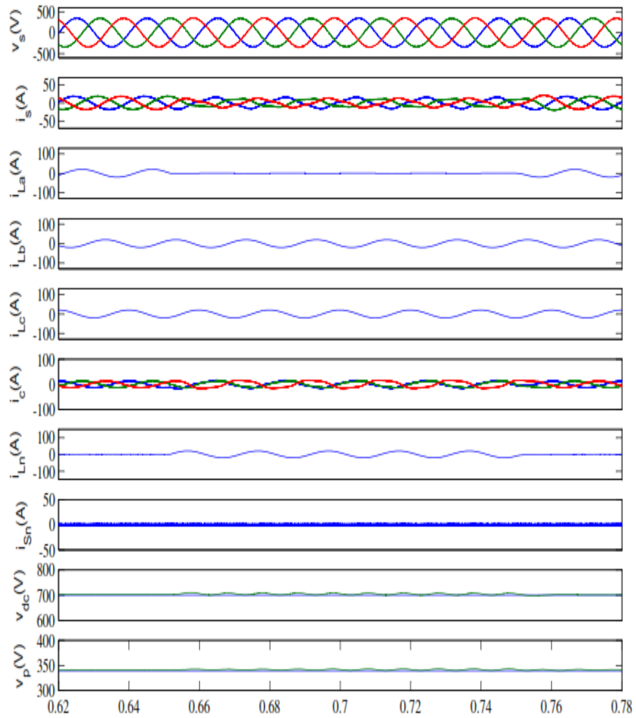

Fig.6.Dynamic performance of DSTATCOM under linear loads in ZVR mode

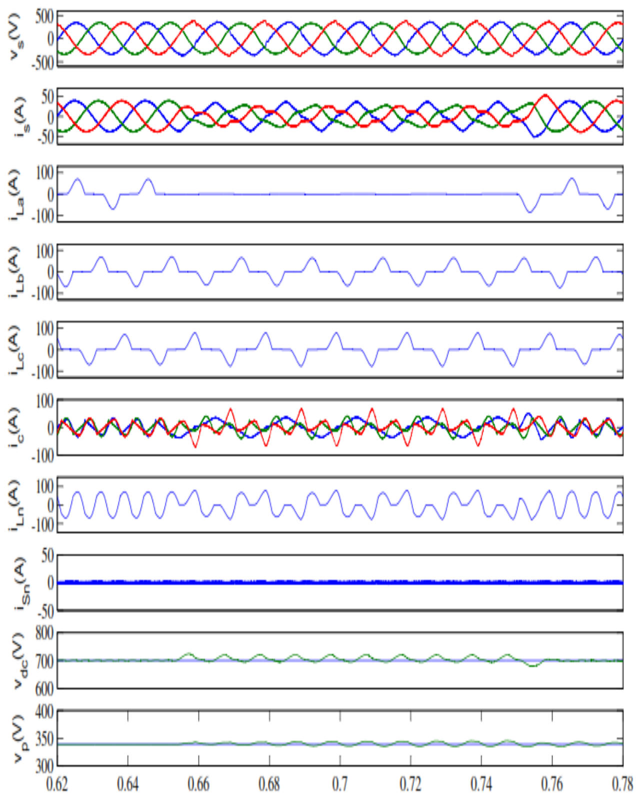

Fig.7.Dynamic performance of DSTATCOM under non-linear loads in ZVR mode

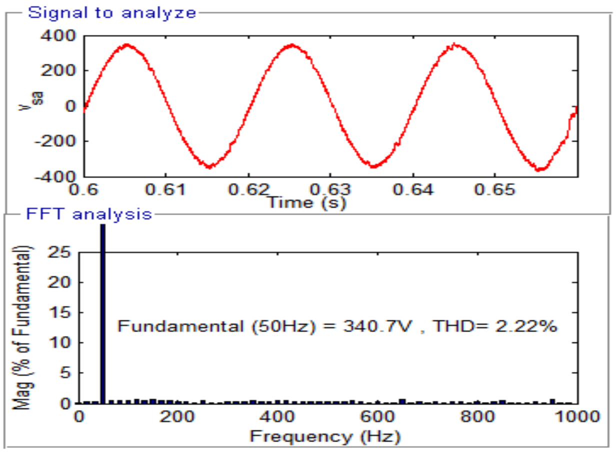

Fig.8(a) Harmonic Spectrum of phase ‘a’ source voltage in ZVR mode

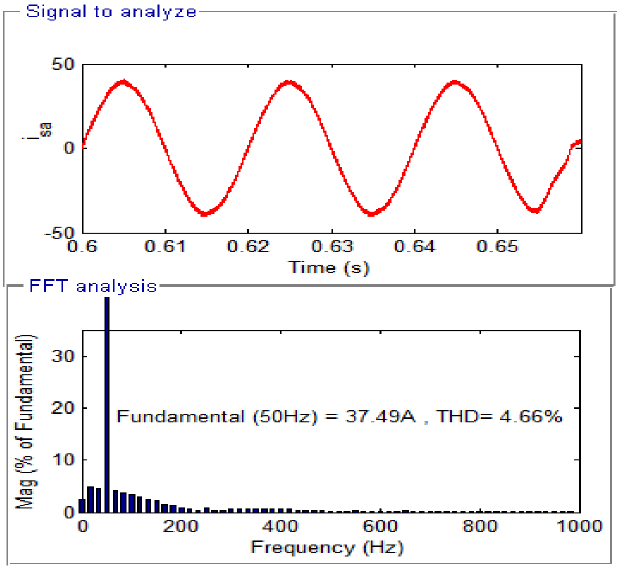

Fig. 8(b) Harmonic Spectrum of phase ‘a’ source current in ZVR mode

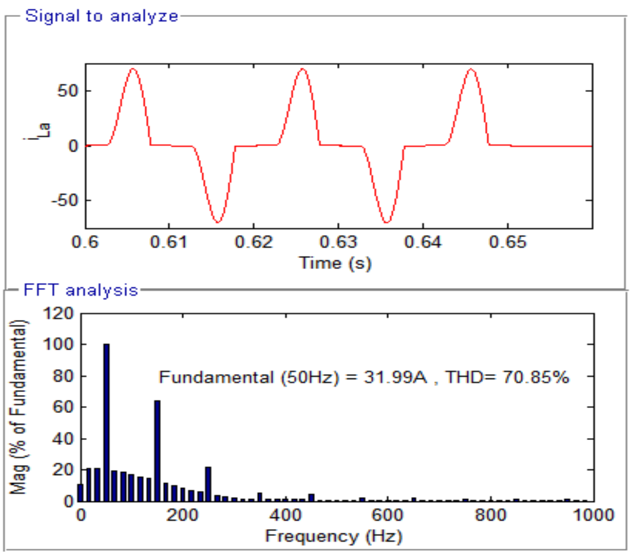

Fig. 8(c) Harmonic Spectrum of phase ‘a’ load current in ZVR mode

neutral current (i_{sn}), sensed dc link voltage (v_{dc}) & reference dc link voltage (v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC(v_p*) are shown in Fig.6 under a time varying load at t=0.62sec to 0.78 sec conditions. The waveforms show that satisfactory operation of DSTATCOM in ZVR mode operation under three phase linear loads.

The performance of four-leg VSC based DSTATCOM for PFC mode with three phase non-linear load is shown in Fig.7. The waveforms of three phase source voltages (v_s), three phase source current (i_s), three phase load currents (i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents(i_c), load neutral current (i_{Ln}), source neutral current(i_{sn}), sensed dc link voltage(v_{dc}) &reference dc link voltage(v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC(v_p*) are shown in Fig.7.The harmonic spectra waveforms of phase ‘a’ source voltage (v_{sa}) ,source current(i_{sa}) and load current harmonic(i_{La}) are shown in Fig.8(a)-8(c).The waveforms shows that the %THD of phase ‘a’ load current (i_{La}) is 70.85% whereas %THD ofsource voltage (v_{sa}) and source current (i_{sa}) are 2.22%, 4.66% respectively. The performance results of DSTATCOM in ZVR modes operation are shown in Table.1. It is observed that the proposed DSTATCOM shows give satisfactory results in ZVR mode operations under three phase non-linear loads. The DSTATCOM is able to regulate reference terminal voltage at PCC of 339V.

Table.1.Performance of DSTATCOM at PFC and ZVR modes of operations

Operating Mode	Performance Parameters	Non-Linear R-C Load
PFC Mode	Source voltage(v_{sa}), %THD	334.9V, 2.23%
	Source current (i_{sa}), %THD	36.38A, 4.96%
	Load current (i_{La}), %THD	31.44A, 70.74%
ZVR Mode	Source voltage(v_{sa}), %THD	340.7V, 2.22%
	Source current (i_{sa}), %THD	37.49A, 4.66%
	Load current (i_{La}), %THD	31.99A, 70.85%

V. CONCLUSION

The proposed unit template control algorithm for four-leg VSC based DSTATCOM has been found to provide acceptable characteristics in PFC and ZVR modes of operation. During the PFC and ZVR modes of operations, the dynamic performance of DSTATCOM shows satisfactory results for harmonic elimination, reactive power control, load balancing, and neutral current compensation under linear and non-linear loads. The DC link voltage and terminal voltage at PCC of proposed DSTATCOM has been also regulated without overshoot to reference value under various load conditions. It is observed that the %THD of source current and source voltage is within IEEE519 standard.

APPENDIX

Three phase supply voltage=415V, 50Hz.
Supply Impedance: R_s=0.05Ω, L_s=5mH
Loads: Linear Loads R=15Ω and L=25mH
Non-Linear R-C Loads: three single phase diode bridge rectifier with R=15Ω and C=500μF
DC bus Capacitor C_{dc}=3000 μF
PWM switching frequency f_s=10 KHz
DC bus PI Controller: K_{dp}=2.36 K_{di}=4.1
AC bus PI Controller: K_{qp}=1.02 K_{qi}=2.41

REFERENCES

[1] R. C. Dugan, M. F. Mc Granaghan and H. W. Beaty, Electric Power Systems Quality, 2ed Edition, McGraw Hill, New York, 2006.
[2] T. A. Short, Distribution Reliability And Power Quality,CRC Press,New York, 2006.
[3] C. PredragPejovi, Three-Phase Diode Rectifiers with Low Harmonics Current Injection Methods, Springer Verlag, London, 2007.
[4] Angelo Baggini, Handbook on Power Quality,John Wiley and Sons,New Jersey, 2008.
[5] SurajitChattopadhyay,MadhuchhandaMitra and SamarjitSengupta, Electric Power Quality, Springer Verlag, London, 2011.
[6] IEEE Recommended Practices and Requirements for Harmonics Control in Electrical Power Systems, IEEE Std.519, 1992.
[7] T. Narongrit, K. L. Areerak and K. N. Areerak,"The comparison study of current control techniques for active power filters," Journal of World Academy of Science, Engg. & Technology, vol. 60 ,pp. 471-476, 2011
[8] Bhim Singh and JitendraSolanki,"A comparison of control algorithms for DSTATCOM,"IEEE Transactions on Industrial Electronics, vol. 56, no. 7, pp. 2738-2745, July 2009.
[9] A. Terciyanli, T. Avci, I. Yilmaz, C. Ermis, K. Kose, A. Acik, A. Kalay-cioglu, Y. Akkaya, I. Cadirci, and M. Ermis, "A current source converter based active power filter for mitigation of harmonics at the interface of distribution and transmission systems," IEEE Trans. Ind. Appl., vol. 48, no. 4, pp. 1374–1386, Jul./Aug. 2012.
[10] Bhimsingh, Jayaprakash, P., and Kothari, D.P.: "A T-Connected Transformer and Three leg VSC based DSTATCOM for Power Quality Improvement,"IEEE Trans. on Power Electronics, 2008, vol.23,no.6, pp.2710-2718.
[11] S. Rahmani, N. Mendalek and K. Al-Haddad,"Experimental design of a nonlinear control technique for three-phase shunt active power filter," IEEE Transactions on Industrial Electronics, vol. 57, no.10, pp.33643375,Oct.2010.
[12] Claudionor Francisco do Nascimento, Azauri Albano de Oliveira Jr, Alessandro Goedtel, Paulo Jose and Amaral Serni,"Harmonic identification using parallel neural networks in single-phase systems," Journal of Applied Soft Computing, vol. 11, pp. 2178-2185, 2011.
[13] Alejandro Garces, Marta Molinas and Pedro Rodriguez,"A generalized compensation theory for active filters based on mathematical optimization in ABC frame,"Journal of Electric Power Systems Research, vol. 90, pp. 1-10, 2012.
[14] R. Bayer and M. Brejcha, "Simple adaptive control for a single phase shunt active filter," in Proc. of International Conference on Applied Electronics, 2011, pp. 1-4.
[15] R.Zahira and A. Peer Fathima,"A technical survey on control strategies of active filter for harmonic suppression,"in Proc. of International Conference on Communication Technology and System Design, 2011,pp.686-693.
[16] G. Bhuvaneswari and M.G. Nair, "Design, Simulation, and Analog Circuit Implementation of a Three-Phase Shunt Active Filter Using the IcosΦ Algorithm," IEEE Trans. Power Delivery, Vol. 23, No. 2, pp. 1222–1235,Apr.2008.
[17] M. K. Ghartemani, H. Mokhtari, M. R. Iravani, and M. Sedighy, "A signal processing system for extraction of harmonics and reactive current of single-phase systems," IEEE Trans. Power Delivery, vol. 19, no. 3,pp. 979–986, Jul. 2004.
[18] Kasal, G.K., Singh, B.: 'Decoupled voltage and frequency controller for isolated asynchronous generators feeding three-phase four-wire loads', IEEE Trans. Power Delivery., vol.23, no.2, pp. 966–973,Mar.2008.
[19] Bhimsingh and V.Rajagopal, "Design of a Star-Hexagon Transformer Based Electronic Load Controller for Isolated Pico Hydro Generating System," in Proc of Third International Conference on Power Systems, 2009, pp. 1-6.

BIOGRAPHIES

.

J.Bangarraju was born in Tanuku, India,in 1982.He received the B.Tech. degree in Electrical and Electronics Engineering from A.S.R College of Engineering, Tanuku in 2004 and the M.Tech degree from JNTU, Hyderabad in 2007. Presently working as Associate Professor in B V Raju Institute of Technology, Narsapur, Telangana, India. His area of interest includes power electronics and drives, power quality, FACTS and Artificial neural networks. He is currently working towards Ph D degree at the Department of Electrical Engineering, JNTU Hyderabad, India. He is a life member of the Indian Society for Technical Education (ISTE) and Member of the Institute of Electrical and Electronics Engineers (IEEE).

V.Rajagopal was born in Kazipet, Warangal, India in 1969. He received the AMIE (Electrical) degree from The Institution of Engineers (India), in 1999, M.Tech. Degree from the Uttar Pradesh Technical University India in 2004 and Ph D degree in Indian Institute of Technology (IIT) Delhi India , in 2012. Presently working as Professor and HOD in Stanley College of Engineering and Technology for Women, Hyderabad, Telangana, India. His area of interest includes power electronics and drives, renewable energy generation and applications, FACTS, and power quality. He is a life member of the Indian Society for Technical Education (ISTE) and the Institution of Engineers (India) (IE (I)) and a Member of the Institute of Electrical and Electronics Engineers (IEEE).

A. Jaya Laxmi was born in Mahaboob Nagar District, Andhra Pradesh, on 07-11-1969. She completed her B.Tech. (EEE) from Osmania University College of Engineering, Hyderabad in 1991, M. Tech.(Power Systems) from REC Warangal, Andhra Pradesh in 1996 and completed Ph.D.(Power Quality) from Jawaharlal Nehru Technological University, Hyderabad in 2007. She has five years of Industrial experience and 14 years of teaching experience. Presently, working as Professor, Electrical & Electronics Engg., and Coordinator, Centre for Energy Studies, JNTUH College of Engineering, Jawaharlal Nehru Technological University Hyderabad, Kukatpally, and Hyderabad. She has 45 International Journals to her credit and also has 100 International and National papers published in various conferences held at India and also abroad. Her research interests are Neural Networks, Power Systems & Power Quality. She was awarded "Best Technical Paper Award" in Electrical Engineering from Institution of Electrical Engineers in the year 2006. Dr. A. Jaya laxmi is a Member of IEEE, Member of International Accreditation Organization (M.I.A.O), Fellow of Institution of Electrical Engineers Calcutta (F.I.E), Life Member of System Society of India

(M.S.S.I), Life Member of Indian Society of Technical Education (M.I.S.T.E), Life Member of Electronics & Telecommunication Engineering (M.I.E.T.E), Life Member of Indian Science Congress (M.I.S.C)