Design of Embedded Controller for Various Multilevel Inverter Topologies

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***Abstract*– Multilevel inverter technology is an emerging trend for the control of electric drives in hybrid electric vehicles of high power rating. This paper proposes three different types of multilevel inverter topologies they are five level flying capacitor multilevel inverter, six switch hybrid multilevel inverter and five switch hybrid multilevel inverter. This paper analyses the total harmonic distortion of the chosen three types of multilevel inverter topologies. Embedded switching pattern scheme is used to improve the performance of Multilevel Inverter. For this type of inverters pulses are developed by using the embedded controller. This scheme reduces the switching loss. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. To validate the developed technique simulations are carried out through MATLAB/SIMULINK.**

Keywords– THD, FCMLI, CMLI, Embedded controller

I. INTRODUCTION

Multilevel inverters (MLI) are plays an important role in industrial power applications. Generally conventional MLIs are categorized into diode clamped, flying capacitor and Cascaded H bridge type. Conventional inverters can either produce the output levels as zero or maximum. So it is called a two level inverter. For a high power application, these types of inverters are not used. Because of it consists of losses with ripple content, frequency deviations, switching losses and device ratings. Multilevel Inverters are tremendously interest to use in Power inverters. The basic concept of a multilevel inverter is to achieve high power by using a series of power semiconductor switches with several lower DC voltage sources to perform the power conversion by synthesizing a staircase voltage waveform. Embedded Controllers (ECs) are often found in low power embedded reference designs, performing a range of input/output and system management functions. Embedded controller is a special purpose controller that is embedded in an electronic system. Embedded controllers has major role in modern machine and automobile than power control systems. Embedded controllers are often the heart of an industrial control system or a process control application. Krishna Kumar et al [1] proposed a multilevel inverter topology with input DC sources which are connected in opposite polarities with one another through power switches. This approach results in reduced number of power switches as compared to classical topologies. K.Gobinath et al [2] developed a novel cascaded multilevel inverter for harmonic elimination. Jacob James Nedumgatt et al [3] discussed a new topology of a cascaded multilevel inverter that utilizes less number of switches than the conventional topology.

The paper first received 8 Apr. 2014 and in revised form 18 Aug. 2015.
Digital Ref: APEJ-2014-08-0446

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Javad Ebrahimi et al [4] suggested a topology which reduces the number of DC voltage sources, switches as the number of output voltage levels increases. Ehsan Najafi et al [5] presented a new topology with a reversing voltage component is proposed to improve the multilevel performance. Roshankumar et al [6] developed a topology which is obtained by cascading a three-level flying capacitor inverter with a flying H-bridge power cell in each phase. K.K. Gupta et al [7] developed a topology for multilevel inverters which increases the number of levels as number of switches and conduction losses can be reduced. Ahmed et al [8] presented two types of multilevel inverters with reduced number of switches, losses. G.S. Konstantinou et al [9] proposed a topology which is a cascaded connection of a conventional three phase, two level inverter. Arif Al-Judi et al [10] proposed a Cascaded Multilevel Inverter with reduced number of Switches. Tehrani et al [11] proposed a new multilevel inverter topology. Ceglia et al [12] suggested a new inverter topology using an auxiliary switch which reducing the number of power devices required to implement a multilevel output. Leon M et al [13] proposed a multilevel inverter using carrier based PWM methods. G.Carrara et al [14] developed a multilevel inverter based on PWM method. N.S.Choi et al [15] proposed multilevel inverter that can realize any pulse width modulation scheme which leads to harmonic reduction.

II. MULTILEVEL INVERTERS

A Multilevel inverter is a power electronic device built to synthesize a desired A.C voltage from several levels of DC voltages. Multilevel inverters have gained more attention in high power applications because it has got many advantages. It can realize high voltage and high power output by using semiconductor switches without the use of transformer and dynamic voltage balance circuits. The proposed scheme is simulated under the MATLAB/SIMULINK environment. Filter is not used at the output side so the THD (Total Harmonic Distortion) is more. If small size filter is used across the load the THD will be within the IEEE standard. The another way to reduce the THD is by increasing the number of levels of the inverter. The Powergui block allows you to choose one of the following methods to solve your circuit (i) Continuous, which uses a variable step solver from Simulink (ii) Ideal Switching continuous (iii) Discretization of the electrical system for a solution at fixed time steps and (iv)Phasor solution. The Powergui block is necessary for simulation of any Simulink model containing Sim Power Systems blocks. It is used to store the equivalent SIMULINK circuit that represents the state-space equations of the model. When using this block in a model, you must follow these rules: Place the Powergui block at the top level of diagram for optimal performance. You can place it anywhere inside subsystems for your convenience; its functionality will not be affected. You can have a maximum of one

Powergui block per model. You must name the block powergui. The Powergui block also gives you access to various Graphical User Interface (GUI) tools and functions for the steady-state analysis of Sim Power Systems models, the analysis of simulation results, and for the design of advanced block parameters. In this continuous block is chosen in the powergui block.

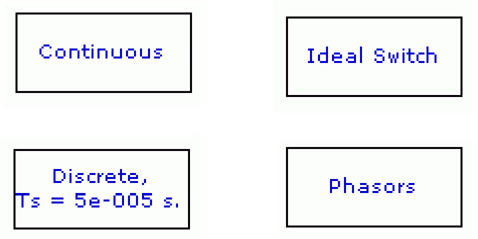

Fig. 1: Environment block for simpowersystems models (Powergui)

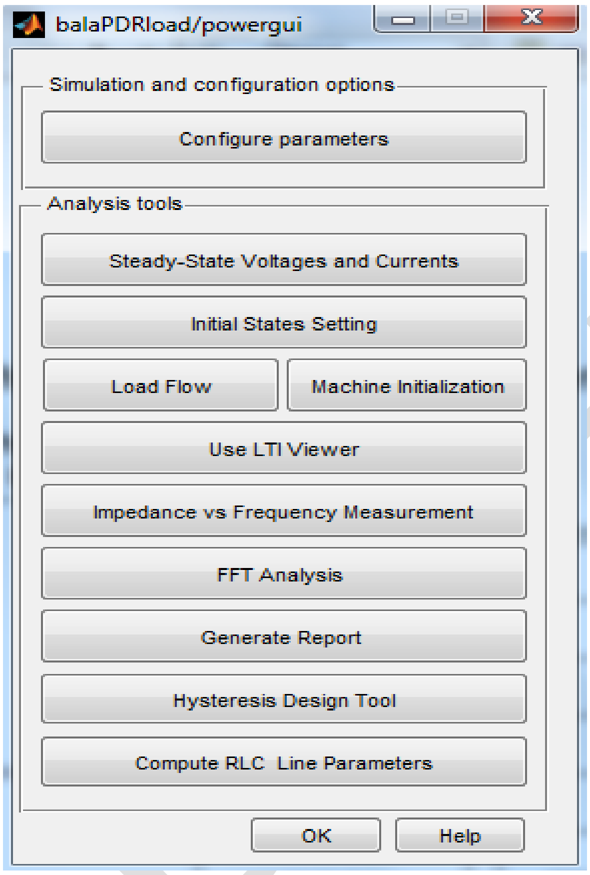

Fig. 2: Options available in the Powergui tool

A. Five Level Flying Capacitor Multilevel Inverter

The structure of this flying capacitor inverter is similar to that of the diode clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. The Flying Capacitor (FC)MLI topology has a ladder structure of DC side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. The main advantage of flying capacitor multilevel inverter is large amounts of storage capacitors can provide capabilities during power outages and also these inverters can provide switch combination redundancy for balancing different voltage levels. The input voltage value of this proposed system is V_{dc}=200 V and the load R=100ohms.

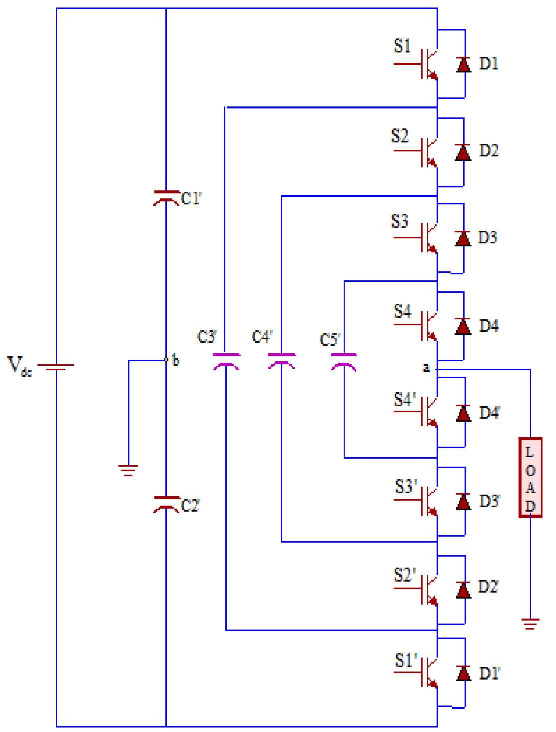

Fig.3: Half bridge five level flying capacitor inverter for R-phase

Fig.3 shows the general structure of half bridge five level flying capacitor inverter for R-phase. FCMLI requires 8 semiconductor switches (S1-S4, S1'-S4') 3 flying capacitors (C3', C4', C5') and 2 DC link capacitors (C1', C2'). This FCMLI consists of four switch pairs (S1,S1'), (S2,S2'), (S3,S3') and (S4,S4'). The switches are clamped by DC-link together with flying capacitors. The four switches (S1-S4) must be connected in series between DC input and load and likewise for switches (S4'-S1'). The three flying capacitors C3', C4' and C5' are charged to different voltage levels. By changing the transistor switching states, the capacitors and the DC source are connected in different ways to produce different load voltage levels. A typical switch combination used to synthesize the various load voltages are shown in Table 1.

This proposed five level flying capacitor multilevel inverter consists of eight switching devices. The switching states of the multilevel inverter are given as the input for the embedded controller based proposed system. This proposed system provides the five output level $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$. At the level of $2V_{dc}$, the first four switches should be turn ON and the remaining switches will be turned OFF. In the $+V_{dc}$ level P1, P2, P3, P5 switches will be turned ON. At the level of 0Vdc P1, P2, P5, P6 should be turned ON. The $-V_{dc}$ level contains P1, P5, P6, P7 will be turned ON. At the level of $-2V_{dc}$ the lower four switches should be turned ON. This proposed system used to obtain the five level output, which are nearer to the sinusoidal output. This proposed system is used to reduce the THD and it can be used to increase the performance of the system. It also can be used to reduce the switching losses. The schematic diagram of proposed method is shown in the Fig. 3.

Table 1 : Switching states of five-level flying capacitor multilevel inverter

S1	S2	S3	S4	C3’	C4’	C5’	V_{ab}
1	1	1	1	NC	NC	NC	$+V_{dc}/2$
1	1	1	0	NC	NC	+	$+V_{dc}/4$
1	1	0	1	NC	+	-	
1	0	1	1	+	-	NC	
0	1	1	1	-	NC	NC	
0	0	1	1	NC	-	NC	0
0	1	0	1	-	+	-	
0	1	1	0	-	NC	+	
1	0	0	1	+	NC	-	
1	0	1	0	+	-	+	
1	1	0	0	NC	+	NC	
1	0	0	0	+	NC	NC	$-V_{dc}/4$
0	1	0	0	-	+	NC	
0	0	1	0	NC	-	+	
0	0	0	1	NC	NC	-	
0	0	0	0	NC	NC	NC	$-V_{dc}/2$

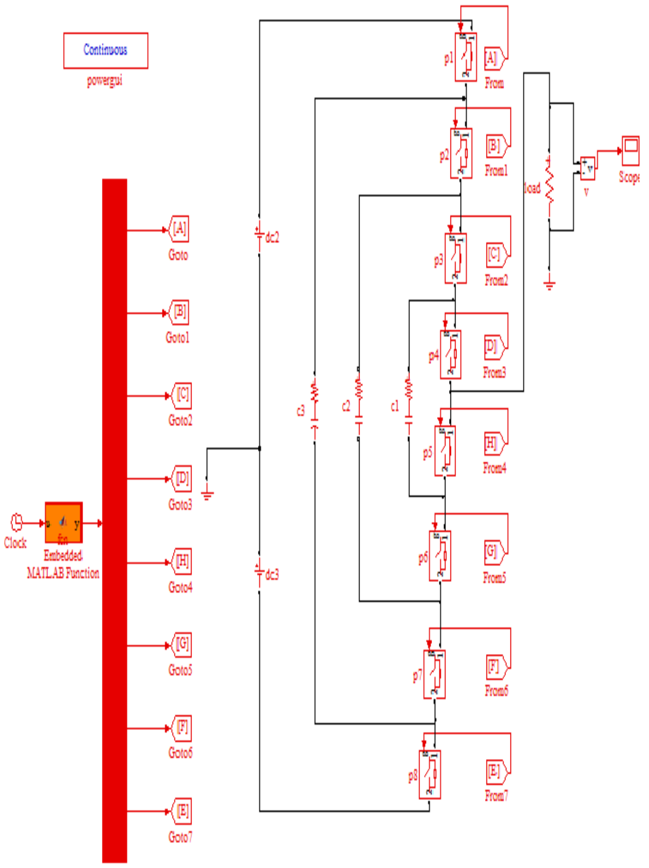

Fig. 4: Sample simulation circuit of five level flying capacitor multilevel inverter using R load

The above table 1 represents the switching states which are given as the input for the proposed five level flying capacitor multilevel inverter. By using the embedded controller the five level output can be obtained for this proposed system. The simulation output of the proposed system is shown in Figure 5. The THD which is a measure of closeness in shape between a waveform and its fundamental component. When the voltage levels of the topologies are increases, the harmonic content of the output voltage waveform decreases significantly.

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=2,3..}^{\infty} V_n^2} \tag{1}$$

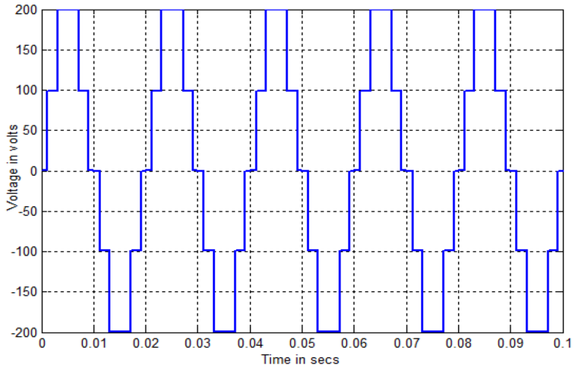

Fig. 5: Five level output voltage of FCMLI

The THD value for the proposed system is shown in Figure 6.

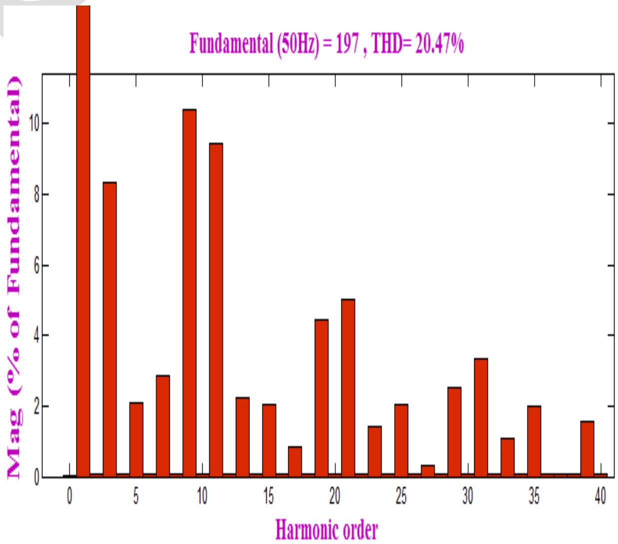

Fig. 6: FFT plot for five level output voltage

By seeing the truth table the coding are generated. This method of generation of pulses is similar to (Selective Harmonic Elimination) SHE PWM method. The coding are developed with the help of MATLAB software.

```
function y  = fcn(u)
 a = mod(u*1000,10);
b = mod(u*1000,20);
 if a<1.2 %0
    p1=1;
    p2=1;
    p3=0;
```

```
    p4=0;
    p5=1;
    p6=1;
    p7=0;
    p8=0;
elseif a<3.1 %3
    p1=1;
    p2=1;
    p3=1;
    p4=0;
    p5=1;
    p6=0;
    p7=0;
    p8=0;
 elseif a<7.2 %4
    p1=1;
    p2=1;
    p3=1;
    p4=1;
    p5=0;
    p6=0;
    p7=0;
    p8=0;
    elseif a<9.1 %5
    p1=1;
    p2=1;
    p3=1;
    p4=0;
    p5=1;
    p6=0;
    p7=0;
    p8=0;
   else %0
    p1=1;
    p2=1;
    p3=0;
    p4=0;
    p5=1;
    p6=1;
    p7=0;
    p8=0;
end
if b<10
y=[p1,p2,p3,p4,p5,p6,p7,p8];
else
y=[p5,p6,p7,p8,p1,p2,p3,p4];
end
```

B. Six Switch Hybrid Multilevel Inverter

The next proposed circuit is embedded controller based five level hybrid cascaded inverter with reduced number of switches is shown in Figure 7. Each separate voltage source V_{dc1}, V_{dc2}, V_{dc3} is connected in cascade with other sources via a special H-bridge circuit associated with it. The most important part in multilevel inverters is switches which define the reliability, circuit size, cost, installation area and control complexity. The first H-bridge circuit consists of four active switching elements and the second Voltage Source Inverter (VSI) circuit consists of two active switching elements that can make the output voltage either positive or negative polarity or it can also be simply zero volts which depends on the switching condition of switches in the circuit.

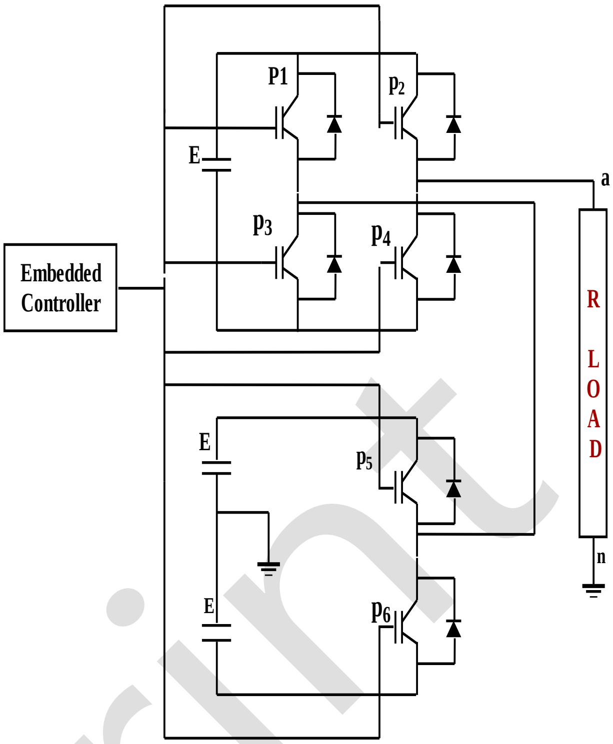

Fig. 7: Five level embedded controller based hybrid multilevel inverter

At the level of $2V_{dc}$, P2, P3, P5 switches should be turned ON. In the V_{dc} level P1, P2, P5 will be turned ON and the remaining switches will turned OFF. The $0V_{dc}$ level contains P2; P3 and P6 switches will be turned ON. At the level of $-V_{dc}$, P1, P2 and P6 switches will be turned ON and the $-2V_{dc}$ level contains P1, P4 and P6 switches should be turned ON. The advantages of cascaded multilevel inverter are modularized layout and packaging. This enables the manufacturing process to be done more quickly and cheaply. In this proposed system the switching states are given as the input by using the MATLAB/SIMULINK. The input voltage value of this proposed system is V_{dc}=200V and the load R=100ohms.

Table 2 : Switching states for five level proposed hybrid cascaded multilevel inverter

Switching states P_1	P_2	P_3	P_4	P_5	P_6	Output Voltage
0	1	1	0	1	0	$2V_{dc}$
1	1	0	0	1	0	V_{dc}
0	1	1	0	0	1	0
1	1	0	0	0	1	$-V_{dc}$
1	0	0	1	0	1	$-2V_{dc}$

The switching states of the proposed hybrid multilevel inverter are shown in Table 2. These switching states are given as the input and the proposed system produce the five levels of output. The simulation output of hybrid multilevel inverter is shown in Figure 8.

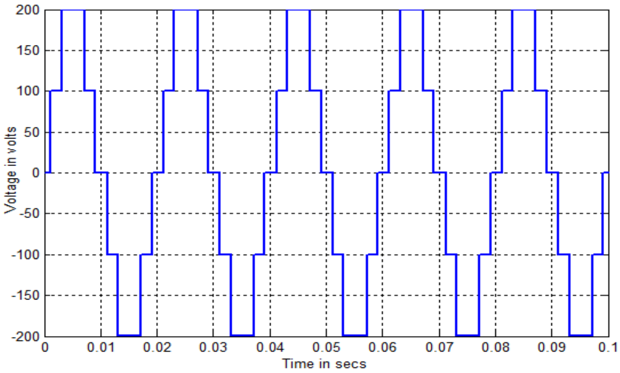

Fig. 8: Simulation output of proposed hybrid multilevel inverter

The total harmonic distortion of the proposed system is shown in Figure 9.

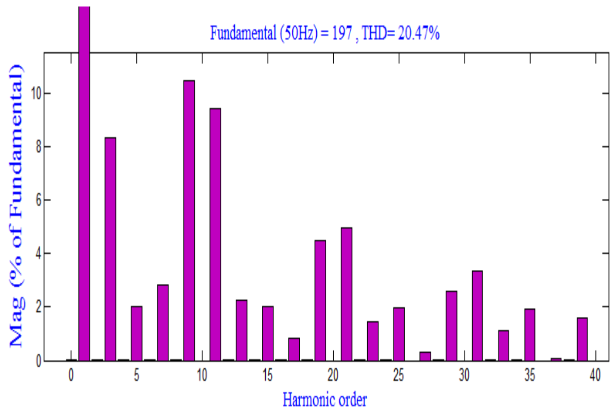

Fig. 9: THD plot for proposed hybrid multilevel inverter

The coding for six switch hybrid MLI is given below

```
function y  = fcn(u)
 a = mod(u*1000,10);
b = mod(u*1000,20);
if a<1.2 %0
    p1=0;
    p2=1;
    p3=1;
    p4=0;
    p5=0;
    p6=1;
elseif a<3.1 %1
    p1=1;
    p2=1;
    p3=0;
    p4=0;
    p5=1;
    p6=0;
 elseif a<7.2 %2
    p1=0;
    p2=1;
    p3=1;
    p4=0;
    p5=1;
    p6=0;
elseif a<9.1 %1
    p1=1;
    p2=1;
    p3=0;
    p4=0;
    p5=1;
    p6=0;
else  %0
     p1=0;
    p2=1;
    p3=1;
    p4=0;
    p5=0;
    p6=1;
 end
if b<10
y=[p2,p3,p5,p1,p4,p6];
else
y=[p1,p4,p6,p2,p3,p5];
end
```

C. Five Switch Hybrid Multilevel Inverter

The next proposed hybrid multilevel inverter is shown in figure 10. This type of proposed system contains five switches which produce the five levels of output by using the embedded controller based MATLAB/SIMULINK. The input voltage value of this proposed system is V_{dc}=200V and the load R=100ohms.

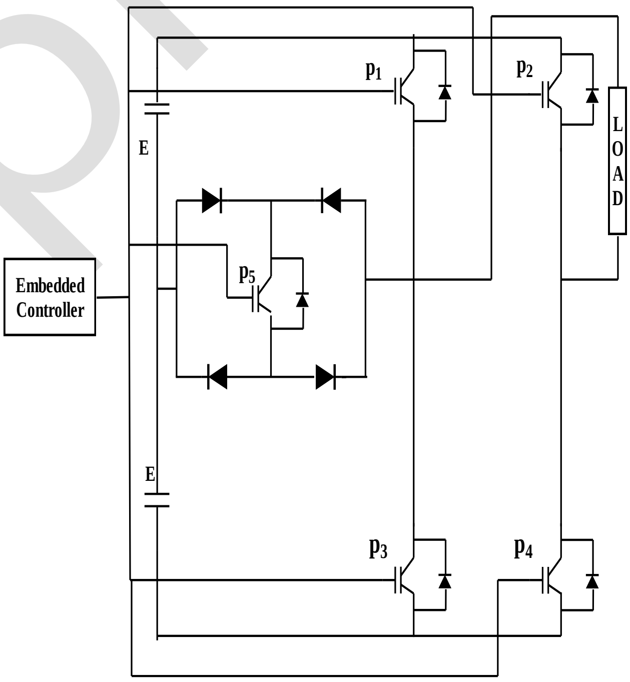

Fig. 10: Five level Embedded controller based hybrid multilevel inverter

This proposed system contains five switches which produce the desired five level output. At the level of $+2V_{dc}$, P1 and P4 switches should be turned ON and the remaining switches will be turned OFF. In the $+V_{dc}$ level P4 and P5 will be turned ON. The 0Vdc level contains P2 and P4 switches will be turned ON. At the level of $-V_{dc}$, P3 and P5 switches will be turned ON and the $-2V_{dc}$ level contains P2 and P3 switches should be turned ON. The switching states of the above proposed system are shown in Table 3.

Table 3: Switching states for embedded controller based hybrid multilevel inverter

Switching states					Output voltage
P_1	P_2	P_3	P_4	P_5	
1	0	0	1	0	$2V_{dc}$
0	0	0	1	1	V_{dc}
0	1	0	1	0	0
0	0	1	0	1	$-V_{dc}$
0	1	1	0	0	$-2V_{dc}$

By using these switching states the Hybrid MLI can produce five levels of output. The simulation output of the proposed system is shown in Figure 11.

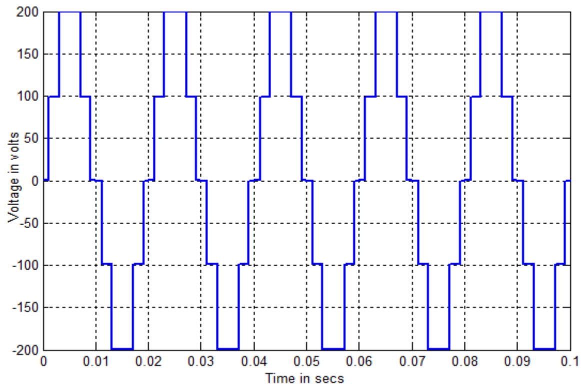

Fig. 11: Simulation output of embedded controller based hybrid multilevel inverter

The total harmonic distortion of the proposed five level hybrid multilevel inverter is shown in Figure 12.

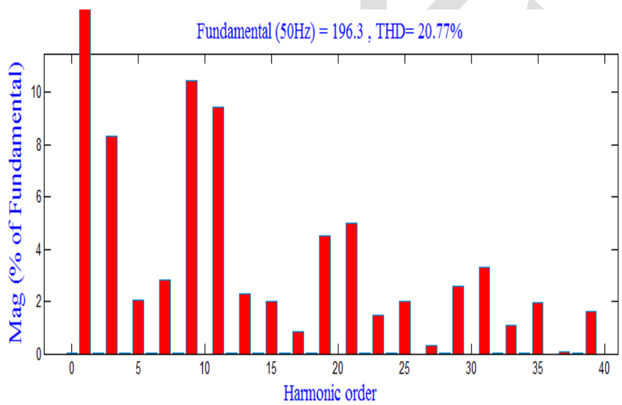

Fig. 12: THD plot for Embedded Controller based hybrid multilevel inverter

The program for the five switch MLI is given below

```
function y  = fcn(u)
a = mod(u*1000,10);
b = mod(u*1000,20);
if a<1.2 %0
    p1=0;
    p2=1;
    p3=0;
    p4=1;
    p5=0;
elseif a<3.1 %1
    p1=0;
    p2=0;
    p3=0;
    p4=1;
    p5=1;
 elseif a<7.2 %2
     p1=1;
    p2=0;
    p3=0;
    p4=1;
    p5=0;
 elseif a<9.1 %1
    p1=0;
    p2=0;
    p3=0;
    p4=1;
    p5=1;
  else %0
    p1=0;
    p2=1;
    p3=0;
    p4=1;
    p5=0;
end
if b<10
y=[p1,p4,p2,p3,p5];
else
y=[p2,p3,p1,p4,p5];
end
```

In a Direct Current (DC) circuit, voltage or current is simple to define, but in an Alternating Current (AC) circuit, the definition is more complicated, and can be done in several ways. Root Mean Square (RMS) refers to the most common mathematical method of defining the effective voltage or current of an AC wave. The number of pulses p per half cycle depends on the carrier frequency. By varying the modulation index m_a, the RMS output voltage can be varied. The area of each pulse corresponds approximately to the area under the sine wave between the adjacent midpoints of off periods on the gating signals. If δ_m is the width of the m^{th} pulse, the RMS output voltage can be expressed as follows:

$$V_{RMS} = V_{dc}\sqrt{\sum_{m=1}^{2p}\frac{\delta_m}{\pi}} \tag{2}$$

Table 4 shows the output obtained for the three topologies chosen. Comparing the different topology of 5-level inverter it is observed that 5-level hybrid five switch MLI requires lesser number of switches. But comparing the performance of the different topology almost three of the MLI provides similar performance only. In the case of five levels hybrid six switches MLI is the combination of H-bridge and VSI inverter. The H-bridge and Voltage source inverter produce 3-levels. These two circuits are connected in series so total output is five levels. In five levels hybrid five switches MLI is the combination of H-bridge and Diode bridge rectifier with one switch. Both circuits produce three levels. By adding five level is obtains as a final output. To implement the inverter it is possible select the Field Programmable Gate Array (FPGA)/dSPACE to generate gate pulse for the switches used. Power circuits are developed with Power (Metal Oxide Semiconductor

Field Effect Transistor) MOSFET and Power diodes. The voltage sources used for hardware may be from battery or through solar panels. Control circuit consists of MOSFET driver circuit, opto coupler and FPGA/dSPACE controller.

Table 4: Parameters of three proposed topologies

Topology	Number of switches	THD	V_{rms}
5-Level FCMLI	8	20.47%	197
5-Level Hybrid six switch MLI	6	20.47%	197
5-Level Hybrid five switch MLI	5	20.77%	196.3

Table 5: Comparison of power component requirement for the chosen inverters

Topology	5-Level FCMLI	5-Level Hybrid 6-switch MLI	5-Level Hybrid 5-switch MLI
Main Switching devices	8	6	5
Main diodes	8	6	10
Clamping capacitors	12	-	-
DC bus Capacitors	4	-	-
DC voltage sources	1	3	2

III. Conclusion

In these paper three types of embedded controller based multilevel inverter topologies are proposed. The topologies are five level flying capacitor multilevel inverter, six switch five level hybrid multilevel inverter and five switch hybrid MLI topologies. The most important feature of the hybrid multilevel inverter is being convenient for expanding and increasing the number of output levels simply with less number of switches. The switching losses also reduced and the performance of the system will be increased. The total harmonic distortion value of the embedded controller based proposed topologies are reduced than the conventional topologies. The total harmonic distortion value of proposed topologies is 20.47%, 20.47% and 20.77%.

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Biographies

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