Bootstrap Gate Driver and Output Filter of An SC-based Multilevel Inverter for Aircraft APU

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Abstract–The objective of this paper is to propose a gate drive circuit and an output filter of a switched-capacitor–based multilevel inverter for aircraft APU. With the bootstrap methodology, only one voltage source is required to power the gate driver of all switches used in the multilevel inverter. With the LC filter, this inverter is capable of providing a pure sinusoidal output voltage waveform. Finally, the performance of the proposed multilevel inverter is evaluated with simulation results and experimental results of an eleven-level prototype inverter.

Keywords–Multilevel inverter, switched-capacitor, bootstrap capacitor driver, sinusoidal PWM.

I. INTRODUCTION

Aircrafts requires an auxiliary power unit (APU) to produce high frequency alternating current, usually 400 Hz. To obtain an output waveform as much as sinusoidal shape, multilevel inverter technique has been an alternative of conventional 2-level inverter. It is well known that the more the levels of an inverter, the more near sinusoidal its output voltage is. It also means the more power semiconductors and voltage sources or capacitors are required. Consequently, one of the key technologies for multilevel inverters is to use less components and simpler structures to obtain the more levels of output voltages.

The conventional multilevel inverters can be divided into three categories [1]: neutral-point-clamped [2], flying capacitors [3], and the H-bridge cascade [4]. One of their common drawbacks is that an excessive number of power semiconductor switches and capacitor sources employed that leads to the complex structure and higher power loss.

In the literature [5], a novel multilevel inverter is presented for high frequency applications. It is made up of a novel DC-DC multilevel converter and an H-bridge as shown in Fig.1. The key point of this inverter is the DC-DC conversion section which consists of multiple switched-capacitor (SC) cells. Each cell employs only one capacitor, one active switch and two diodes. The number of *n-1* SC cells can compose an *n*-level DC-DC converter. They are connected to an H-bridge, a *(2n+1)*-level inverter can be easily derived. The structure is very simple and fewer components are required.

In order to promote this novel multilevel inverter for industrial applications, a simple gate drive circuit is developed by using bootstrap technique in this paper. It means that only one power supply is required to power the gate drive circuit for all switches employed in this inverter. This design philosophy contributes the small size and cost-effectiveness of the inverter.

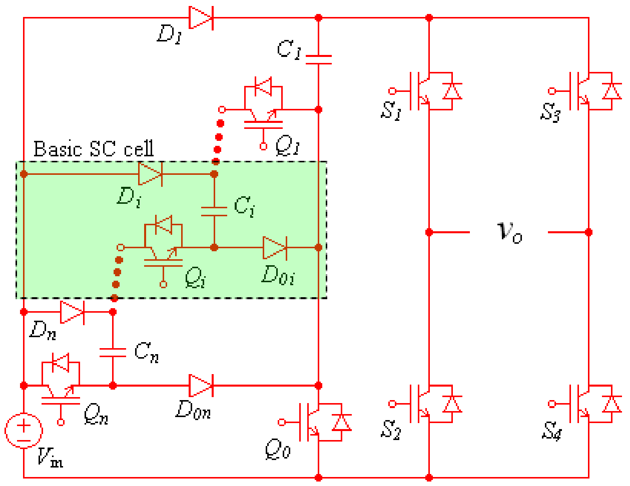


Fig.1: The multilevel inverter presented in [5]

To develop a pure sinusoidal output voltage waveform, an LC filter is added on the output terminal of this multilevel inverter in this paper.

Both simulation and experimental results of a seven-level inverter prototype are provided to evaluate the performance of the inverter.

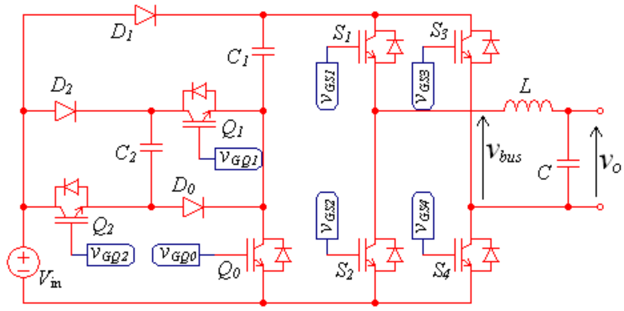


Fig.2: The seven-level topology of the multilevel inverter

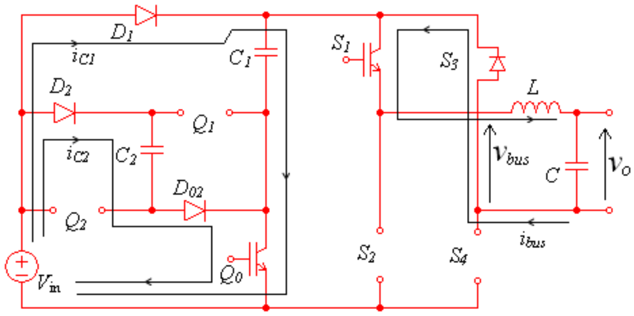
II. CIRCUIT DESCRIPTION AND STATES ANALYSIS

1. Circuit Description

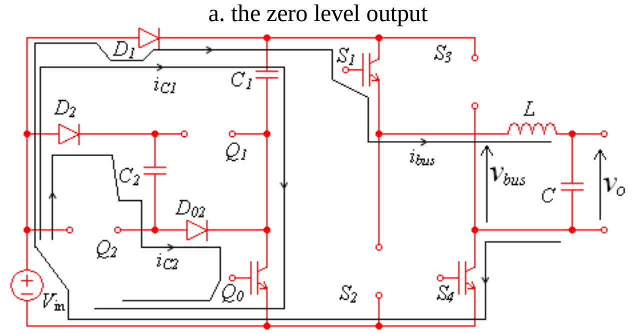
Fig.2 shows the topology of proposed inverter in seven levels. It is composed of a three-level DC-DC converter, a full bridge and an output low-pass filter. As mentioned before, the key point of the seven-level inverter is the section of DC-DC converter which consists of three active switches Q_0, Q_1 and Q_2, three diodes D_1, D_2 and D_{02}, and two capacitors C_1 and C_2. With different control strategies for the three active switches, the DC-DC conversion section is capable of converting the input voltage V_{in} in different levels, including $3V_{in}$, $2V_{in}$ and V_{in}. Like many other multilevel inverters aforementioned, the proposed inverter also includes an inverter bridge which employs four active switches S_1~S_4, and an output *LC* filter used for filtering higher harmonics.

2. States analysis

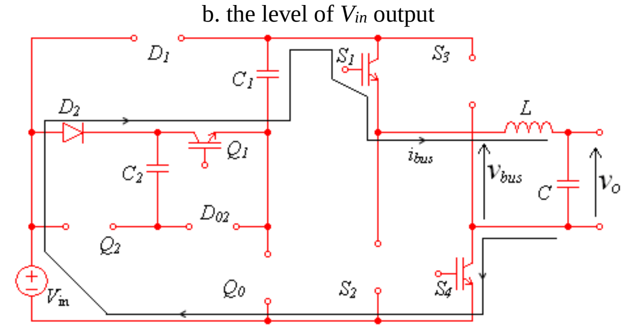
As mentioned before, with different control strategies, the circuit section of multilevel DC-DC converter of the proposed inverter is capable of converting the input voltage V_{in} in different levels. For the seven-level inverter as shown in Fig.2, there are three levels that can be produced by the multilevel converter section, including the levels of V_{in}, $2V_{in}$ and $3V_{in}$. With the combination of the operation of the inverter bridge, the inverter can provide seven levels of voltage: $3V_{in}$, $2V_{in}$, V_{in}, 0, $-V_{in}$, $-2V_{in}$ and $-3V_{in}$.



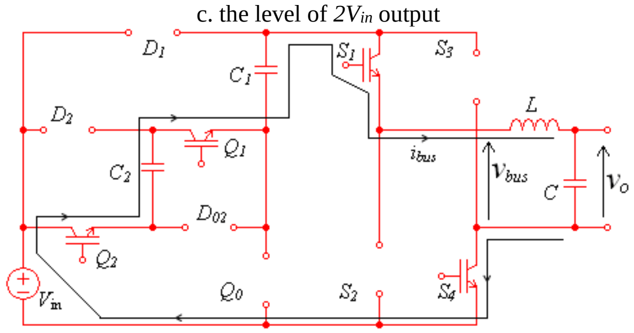
a. the zero level output



b. the level of V_{in} output



c. the level of $2V_{in}$ output



d. the level of $3V_{in}$ output

Fig.3: Working states for the proposed inverter

Specifically, when the switch Q_0 is turned ON and Q_1 and Q_2 being OFF, V_{in}, D_1, C_1 and Q_0 form a closed loop and C_1 is charged by input power V_{in}. And another closed loop is formed by V_{in}, D_2, C_2, D_{02} and Q_0, and C_2 is also charged by V_{in}. In this case, when the switch S_1 is turned ON and other switches in the H-bridge maintains the OFF state as shown in Fig.3a, the output bus voltage v_{bus} is equal to 0. But if the switch S_4 is turned ON as well as shown in Fig.3b, the bus voltage will change to V_{in}. Of course, when the switch S_2 is turned ON, and S_1 and S_4 maintain OFF state, another 0 level and $-V_{in}$ could be produced by being OFF or ON of S_3.

In the DC-DC conversion section, when the switch Q_1 is turned ON and other switches are OFF, the capacitor C_1 is connected in series with input power V_{in} through Q_1 and D_2 and the DC-DC converter section output the voltage level of $V_{in}+V_{C1}$. Assuming the capacitance of C_1 is large enough, the $2V_{in}$ level can be produced by being ON of S_1, S_4 and OFF of S_2 and S_3 as shown in Fig.3c. Similarly, when S_1 and S_4 are turned OFF and S_2, S_3 are turned ON, the level of $-2V_{in}$ can be produced as the bus voltage v_{bus}. When Q_1 and Q_2 are turned ON simultaneously while Q_0 being OFF, capacitors C_1, C_2 and input source V_{in} are connected in series by switches Q_1 and Q_2. Under the condition of the values of C_1 and C_2 are both large enough, the level of $3V_{in}$ can be output by the DC-DC converter section. In this case, if the switches S_1 and S_4 are turned ON and S_2 and S_3 being OFF, the bus voltage v_{bus} is equal to $3V_{in}$ as shown in Fig.3d. With similar method, the level of $-3V_{in}$ can be produced by turning switches S_1 and S_4 OFF, and S_2 and S_3 ON.

According the above analysis, the working states' combination of the seven-level version of the proposed inverter is concluded as shown in Tab.1. It can be seen from Tab.1 that there are eight working states for the inverter corresponding to seven voltage levels, including two zero level states. In each state, a maximum of only four switches are in conduction. And when the inverter operates alternatively in two adjacent states, there is only one or two switches' states needed to be changed.

TABLE I

Working states' combination of the seven-level inverter

No. of states	Bus voltage v_{bus}	Switching states						
		Q_0	Q_1	Q_2	S_1	S_2	S_3	S_4
1	$+3V_{in}$	0	1	1	1	0	0	1
2	$+2V_{in}$	0	1	0	1	0	0	1
3	$+V_{in}$	1	0	0	1	0	0	1
4	0	1	0	0	1	0	0	0
5		1	0	0	0	1	0	0
6	$-V_{in}$	1	0	0	0	1	1	0
7	$-2V_{in}$	0	1	0	0	1	1	0
8	$-3V_{in}$	0	1	1	0	1	1	0

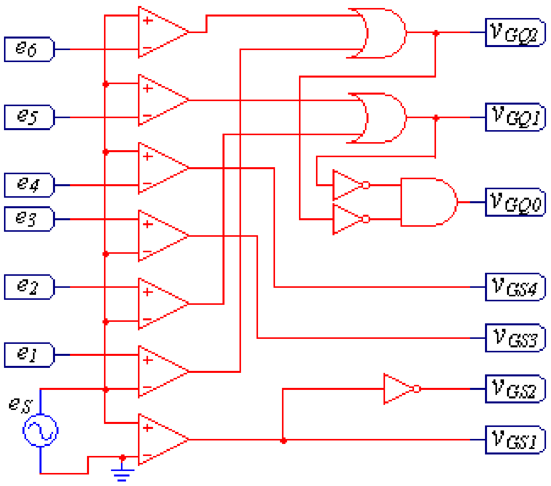
3. Modulation Method

There are many modulation methods to control a multilevel inverter, such as classic carrier-based sinusoidal PWM (SPWM) method [6]. In this section, SPWM is also introduced to modulate the multilevel inverter, as follows.

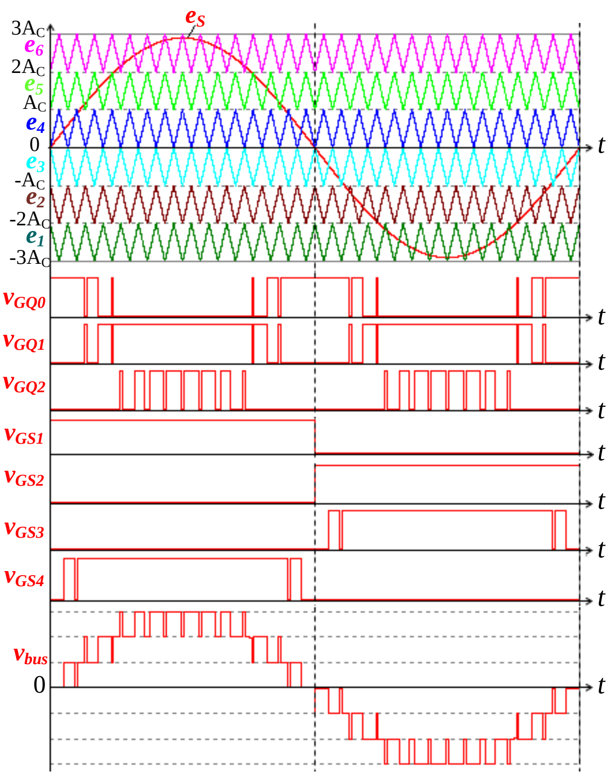
For the seven-level inverter, there are six carrier signals e_1~e_6 and a modulated sinusoidal signal e_S needed, as shown in Fig.4a which is the modulation logic circuit for the proposed seven-level inverter. Fig.4b shows the corresponding modulation waveforms, in which A_C is the amplitude of the carrier signals. If defining the symbol A_S as the amplitude of the modulated sinusoidal signal, the modulation index M can be defined as

$$M = \frac{2A_S}{(N-1)A_C} \qquad (1)$$

where N is the number of the levels and it is odd. For the proposed seven-level inverter, N=7.



a. modulation logic circuit



b. modulation waveforms

Fig.4: Modulation method for the proposed seven-level inverter

And the frequency modulation ratio can also be defined as

$$P = \omega_C / \omega_S \qquad (2)$$

where ω_C and ω_S are the angular frequencies of the carrier signal and modulated signal respectively. And the desired output sinusoidal voltage therefore can be derived as (3).

$$v_O = \frac{N-1}{2} MV_{in} \sin \omega_S t \qquad (3)$$

III. Gate Driver and Output Filter

1. Gate driver for the proposed inverter

For multilevel inverters, a large number of active switching elements are required and the drive circuit is needed for each switch. In this respect, the cost and complexity of the gate driver depends on the number of active switches required for the multilevel inverter. For the proposed inverter, although the number of active switches employed is much lesser than conventional multilevel inverter, its gate drive circuit is still a very important issue. Bootstrap capacitor driver (*BSCD*) is a mature gate drive technique and has traditionally been applied in various bridge circuits [7]. Based on the special structure of the proposed inverter, *BSCD* technique is also introduced to drive the all active switches.

In the proposed topology which consists of a full bridge and a multilevel DC-DC converter, the gate drivers for the full bridge is very simple and is not elaborated in the text. For the DC-DC conversion section, active switches Q_1 to Q_n are actually connected in series with Q_0 though diodes D_1' to D_n' respectively. And Q_0 can be turned ON just after all other switches Q_1 to Q_n being OFF. The voltage for the gate driver of Q_0 therefore can be supplied directly by the signal power V_{gate}. And the voltage sources for the gate drivers of Q_1 to Q_n could be implemented by using a bootstrap capacitor for each switch as shown in Fig.5. Take the diver circuit of Q_1, BSCD-1 as an example, when switch Q_0 is turned ON while Q_1 being OFF, the capacitor C_{B1} is charged by the signal power V_{gate} though D_{11}, D_1' and Q_0, the energy is stored in C_{B1} and its voltage is eventually equal to V_{gate}. When Q_0 is turned OFF, switch Q_1 could be controlled by its trigger signal v_{GQ1} and voltage as well as power are supplied by the capacitor C_{B1}. For other switches Q_i (i=2, 3, …, n), the gate drivers BSCD-i are totally the same as BSCD-1. The gate diver for the total inverter is therefore very simple and only one signal power V_{gate} is required.

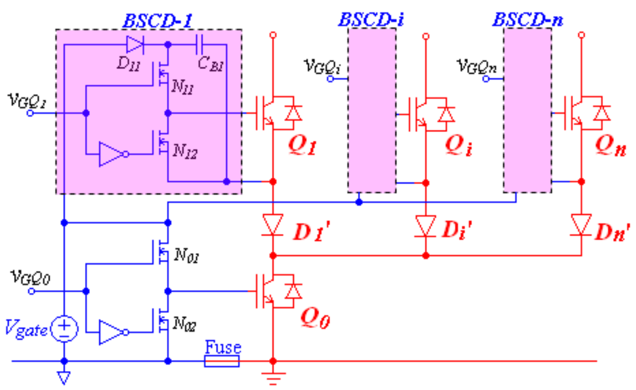


Fig.5: Gate driver for the proposed inverter

2. Output filter design for the proposed inverter

Comparing with 2-level inverter, the output performance of the multilevel inverters is more satisfactory in the terms of harmonics. The output filters therefore are easier to be designed. Usually, the multilevel inverters only need to employ an *LC* low-pass output filter with reasonable parameters to provide satisfactory output sinusoidal voltage. The detailed design methods of *LC* filter for PWM inverters have been introduced in [8], [9] and the technique is very mature, that is mainly based the considerations of reactive power and output voltage harmonics. Simply, the design steps of a *LC* filter for PWM inverters can be summarized as follows.

1). to determine the filter cut-off frequency ω_f referring to the carrier signals frequency ω_C and the modulated signal frequency ω_S, i.e.

$$\omega_f = \frac{1}{\sqrt{LC}} \tag{4}$$

and

$$\omega_S < \omega_f < \omega_C \tag{5}$$

2). to determine the inductance of the filter according to the principle of minimum reactive power. For the pure resistance load, the reactive power Q_{LC} caused by the *LC* filter could be approximately expressed as

$$Q_{LC} \approx \omega_S I_O{}^2 L + \left(\frac{\omega_S}{\omega_f{}^2} + \frac{\omega_S{}^3}{\omega_f{}^4}\right) U_O{}^2 \frac{1}{L} \tag{6}$$

where U_O and I_O are the rms values of the output voltage and load current respectively. The minimum reactive power is obtained when $\partial Q_{LC}/\partial L = 0$. The value of the inductor L therefore can be calculated by

$$L = \frac{U_O}{I_O \omega_f} \sqrt{1 + \left(\frac{\omega_S}{\omega_f}\right)^2} \tag{7}$$

3). calculate the capacitance of the filter according the value of inductance L and the cut-off frequency ω_f, i.e.

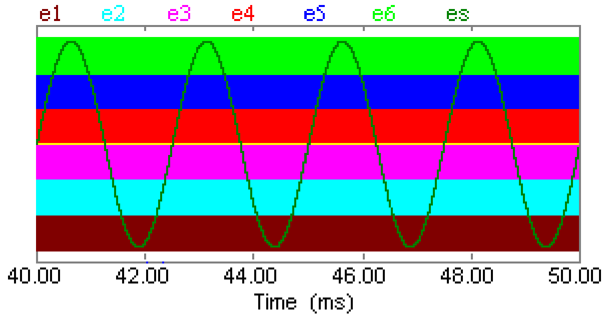
$$C = \frac{1}{\omega_f{}^2 L} \tag{8}$$

IV. Simulation Experimental Verification

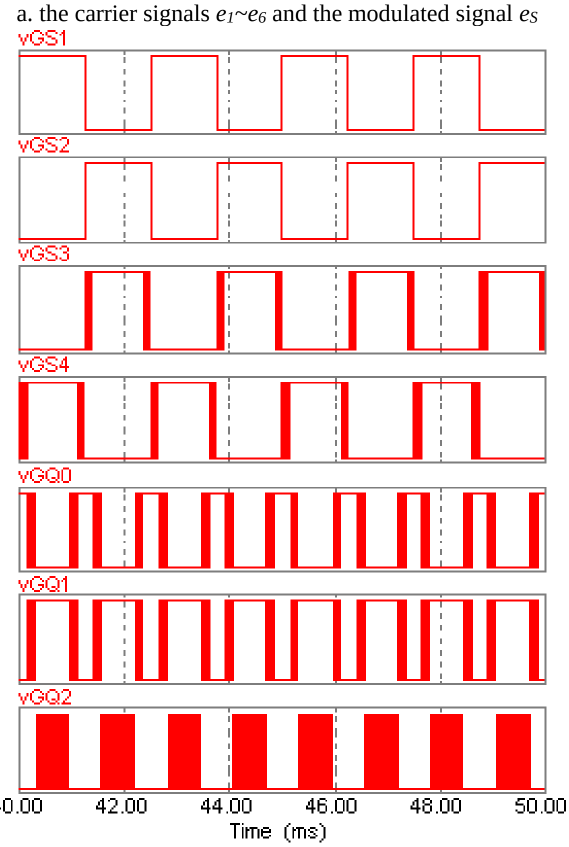
1. Simulation Results

To verify the feasibility of the proposed gate driver and the LC output filter developed for the multilevel inverter of Fig.1, a simulation model is built based on the seven-level topology, the multicarrier SPWM technique and the gate driver structure as shown in Figs. 2, 4a and 5 respectively. Fig.6 shows the simulated results and the simulation parameters are chosen as following: the dc input voltage V_{in} is 24V; the capacitances of C_1 and C_2 both are 1000μF; the carrier signals frequency and the modulated signal frequency are 40kHz and 400Hz respectively; the modulation index *M* is 0.96 and the load resistance is 22Ω; the signal power V_{gate} is 15V and the bootstrap capacitor is 1μF; the output filter inductance *L* and capacitance *C* are 850μH and 2.2μF respectively.

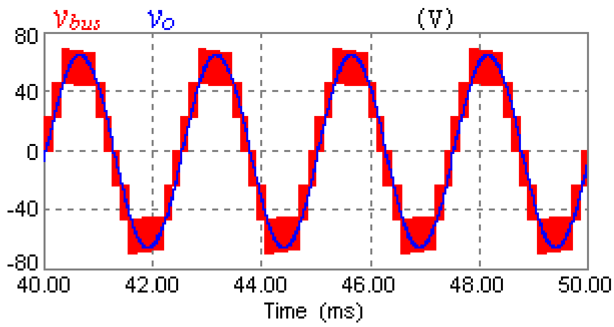
Simulation results indicate that the multilevel inverter is capable of generating a pure sinusoidal output voltage waveform v_O and this is benefited from the bootstrap gate driver circuit and the LC filter developed in this paper.



a. the carrier signals e_1~e_6 and the modulated signal e_S



b. switching control signals

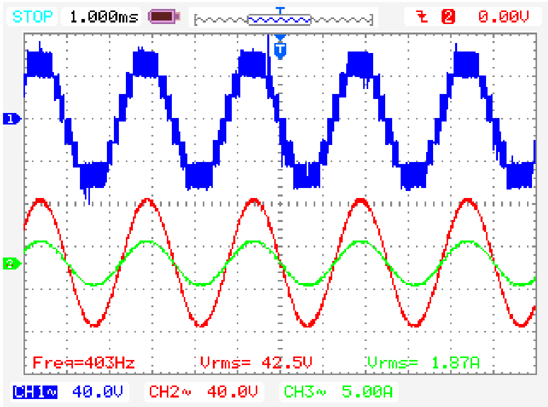


c. output voltage waveforms

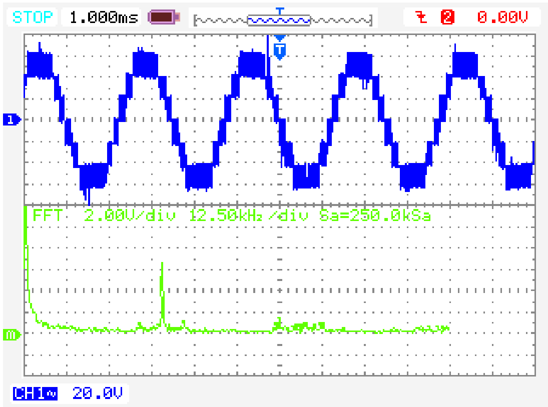
Fig.6: Simulation results of the seven-level output

2. Experimental Results

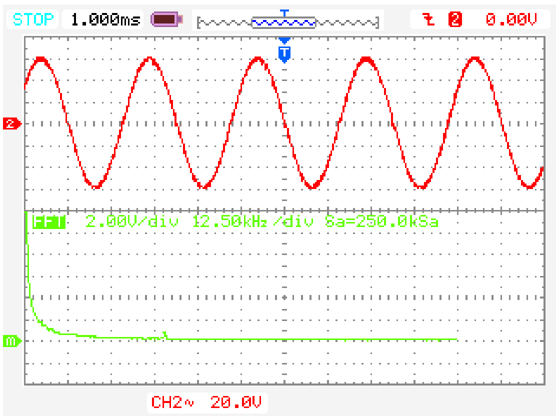
A prototype of the seven-level version of the proposed inverter is developed to evaluate the performance of the proposed topology in the generation of a desired output voltage waveform. The basic parameters are the same as that used for simulation and the switches are selected as following: S_1~S_4 and Q_0 are MOSFETs IRFB4019PBF; Q_1 and Q_2 are MOSFETs IRFI540A; MBR10100 are used as the diodes D_1, D_2 and D_{02}. The modulation index M is still 0.96. The experimental results are shown in Fig.7. As shown in Fig.7a, the output voltage waveforms are basically the same as the simulation results aforementioned except for the amplitude, which is slightly lower than the theoretical value the simulation result because the voltage drops of the switching devices. Fig.7b shows the frequency spectrum of the bus voltage v_{bus}. It can be seen that the lower order harmonics are small but the higher harmonics cannot be neglected, especially those closed to the carrier signals frequency. This issue is easily solved by the output LC filter as shown in Figs.7c and 7d, which show the frequency spectrum of the output voltage v_O.



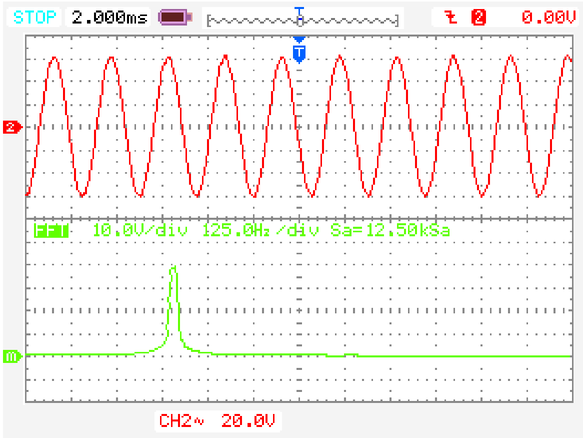
a. CH1: v_{bus}; CH2: v_O; CH3: i_O



b. frequency spectrum of v_{bus} (0~125kHz)



c. frequency spectrum of v_O (0~125kHz)



d. frequency spectrum of v_O (0~1.5kHz)

Fig.7: Experimental results of the seven-level inverter

IV. Conclusion

In this paper, a simple gate drive circuit and an output filter are developed for the multilevel inverter presented in [5]. With this bootstrap gate driver, only one voltage source is required to power the drive circuit of all switches employed in this inverter. This makes it has the advantages of small size and cost-effectiveness. With the LC filter, this inverter is capable of providing a pure sinusoidal output voltage waveform. And it is very suitable for aircraft APUs. Simulation and experimental results indicate the gate driver and the LC filter introduced in this paper provide a very well solution to promote the industrial applications of the multilevel inverter.

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