Soft-switching Topologies for Switched Reluctance Motors in the Application of Electric Vehicles

Jingwei Zhu[1] K.W.E Cheng[2] N.C. Cheung[3]

[1,2,3] Power Electronics Research Centre, Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong
E-mail: 15901658r@connect.polyu.hk, eeecheng@polyu.edu.hk, norbert.cheung@polyu.edu.hk

Abstract- two topologies of soft-switching for the switched reluctance motor (SRM) are proposed in this paper to reduce the switching loss and EMI in the chopping and commuting periods. The design circuit of the topologies are shown and the feature of the current or voltage of resonant elements are analyzed in theory and confirmed by simulation of Matlab/Simulink. Besides, the energy loss of the soft-switching circuit for the second topology is calculated and compared with the conventional one. The loss is computed under different rotating speeds to simulate electrical vehicle (EV) running under various speeds and the advantage of the proposed circuit is proved.

Keywords-SRM, Matlab/Simulink, soft-switching, energy loss, topology

I. INTRODUCTION

With the increasingly serious environment pollution and energy crisis, EV has become a new trend for future industrial vehicle study due to its high efficiency and low emission. Motor drive is the central part of EV because of offering enough power for its performing. The SRM has the advantage over other kinds of motors as it has a simple structure, low cost, high efficiency, easy control, low starting current and high pull-up torque. Therefore, it has a potential prospect in the application of machine drives of EV. But in order to optimize a control strategy for SRM drive, high frequency is required for accurate current and flux linkage regulation, causing considerable switching losses and EMI. Soft switching technology is an efficient method in lowering these losses for EV in normal urban driving [1].

In [2], resonant DC link (RDCL) is utilized to achieve ZVS on and ZCS off, but the resonant inductor is in series with the inverter-bridge leading to unnecessary loss since both resonant and load current flow through this resonant inductor. Literature [3] introduces additional inductors and capacitors into the topology, however, there's a resonant inductor in the main loop as well. A novel topology is put forward in [4] with PWM method to reduce the switching losses, but the resonant inductor is still in the main circuit. The soft-switching topology in [5] can only attain ZVS on for phase switches. Document [6-8] solved the inverter problems above, but when there is no load, the formation of zero voltage between the DC bus encounters great difficulties.

This paper proposes two topologies to reduce the switching losses and settle the challenges above. The topology in section II utilizes only one auxiliary switch and remains the resonant inductor in the resonant circuit, thus declining the current flowing through it greatly. Besides, the number of the auxiliary elements is reduced to a great extent. Section III gives an improved topology to achieve controlling the zero voltage duration freely and no current flowing through the resonant inductor during normal conducting time, although it adds two additonal auxiliary switches. Section IV makes a comparison of the energy losses between the improved topology in section III and the convential one; furthermore, some analysis is offered.

II. A SUITABLE SOFT-SWITCHING TOPOLOGY FOR THE SRM

The designed circuit is in the following Figure 1:

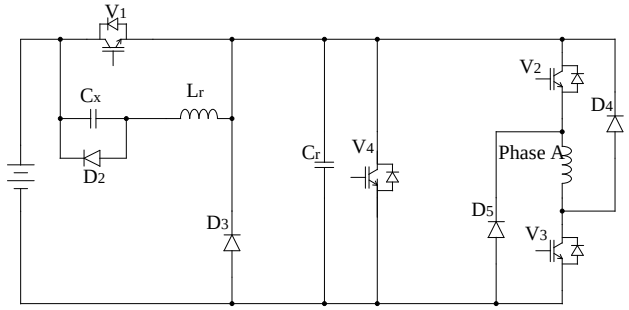


Figure 1. Schematic of the new soft-switching topology.

In this Figure 1, one phase of the SRM is simplified as a constant inductance during the soft-switching period since it is short enough. And the parameter of the elements in the circuit is in the following Table 1:

Table 1: Circuit Parameters for the Topology

E (V)	300	C_s (pF)	0.1
C_x (nF)	1000	L_r (μF)	60
C_r (nF)	30	L_A (mF)	10

V_1, V_2, V_3, V_4 of the switching components are all selected as IGBT. This proposed circuit can simplify the control of switching elements, reduce the number of switching and resonant components to lower the hardware cost. Besides, it has extra advantages of each switch turning on-off at zero voltage and the maximum enduring voltage is equal to that of the DC source. Meanwhile, because of no series voltage-divider capacitors between the DC bus, there's no potential variation of the neutral point [9].

The theoretical waveforms of the switching signal, voltage or current of the resonant components are shown as follows in Figure 2:

This circuit can be divided into six working modes

Mode I ($0\sim t_0$): it's the initial condition of the whole circuit with V_1, V_2, V_3 on and V_4 off. The circuit is stable and there is a constant reverse current I_{L0} flowing through the resonant inductor L_r.

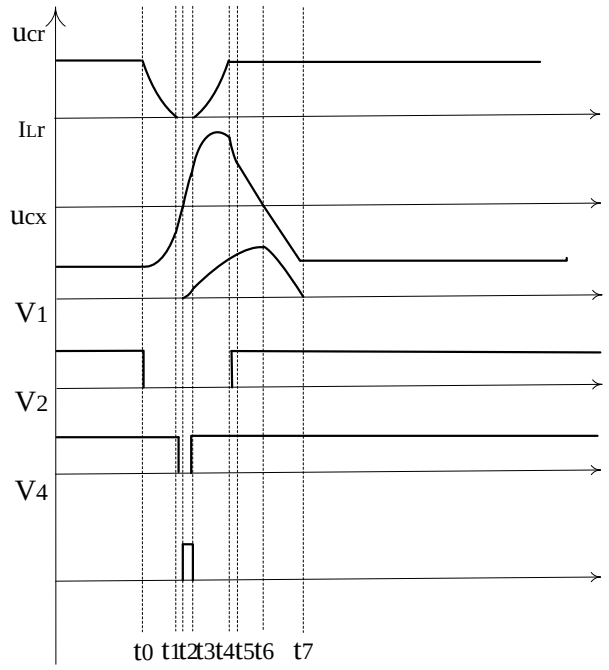


Figure 2. theoretical waveform for the novel topology

Mode II (t_0~t_1): when V_1 is off, L_r and C_r begin their resonance with both the current I_{lr} and voltage u_{cr} decreasing. The energy of L_r feeds back to the battery while that of C_r is transferred to both the winding and the battery. With C_r discharging, the DC bus voltage is declining gradually until zero. The differential equation is as follows:

$$u_{cr} = -L_r \cdot \frac{di_r}{dt} + E \tag{1}$$

$$C_r \cdot \frac{du_r}{dt} = i_r - I_0 \tag{2}$$

Then, with the initial value $u_{cr}(t_0) = E$, $i_{cr}(t_0) = -I_{L0}$, we can get

$$u_{cr} = E - \frac{(I_0 + I_{L0})}{\omega_r C_r} \sin[\omega_r (t - t_0)] \tag{3}$$

$$i_r = I_0 - (I_0 + I_{L0}) \cos[\omega_r (t - t_0)] \tag{4}$$

where, $\omega_r = \frac{1}{\sqrt{L_r C_r}}$, I_0 is the current of the winding load. Therefore, the mode II time,

$$T_2 = \frac{1}{\omega_r} arcsin \frac{\omega_r C_r E}{I_0 + I_{L0}} \tag{5}$$

Mode III (t_1~t_2): when u_{cr} reaches zero, diode D_3 conducts which clamps the DC bus voltage at zero and V_2 can be switched off at zero voltage. During this period, L_r bears a constant voltage of the DC source and i_r decreases linearly until it reaches zero point. So,

$$i_r = \frac{E}{L_r}(t - t_1) - I_1 \tag{6}$$

Thus, the mode III time,

$$T_3 = \frac{L_r I_1}{E} \tag{7}$$

Mode IV (t_2~t_3): IGBT V_4 is turned on to keep i_r positive and the capacitor u_{cx} is conducting. So C_x and L_r start their resonance under the DC bus voltage until it i_r attains its setting value I_2 at the moment t_3. At the end of this period, the switch V_2 is turned on at zero voltage point of the DC bus. Then IGBT V_4 is turned off. We can get the equation,

$$u_{Cx} + L_r \frac{di_r}{dt} = E \tag{8}$$

$$C_x \frac{du_{Cx}}{dt} = i_r \tag{9}$$

From (8) and (9), the result is

$$u_{Cx} = E - E\cos[\omega_x (t - t_2)] \tag{10}$$

$$i_r = \omega_x C_x E \sin[\omega_x (t - t_2)] \tag{11}$$

Therefore, the duration of this mode is

$$T_4 = \frac{1}{\omega_x} \arcsin\left(\frac{I_2}{C_x \omega_x E}\right) \tag{12}$$

Mode V(t_3~t_4): With V_4 switched off, L_r, C_x, C_r begin their resonance together. Because of $C_x >> C_r$, the series capacitor can be simplified as

$$\frac{C_x C_r}{C_x + C_r} \approx C_r \tag{13}$$

In this mode, u_{Cx} can be regarded as constant U. During the resonance process, both L_r and C_r are charged, with i_r and u_{Cr} increasing till u_{Cr} getting to the DC bus voltage.
The differential equations are as follows:

$$E - U = L_r \frac{di_r}{dt} + u_{cr} \tag{14}$$

$$i_r - I_0 = C_r \frac{du_{cr}}{dt} \tag{15}$$

Then we can calculate,

$$u_{cr} = (E - U)(1 - \cos[\omega_r (t - t_3)]) + \frac{I_2 - I_0}{\omega_r C_r} \sin[\omega_r (t - t_3)] \tag{16}$$

$$i_r = I_0 + (I_2 - I_0)\cos[\omega_r (t - t_3)] + \omega_r C_r (E - U) \sin[\omega_r (t - t_3)] \tag{17}$$

From the outcome, when u_{cr} increases to $(E - U)$, i_r reaches its maximum and from then on, u_{cr} augments while i_r decreases. The duration of this mode can be calculated as

$$T_5 = \frac{1}{\omega_r} \left(\arcsin\left(\frac{E - U}{M}\right) + \arcsin\left(\frac{U}{M}\right)\right) \tag{18}$$

where, $M = \sqrt{\frac{(I_2 - I_0)^2}{\omega_r^2 C_r^2} + (E - U)^2}$

Mode VI(t_4~t_7): During this mode, two parts of it need to be analysed. To start with, when i_r is still positive, C_x and L_r start resonance with u_{cx} increasing and i_r declining. Before i_r descends to the winding load current I_0, Diode

D1 is conducting during which time the switch V_1 can be turned on under zero voltage condition. The first part ends with u_{cx} arriving at its peak and i_r dropping to zero. The second part begins when i_r is negative, during which, C_x is discharged and i_r increases reversely. It comes to an end when u_{cx} drops to zero voltage and Diode D_2 is on. Later, it comes back to Mode I and start a new circulation.
The equation is as follows:

$$u_{cx} + L_r \frac{di_r}{dt} = 0 \tag{19}$$

$$C_x \cdot \frac{du_{cx}}{dt} = i_r \tag{20}$$

Then the value we get is

$$u_{cx} = Ucos[\omega_r(t - t_4)] + \frac{I_3}{C_x\omega_x} sin[\omega_r(t - t_4)] \tag{21}$$

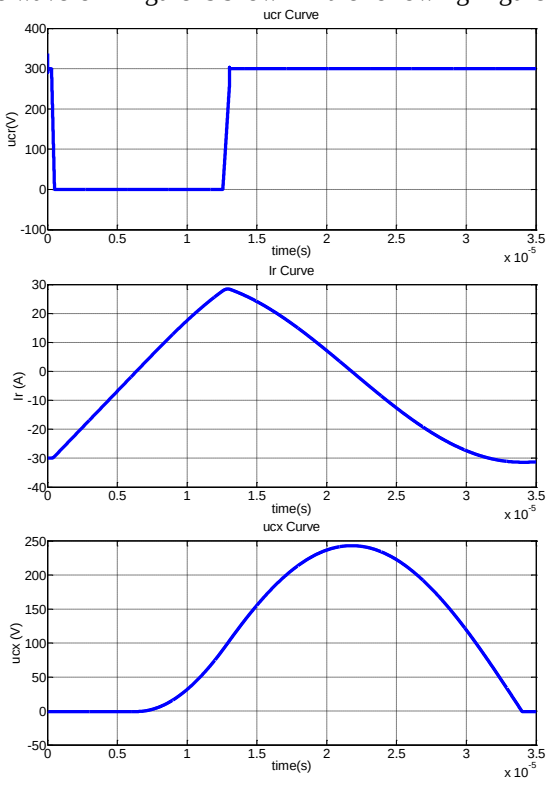
$$i_r = I_3 \cos[\omega_r(t - t_4)] - C_x\omega_x Usin[\omega_r(t - t_4)] \tag{22}$$

The length of time is

$$T_6 = \frac{1}{\omega_x}(\pi - arctan\frac{UC_x\omega_x}{I_3}) \tag{23}$$

According to the theory analysis above, a simulation of one circulation based on Matlab/Simulink has been done to confirm the theory. The switching signal is applied on the basis of the calculated duration of six modes. The initial current I_{l0} is set as -30A, I_2 is selected as 37.6A and winding load current I_0 is chosen as 12A.

The waveform figure is shown in the following Figure 3:



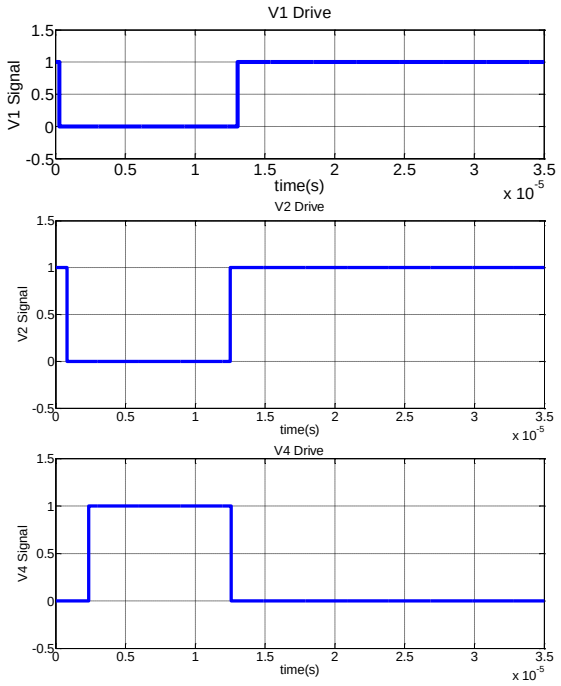


Figure 3. Waveform from Matlab/Simulink

The simulation results agree with the theoretical analysis, confirming the validity of this new topology.

III. An Improved Topology For The SRM

The proposed topology is shown below in Figure 4:

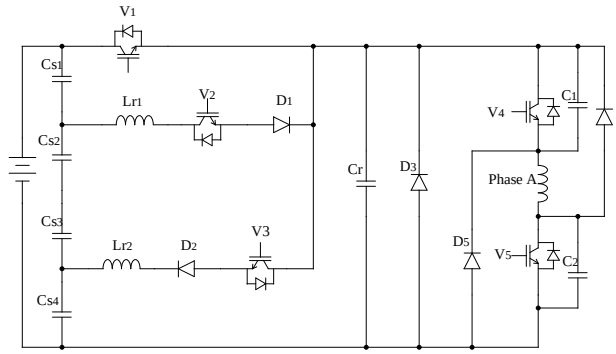


Figure 4. Schematic of the improved soft-switching topology

In this Figure 4, one phase of the SRM is also simplified as a constant inductance during the soft-switching period since it is short enough. And the parameter of the elements in the circuit is in the following Table 2:

Table 2: Circuit Parameters for the Improved Topology

$E(V)$	240	$L_A(mH)$	0.01
$C_r(nF)$	25	$L_r(\mu H)$	10
$C_i(pF)$ $(i$ from 1 to 2$)$	0.1	$L_{r1}(\mu H)$	10
C_{si} (μF) $(i$ from 1 to 4$)$		25	

V_1, V_2, V_3, V_4, V_5 are all IGBT in the schematic. This improved circuit has the advantage of controlling the zero voltage time by selecting the turning-on time of V_2 [10]. And the theoretical waveforms of the elements in this topology are shown as follows in Figure 5:

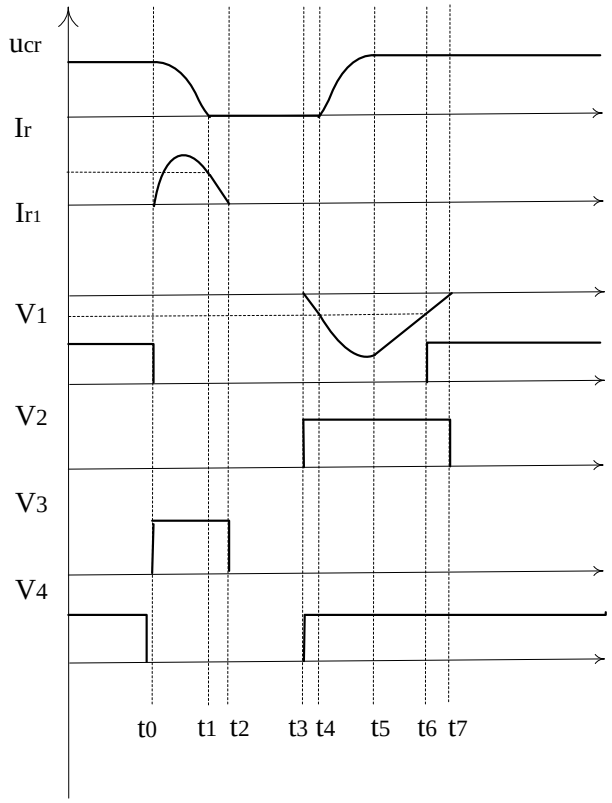


Figure 5. theoretical waveforms for the improved topology

This topology can be separated into eight modes.

Mode I ($0\sim t_0$): both V_2 and V_3 are off while V_1, V_4, V_5 are on during this period. Phase A is conducting.

Mode II ($t_0\sim t_1$): At the moment t_0, the switch V_1, V_2 and V_4 are all been turned off with only V_3 and V_5 on. Because of the existence of C_i, V_4 is turned off at zero voltage. Meanwhile, V_1 is also turned on during zero voltage stage. C_r, V_3, L_r, C_4 makes up a loop with C_r and L_r starting their resonance. Because of no sudden change of current in L_r, V_3 is switched on under a zero current condition. At the beginning, C_r is discharged while i_r increases until u_{cr} reaches $\frac{E}{4}$, then i_r starts to decrease ending with u_{cr} getting to the zero voltage point. At the time t_1, C_r is clamped by D_3 to keep a constant zero voltage situation. The equations of it are as follows:

$$u_{cr} = L_r \cdot \frac{di_r}{dt} + \frac{E}{4} \tag{23}$$

$$C_r \frac{du_{cr}}{dt} = -i_r \tag{24}$$

The results are calculated as

$$u_{cr} = \frac{E}{4} + \frac{3}{4}Ecos[\omega_r(t-t_0)] \tag{25}$$

$$i_r = \frac{3}{4}E\omega_r C_r sin[\omega_r(t-t_0)] \tag{26}$$

Therefore, we can get the duration of this period

$$T_2 = \sqrt{L_r C_r}\arccos(-\frac{1}{3}) \tag{27}$$

Mode III ($t_1\sim t_2$): since C_r is clamped by D_3, L_r will begin to discharge under the reverse voltage $\frac{E}{4}$ until it arrives at zero point.

$$i_r = I_1 - \frac{E(t-t_1)}{4L_r} \tag{28}$$

The time period is

$$T_3 = \frac{4L_r I_1}{E} \tag{29}$$

Mode IV ($t_2\sim t_3$): during this mode, no switches are on and the length of period can be controlled by deciding the turning on moment of V_2. V_3 is both zero voltage and zero current turned off. Therefore, the switching on moment of V_4 can be located during the zero voltage stage definitely without thinking about the value of L_r and C_r.

Mode V ($t_3\sim t_4$): V_2, V_4 and V_5 are on while V_1 and V_3 are off. The phase winding is conducting. Because the DC bus voltage is zero, V_4 is ZVS on and V_2 is ZCS on as a result of the existence of L_{r1}. During this mode, u_{cr} still keeps zero voltage and i_r increases reversely under the voltage of $\frac{3}{4}E$ until it reaches the winding current I_0.

$$i_{r1} = -\frac{3E}{4L_{r1}}(t-t_3) \tag{30}$$

Therefore, the length of this period is

$$T_5 = \frac{4L_{r1}I_0}{3E} \tag{31}$$

Mode VI ($t_4\sim t_5$): C_r and L_{r1} start their resonance and it lasts until u_{cr} reaches E.

$$\frac{3}{4}E = -L_{r1}\frac{di_{r1}}{dt} + u_{cr} \tag{32}$$

$$C_r \frac{du_{cr}}{dt} = -i_{r1} - I_0 \tag{33}$$

Then we can get the result

$$u_{cr} = \frac{3}{4}E - \frac{3}{4}Ecos[\omega_r(t-t_4)] \tag{34}$$

$$i_{r1} = -I_0 - \frac{3}{4}EC_r\omega_r \sin[\omega_r(t-t_4)] \tag{35}$$

$$T_6 = \frac{1}{\omega_r}\arccos\left(-\frac{1}{3}\right) \tag{36}$$

Mode VII ($t_5\sim t_6$): Since during this mode, $|i_{r1}|>I_0$, the voltage of $\frac{E}{4}$ is added to L_{r1}. C_{si}, V_1, V_2, L_{r1} form a series loop. V_1 is clamped by the diode, so it's ZVS on during this period.

$$i_{r1} = -I_0 - \frac{\sqrt{2}}{2}EC_r\omega_r + \frac{E}{4L_{r1}}(t-t_5) \tag{37}$$

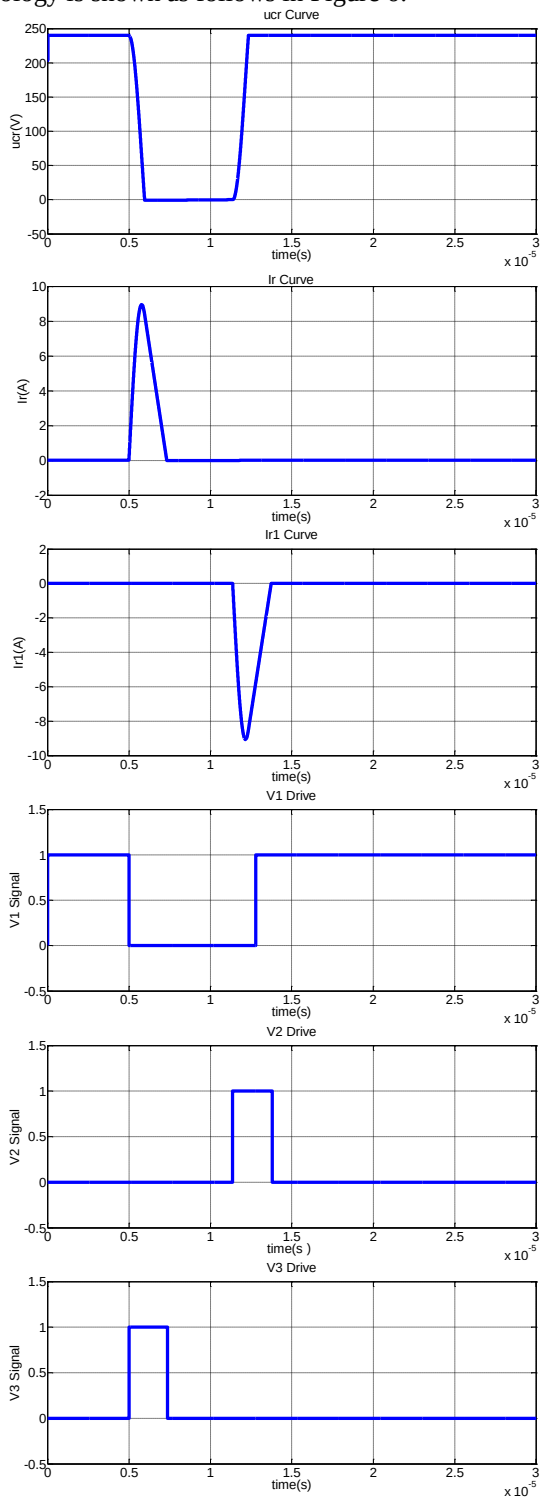
So the duration is

$$T_7 = 2\sqrt{2}\omega_r C_r L_{r1} \tag{38}$$

Mode VIII $(t_6 \sim t_7)$: L_{r1} is still under $\frac{E}{4}$ voltage and the changing rule of i_{r1} is the same as that in Mode VII. When i_{r1} reaches zero, V_2 is ZCS off. Then a new circulation begins.

$$T_8 = \frac{4L_{r1}I_0}{E} \tag{39}$$

The simulation results during one time period of this topology is shown as follows in Figure 6:



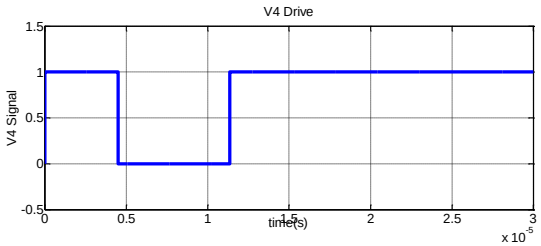


Figure 6. Waveforms from Matlab/Simulink of the improved topology

Then the improved topology is added into a whole current chopping control (CCC) system for a 6/4 SRM. And the DC source voltage is changed to 120V with other parameters unchanged. CCC is a common control method for SRM. When a SRM is running at a low speed, it has a small rotating EMF and a high value of di/dt. Also, because of long period for inductance increasing, we usually utilize CCC to prevent overcurrent in each phase. It regulates the upper and lower limit of the permitted current and keep θ_{on}、θ_{off} constant, in order to limit the value of current within an expected range. Its principle is in the following shown in Figure 7:

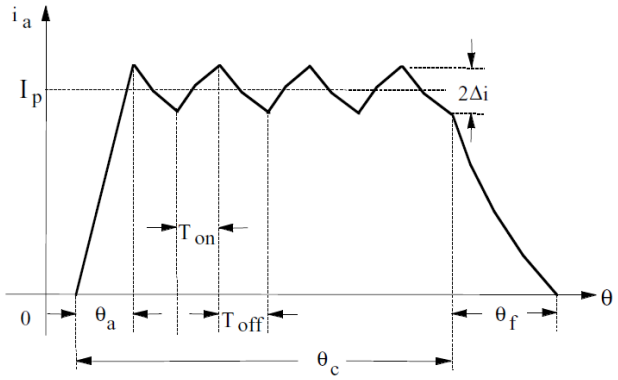
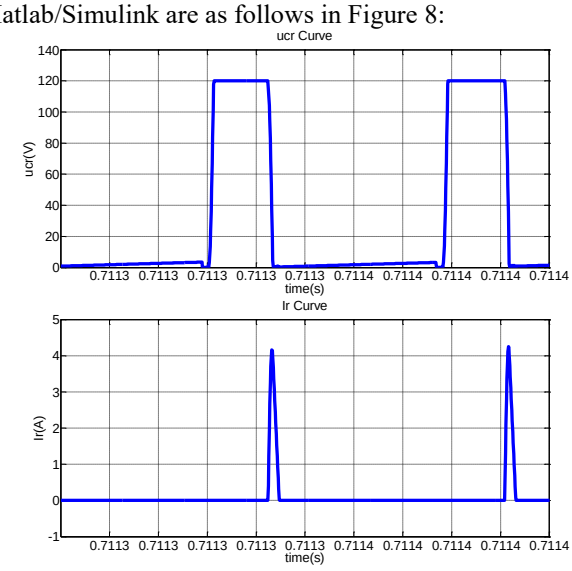


Figure 7. I_p is the chopping current of the winding with the upper limitation $I_p + \Delta i$ and the lower limitation $I_p - \Delta i$

The simulation results of the waveforms on the basis of Matlab/Simulink are as follows in Figure 8:



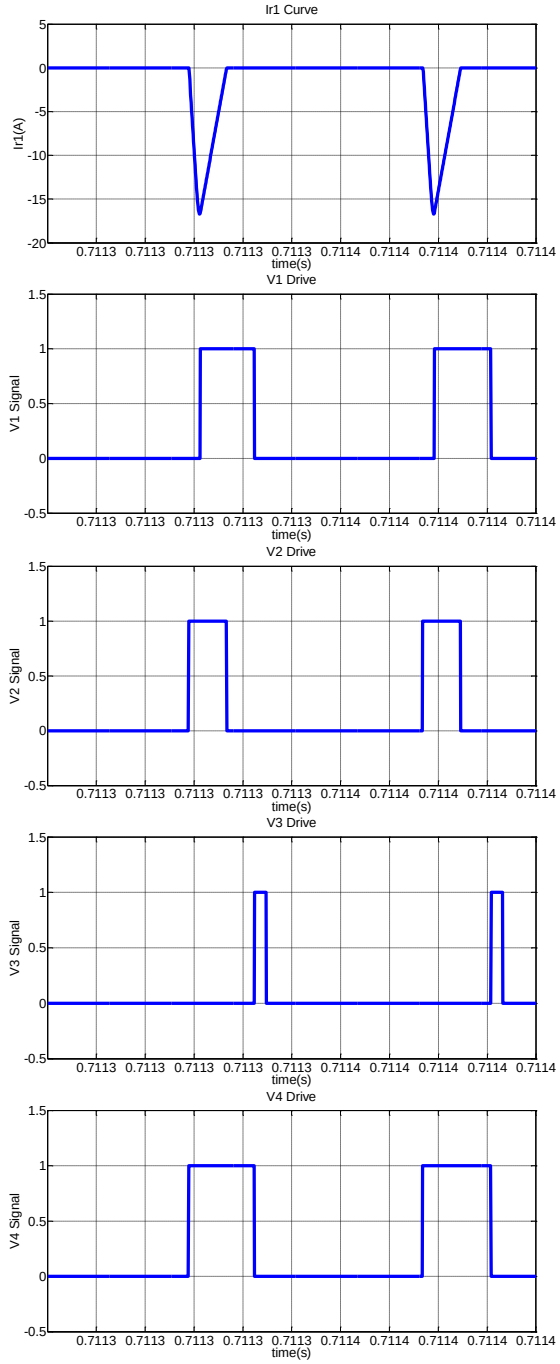


Figure 8. Waveform from Matlab/Simulink of the improved topology when applied to a CCC system for a 6/4 SRM

IV. Comparison Of The Improved Soft-switching Topology With The Conventional One In The Applications Of Electric Vehicles

According to the analysis of the mode of the improved topology, all the switching elements achieve the ZVS or ZCS on-off, so the switching loss is zero. However, because of increasing the number of auxiliary switches and diodes, the conducting loss will rise. It is known that the losses include the sorts of switching and conducting. Therefore, a comparison of loss between the proposed improved topology and the traditional one is needed.

The additional conducting losses come from the clamped diode of V_1, diodes D_1, D_2, D_3 and IGBT V_1, V_2, V_3. f_0 in the following equations is the switching frequency of current chopping control.

$$P_D = f_0 U_{ce} \int_0^{T_7} (-\frac{\sqrt{2}}{2} E C_r \omega_r + \frac{E}{4L_{r1}} t) dt \quad (40)$$

$$P_{D3} = f_0 U_{ce} \int_0^{T_3} (I_1 - \frac{Et}{4L_r}) dt \quad (41)$$

$$P_{D2} = f_0 U_{ce} (\int_0^{T_2} \frac{3}{4} E \omega_r C_r \sin(\omega_r t) dt + \int_0^{T_3} (I_1 - \frac{Et}{4L_r}) dt) \quad (42)$$

$$P_{D1} = f_0 U_{ce} [\int_0^{T_5} \left(-\frac{3E}{4L_{r1}} t\right) dt + \int_0^{T_6} \left(-I_0 - \frac{3}{4} E C_r \omega_r \sin(\omega_r t)\right) dt + \int_0^{T_7} \left(-I_0 - \frac{\sqrt{2}}{2} E C_r \omega_r + \frac{E}{4L_{r1}} t\right) dt + \int_0^{T_8} (-I_0 + \frac{E}{4L_{r1}} t) dt] \quad (43)$$

$$P_{V_1} = I_0^2 R T_1 + \int_0^{T_8} (\frac{E}{4L_{r1}} t)^2 R dt \quad (44)$$

$$P_{V_2} = \int_0^{T_5} (\frac{3E}{4L_{r1}} t)^2 R dt + \int_0^{T_6} [-I_0 - \frac{3}{4} E C_r \omega_r \sin(\omega_r t)]^2 R dt + \int_0^{T_7} \left(-I_0 - \frac{\sqrt{2}}{2} E C_r \omega_r + \frac{E}{4L_{r1}} t\right)^2 R dt + \int_0^{T_8} (-I_0 + \frac{E}{4L_{r1}} t)^2 R dt \quad (45)$$

$$P_{V_3} = \int_0^{T_2} [\frac{3}{4} E \omega_r C_r \sin(\omega_r t)]^2 R dt + \int_0^{T_3} (I_1 - \frac{Et}{4L_r})^2 R dt \quad (46)$$

Where D is the clamped diode of V_1, U_{ce} is the forward voltage drop of a diode.

For the hard switching period in a conventional topology for the SRM, the switching process of the voltage and current can be simplified as the following equation as:

$$u_{ce} = E - \frac{E}{\Delta t} t \quad (47)$$

$$i_{ce} = \frac{I_0}{\Delta t} t \quad (48)$$

$$P_{sw} = \frac{1}{T_0} \int_0^{T_0} u_{ce} \cdot i_{ce} dt = \frac{2}{T_0} \int_0^{\Delta t} u_{ce} \cdot i_{ce} dt = \frac{1}{3} E I_0 f_0 \Delta t \quad (49)$$

Where, the switching period T_0 is 4×10^{-5}s, voltage rising and current descending time Δt is 2×10^{-7}s.

In Table 3, power loss of both topologies is shown as below:

Table 3: Power Loss Of The Conventional And Improved Topology

n(r/min)	Conventional		Soft-switching		Percentage saved(%)
	I_0(A)	P	I_0(A)	P	
100	9.0	1.80	8.80	1.19	33.9
200	9.8	1.96	9.60	1.30	33.7
300	10.6	2.12	10.4	1.41	33.5
400	11.3	2.26	11.1	1.51	33.2
500	12.0	2.40	11.8	1.60	33.3
600	12.6	2.52	12.3	1.67	33.7
700	13.3	2.66	13.0	1.77	33.5
800	13.8	2.76	13.5	1.84	33.3
900	14.3	2.86	14.0	1.91	33.2

1000	14.8	2.96	14.5	1.98	33.1

The comparison curve of both topologies for the power loss is shown in the following Figure 9:

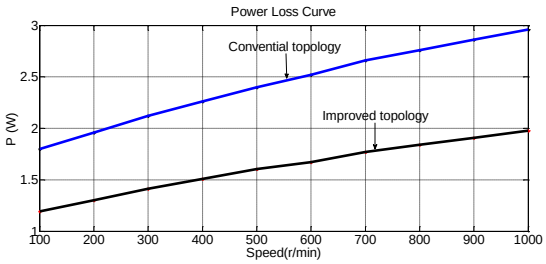


Figure 9. comparison of power loss for different topologies under various speed

From the comparison between these two topologies, less power loss of the proposed topology is seen in the table and figure, about 33 percent of energy saving. Furthermore, with the vehicle speed increasing, the current produced by the DC source ascends, thus increasing the energy or power loss.

VI. Conclusion

This paper proposes two topologies of soft-switching for the SRM drive. Each topology is analysed theoretically and calculated by equations to gain the ideal waveforms of the auxiliary components in the soft-switching part. These topologies also have their own deficiencies. The first one has current flowing through the resonant inductance during normal conducting time increasing extra loss and the zero voltage period can't be controlled. Furthermore, the auxiliary switching element is in the main circuit. As for the second improved topology, it solved most of the problems of the former one except one switching device in the main loop by adding another two assistant switching components. The waveforms of the above two topologies are confirmed by simulation based on Matlab/Simulink. Besides, the second improved topology is applied to the CCC system of a 6/4 SRM to prove that power loss of the proposed one is much less than the traditional one under various running speed for EV. Therefore, the proposed topologies has their potential prospects in the application of EV motor drives.

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Biographies

Jingwei Zhu received his B.S. degree in 2015 in Electrical Engineering & Automation from Zhejiang University, Hangzhou, China.
He joined the department of Electrical Engineering, The Hong Kong Polytechnic University as a postgraduate. His main research interests are in the field of power electronics and motor drives.

K.W.E.Cheng obtained his BSc and PhD degrees both from the University of Bath in 1987 and 1990 respectively. Before he joined the Hong Kong Polytechnic University in 1997, he was with Lucas Aerospace, United Kingdom as a Principal Engineer.
He received the IEE Sebastian Z De Ferranti Premium Award (1995), outstanding consultancy award (2000), Faculty Merit award for best teaching (2003) from the University and Silver award of the 16th National Exhibition of Inventions. Faculty Engineering Industrial and Engineering Services Grant Achievement Award (2006), Brussels Innova Energy Gold medal with Mention (2007), Consumer Product Design Award (2008), Electric vehicle team merit award of the Faculty (2009), Special Prize and Silver Medal of Geneva's Invention Expo (2011) and Eco Star award (2012). He has published over 250 papers and 7 books. He is now the professor and director of Power Electronics Research Centre.