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Overview of the DC Power Conversion and Distribution

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Abstract – The DC distribution is discussed. A comparison of the DC distribution to conventional AC distribution has been made. The alternative method of high frequency AC distribution is addressed. DC distribution can often eliminate conversion stages. New methods of DC-DC power conversion have been reviewed. It can also facilitate the energy storage and enhance the reliability. Its application in electric vehicles is also described. Finally the future development of power electronics is highlighted.

Keywords - Power converter, DC distribution, AC distribution, motor drives, alternative energy, electric vehicle

I. INTRODUCTION

The DC distribution system is an alternative method for delivering power. The method has been proved to have advantages over conventional AC distribution in terms of energy saving, operation and cost. Thanks to the recent development in power electronics, the handling of the DC system including the voltage stepping, switching, DC energy storage is quite mature. In the last two decades, the rapid development in DC-DC power conversion is made in dramatic manner. New topology, analysis and control method have been reported. Therefore it is time to revisit such system and widen the opportunity to develop into a more practical establishment. Most of the electrical parts and systems are DC based. They may accept AC but internally have embedded with an AC-DC converter to obtain the necessary DC. For example, the computer units are derived by low voltage DC such as 3-20V. The motor drive inverter has also a DC link supplied by AC-DC rectifier. Most of the electronic lighting is now embedded with an electronic ballast which is also with a DC link of several hundred volts. The recent popular LED lighting is also a DC based system.

Most energy storage systems such as battery, hydrogen storage and ultra-capacitor are DC devices. Alternative energy sources such as photovoltaic is also DC source. Therefore it is straight forward to use DC distribution for power transfer and power conversion. Another major alternative energy source, wind power, can output DC as well. Fig. 1 shows the configuration. The driver or power converter for the generator has a DC link.

Nowadays, the wind power generation has biased to direct drive because of efficiency and elimination of the mechanical parts. The use of DC link will be advantageous because it allows a buffer stage to convert the variable frequency or low frequency from the generator side through an intermediate stage to the output stage. An inverter (AC-DC) is connected in the AC line using grid connection control. If DC distribution is used, the grid connection inverter can be eliminated.

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The control through joining different DC generator sources in a station is simple because there is no frequency and phase synchronization. DC system is not new. It has been used in office and factory areas for local distribution. It has also been used in aerospace system. This includes aircraft, space, and maritime DC distribution. Obviously the future applications will be moved to consumer level including buildings, home and office.

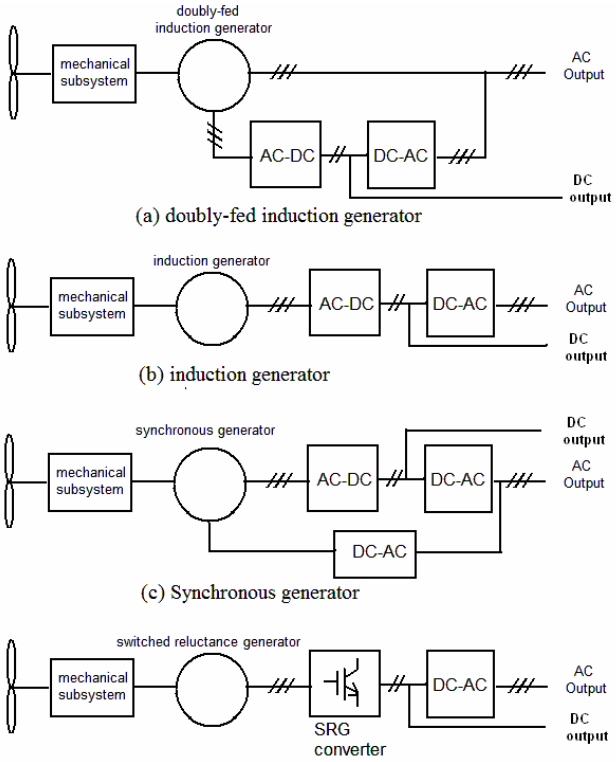


Fig. 1: Wind power energy source

Despite the rapid development in the DC system and power electronics, the development of such DC distribution has still a number of problems to be resolved. These include the fault detection, DC switching, stability, startup and shutdown, overall system issue and cost issue. This paper is focused on low voltage systems rather than the high voltage systems, as the high voltage transmission has been well discussed in many reports and has been used extensively for power cross-country power transmission.

II. DC DISTRIBUTION

A. Previous work on DC distribution

DC distribution network has a number of well-known advantages as compared with the conventional AC distribution. The applications in general buildings [1], maritime shipboard [2] and aerospace environment [3] have been reported. The main reason of not being widely used for the last decade extensively is mainly

economic reasons and partly because of the conservation of engineers. Today, the rapid development of power electronics provides an opportunity of this method because it allows DC conversion to be easily applied. As we know, most energy sources can produce DC voltage, by this; we mean fuel cell, photovoltaic cell and even many generators. Many energy storages these days are also DC, including capacitor, inductor and battery. The use of DC distribution undoubtedly has better cost implication and higher efficiency because of fewer conversion stages. The recent DC to DC power conversion research in the field of power electronics has also given additional favourable method of this DC distribution. The DC distribution has been used successfully in high voltage DC system [4-5] and many micro-distribution systems in electric vehicles [6]. However there are still a number of research difficulties that needs to be tackled before it can be realized for industrial use. The following are some researches reported on this topics:

The low voltage DC distribution has been reported by several researchers recently. The main work on these areas entail the fault detection based on the impedance characteristics [7-8]. This method is based on checking the impedance of individual modules against their specifications. The circuit breakers modeling for the DC distribution system (DDS) based on PSpice [9] has been reported. The model can further be implemented to simulate the whole protection system. The electronic circuit breaker for the DC system has been reported based on the zero-voltage switching [10]. The switch uses auxiliary circuit of RCD snubber for the assistance to the improvement of the switching transient. The switching time of 200μs has been simulated.

The PEBB (power electronics building block) is a concept to provide generic building blocks for power electronics. It has been recently reported [11] for use in DDS. This idea can be extended to the future larger scale DC distribution in buildings and other systems.

The stability study on the DC distribution system has been reported by Logue [12]. The negative incremental impedance can cause stability problems and this is especially important for DC conversion network where the energy storage components such as the passive devices in the distribution line and load side exist and cause unwanted stability problems. Some early study on the load impedance on the stability in the distribution systems has been reported [13]. Some initial studies on the bulk capacitance and the load changes on the stability have been reported [14].

B. EMI for DC distribution

The EMI is also a concern in the DC distribution. There have been many international standards on AC distribution and EMI on various AC systems and DC conversion electronics, however, on the consideration of DC distribution is limited. The proposed standard for 48V rail [15] is an initial step in this direction. Similarly, although there are extensive researches conducted in the EMI properties on DC power conversion, the study on the EMI effect on DC distribution buses has been less thoroughly studied. Ref [16] is the modeling of the interference properties on this topic.

C. Protection and power quality on DC distribution

The use of switched mode for current protection has been reported in [17]. The stabilization of DC distribution is affected by the cable, capacitive load, inductive load and load changes. A controlled auxiliary power through bulk capacitance has been proposed in [18]. A control logic for different operating conditions has also been examined for low voltage DC distribution system [19].

D. The saving in DC distribution

The DC distribution allows saving in cable size, rectifier or AC-DC converter, equipment or appliance materials and package size. The saving in the loss of power processing can also be reduced because the rectifier stage is reduced. For the AC power source related system such as interruptible power supply (UPS), the inverter stage can also be reduced. The following table gives an estimation of the potential saving.

Table 1: Estimation saving using DC distribution

	Size reduction	Power input reduction
Electronic ballast	30%	5%
Motor inverter	30%	4%
Renewable energy system	40%	5%
Distribution	50%	2%
Low power Charger	20%	10%
Video/Audio Entertainment	10%	10%
Computer	15%	8%
Average	25%	4.50%

Other advantages including the audible emission will be eliminated as many equipment or appliances will emit 50/60Hz noise under poor design or aged condition. Further, the quality of the entertainment system will be improved because it is free from interference of mains frequency. The 100/120Hz flickering of many lighting units will also disappear.

III. DC Distribution Versus AC Distribution

A. Conventional low frequency AC

The discussion of the comparison of DC and AC distribution has been made in many literatures in the past. It is obvious that the DC distribution has many advantages over conventional system. The main reason for the unwillingness of change is because the world has adapted to the AC system for many years. The change cannot be sudden and must be made gradually. It is also expected the change should start in a smaller scale such as office or a section of a plant.

B. High frequency AC

Recently there is discussion on the use of high frequency AC distribution. The use of high frequency AC is not new. The aerospace standard has used 400Hz for years because of the reduction of the passive components. Higher frequency has been discussed extensively in recent publications [20-21] in the comparison and switching waveforms. The main advantage of high frequency AC distribution is the reduction of the filter and reactive

components. It also increases the transient response as just a few cycles of reaction time refers to a fraction of ms.

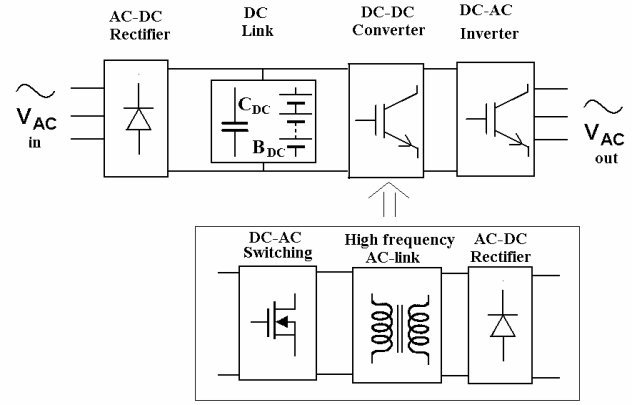


Fig. 2: High frequency AC-link is embedded to DC converter

The DC-DC power conversion uses high frequency AC link for power transfer. There is at least one high frequency transformer or inductor for voltage stepping or temporary energy storage. AC distribution has been used inside most of the DC-DC power conversion. Fig 2 shows the block representation.

For general AC-AC power converter such as variable speed drive (VSD) for motors, if wide voltage variation is needed, DC-DC power converter is also needed. The high frequency AC-link is then also embedded in the unit. It is rational to examine if the high frequency AC-link should be used and how it is compared with the DC link.

Using high frequency AC link will have the same problem of the synchronous of frequency and phase when different voltage sources are added in either parallel or series. The high frequency loss is a factor to be overcome. Therefore, the cable, inductor and transformer design must be properly developed. Care must be taken for skin effect and proximity effect, otherwise, the loss and heating effect in the conductor will cause operation and life time problem [22-24].

C. Health issue

The high frequency AC may generate biological effect to human[25]. The standard [26] has shown that exposure to AC frequency for general public should be less than 10kV/m to 0.4kV/m for electric field and 0.64mT to 0.021mT for magnetic field from 50Hz to 10kHz respectively. The International Commission on Non-Ionizing Radiation Protection (ICNICP) [27] has recommended that the electric and magnetic field should be 10V/m to 610V/m and 0.4A/m to 1.6A/m from 50Hz to 100kHz. The National Radiological Protections Board (NRPB) has also published their guideline on the exposure limits [28]. Tables 1 and 2 shows the comparison of different standards:

Table 1: Exposure limits to electric field for public

	ENV50166-1	ICNIRP	NRPB
50Hz	10kV/m	10kV/m	12.28kV/m
10kHz	0.4kV/m	87V/m	614V/m
100kHz	-	87V/m	614V/m

Table 2: Exposure limits to magnetic field for public

	ENV50166-1	ICNIRP	NRPB
50Hz	0.028mT	0.1mT	2mT
10kHz	0.021mT	6.25μT	0.2mT
100kHz	-	9.2μT	0.06mT

The exposure limit for power frequency (50/60Hz) is high because it carries too little energy in each quantum to break chemical and molecular bonds. The heating effect by the power frequency is very low as compared to the human body's own background rate of heat generation. For high frequency, the innovation effect and other high frequency damage will be increased dramatically and the limit is much lower. However, the actual damage due to power of high frequency is difficult to be studied as it requires an actual model. The long duration exposure under lower than the exposure limits has no established study and it is recommended to avoid consistent contact to such field. Therefore the use of DC may have advantages against the DC distribution for such argument.

IV. DC Distribution in Electric Vehicle

A. The more electric vehicle

Electric vehicle is a good system that shows a combination of different power electronic units. It includes the DC battery system, battery charger, DC-DC power conversion, DC-AC inverter for motor drive as shown in Fig. 3. Fig. 4 shows a typical electric vehicle that has demonstrated the application of power electronics and DC distribution. Each of the unit requires substantial power electronics work. The electric vehicle is not restricted to automobile, other vehicle such as aircraft [29] and or ship [30] has also been examined for DC distribution. The More Electric Aircraft concept has been promoted in the last 2 decades because of the rapid development in power electronics. Many actuation and control system are power electronic driven. The use of DC distribution will enhance power and dynamic performance. The following discusses the recent development in electric vehicle:

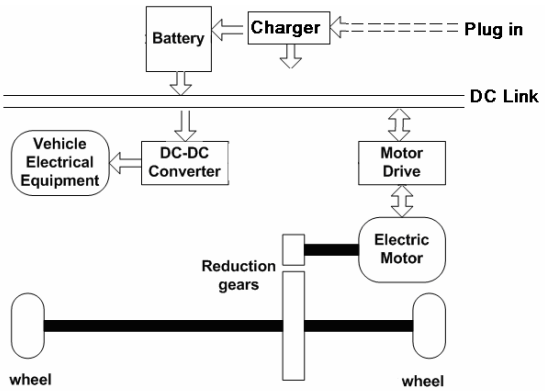


Fig. 3: Typical configuration of electric vehicle

B. DC conversion in vehicle

Electric vehicle is a standalone network and it is using battery as the main power. The hybrid electric vehicle also uses battery as an intermediate stage for electric motor. There are lots of works for DC power conversion

so that the battery voltages can be converted to different levels for equipment.

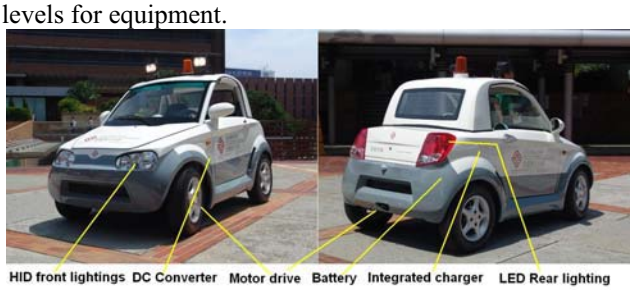


Fig. 4: Electrical vehicle DC system

C. Battery charging and management

The recent development is towards the design for intelligent charging for high performance battery such as Li-ion[31] and battery management system [32]. The battery management should provide battery balancing, determining the State of Charge (SoC) and State of Health (SoH).

The battery charger is actually an AC-DC converter. For low power application, the flyback converter is commonly used because of its low component count; for higher power level such as hundreds of Watt or above, the H-bridge converter is commonly used.

D. Motor drive

The motor drive for electric vehicle is to convert from DC battery to switched waveforms to drive the motor. The DC drive for DC motor is commonly used for low power. The H-bridge converter is used because it provides 4-quadrant control. The induction motor is driven by conventional 3-phase inverter. Commonly, the switched-reluctance motor (SRM) is considered for high performance motor drive. The new SRM is designed using in-wheel method in which the stator is in the center and the rotor is in the outer. An 8/6 motor and the drive is shown in Figs. 5 and 6.

Fig. 5: 8/6 in-wheel motor

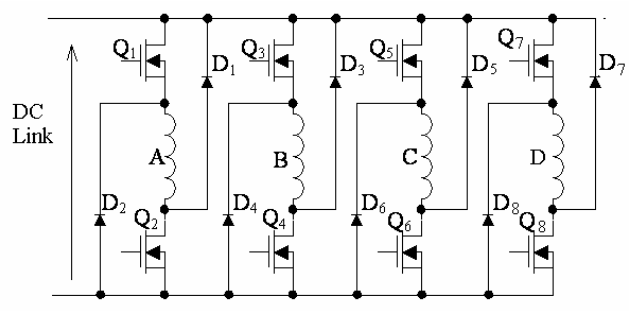


Fig. 6: The SRM drive for 8/6 motor

The in-wheel motor can replace the wheel as shown in Fig 7. The method allows the skid-steering rather than the conventional angle steering as the steering method for tank. The mechanical subsystem including the gear box, clutch, transmission and other actuator and hydraulic system can be eliminated. The saving in heavy and bulky mechanical and hydraulic units will increase the overall efficiency and reduce materials.

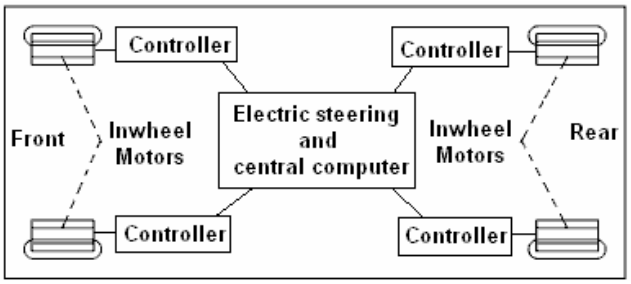


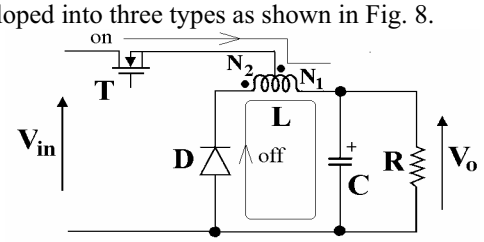
Fig. 7: Four-wheel drivetrain system

V. DC-DC Power Conversion

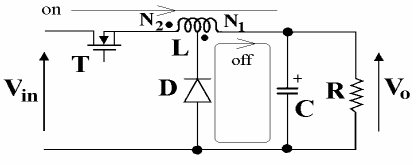
In order to facilitate the application of DC distribution, the use of switched mode power conversion is necessary. For general voltage conversion, the classical topology can be used, for example, the Buck, Boost or Buck-boost. For isolated application, the use of transformer or coupled-inductor circuit topologies is used, for example, flyback converter or forward converter. For high power application, full bridge topology should be used. The typical circuit is phase-shifted converter [33] or load-resonant converter [34]. If soft-switching is needed such that the softer current or voltage is needed to reduce the switching transient, the quasi-resonant [35], extended-period resonant [36] or the resonant transition [33-34] can be used. There are a number of new topologies now available for DC-DC power conversion. They are discussed as follows:

A. Tapped inductor

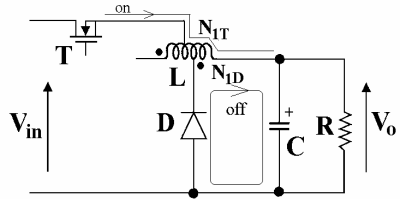
The non-isolated converter can be used for applications of fixed and non-human-contacted equipment or the EMI concern is not an issue. Recently the tapped inductor converter is promoted by [37] because of it's simple in structure and wide voltage conversion range while maintaining high efficiency. The tapped inductor is basically derived form the conventional power converter and allows taps of the inductor to connect to either the transistor or diode or both. This allows a wide range of voltage conversion. For example, a buck converter can be developed into three types as shown in Fig. 8.



(a) Transistor-tapped



(b) Diode-tapped



(c) Transistor-diode-tapped

Fig. 8: Buck tapped inductor circuit

If the tapped ratios k, k_T and k_D are given by:

$$k = \frac{N_1}{N_{12}} \; ; \; k_T = \frac{N_{1T}}{N_{12}} ; \; k_D = \frac{N_{1D}}{N_{12}} \quad (1)$$

where N_{12} is the total number of turns, then, the voltage conversion ratio under continuous mode for each circuit is a function of the duty ratio D and the above k ratios:

$$\frac{V_o}{V_{in}} = \frac{D}{D(1-k)+k} \quad (2)$$

$$\frac{V_o}{V_{in}} = \frac{kD}{1-D+kD} \quad (3)$$

$$\frac{V_o}{V_{in}} = \frac{k_D D}{(1-D)k_T + k_D D} \quad (4)$$

for transistor-tapped, diode-tapped and transistor-diode tapped respectively. The conversion ratio for each circuit has been plotted in Fig 9. It can be seen that the conversion ratio for transistor-diode tapped version covers the conversion ratio from 0 to 1 for any duty ratio. Experimental results has indicated that the converter has high efficiency even under wide conversion ratio.

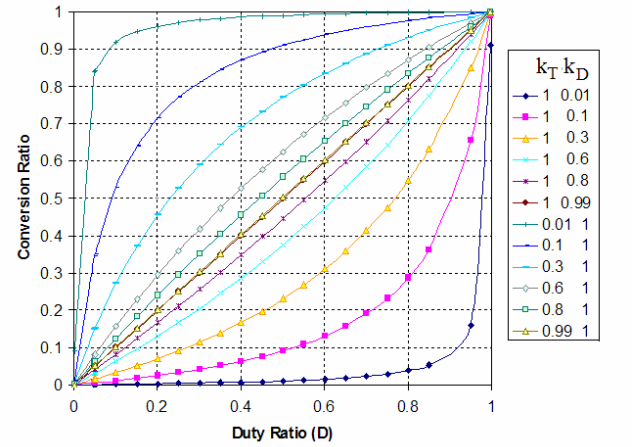


Fig. 9: Voltage conversion ratio for the transistor-diode tapped Buck converter

B. Switched-capacitor

Recently there are a number of discussions on the switched-capacitor resonant converter and its advantages against the conventional switched mode power converter and the classical switched capacitor converter [38-39]. There are comments made in [40-41] that the switched-capacitor resonant converter does not have voltage regulation which is supposed to be the mandatory condition for all power converters. Further, the loss is not related to the component loss characteristics. It is noted that the switched-resonant converter is an improved development of the conventional switched-capacitor converter. The methods [38-39] have quantified the amount of the inductance needed in order to control the resonant property of the converter. The inherit voltage regulation is within 10%. The resonant converter is suitable for applications with less demand on exact voltage regulation such as a DC-DC transformer. The conventional converters [40-42] do have theoretical efficiency independent of components but its practical efficiency is strongly dependent on components.

In the conventional method, the amount of the parasitic inductance is uncontrolled or ignored and therefore the loss due to the switching is also not controlled and the switching loss and noise are resulted. The readers have to consider carefully which method they should use. The comparison is as follows:

Table 3: Comparison of resonant and conventional switched capacitor converters

	Conventional	Resonant
Magnetic components	No magnetic components, use uncontrolled parasitic	Small inductor is needed.
Current stress	High	Low
Number of transistors	Depends on the circuit, usually many especially for high fractional or multiple ratio	Two transistors
Efficiency	Low. Depend on the voltages of switching capacitors, input and output voltages. Practical efficiency is low	Theoretical 100%, practical higher than 90%
Power level	Low power, usually less than 100W	No restriction on power level. Reported power level is more than 1kW.

The new version of the switched–capacitor resonant converter has been reported in many literatures. Fig. 10 shows the family of the converters and its voltage conversion ratio M.

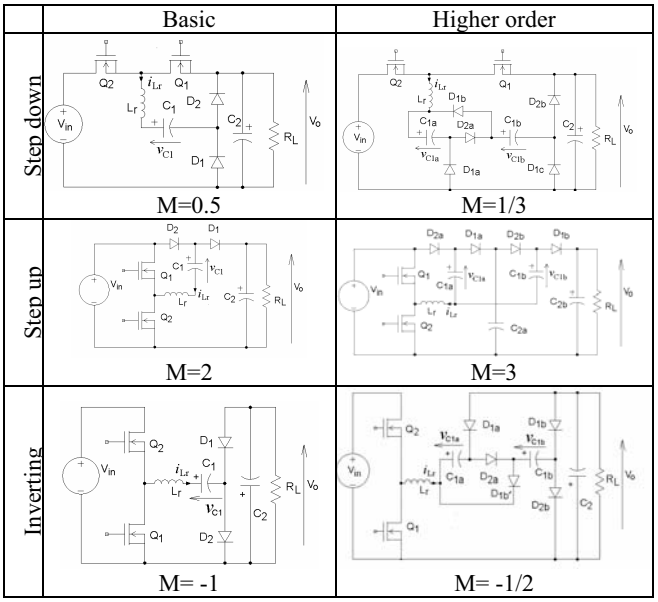


Fig. 10: The family of switched-capacitor resonant converter

Other new development in multiple output and power factor correction can be referred to [43-44].

VI. MAGNETICS

Magnetic device is one of the basic components on DC power conversion because it provides temporary energy storage, isolation and voltage stepping. Besides the development of ferrites and Molydbenum Permalloy Powder (MPP) in the last tens of years, there is no advance development in the magnetic materials. The latest development in magnetics can be reported in the following two areas:

A. Polymer-bonded magnetics

High frequency power conversion usually requires air-gap or distributed air-gap in order to reduce the overall permeability and saturation of ferrites and iron core. The invenion of the polymer-bonded magnetics [45] meets this need; it is directed to a magnetic composition containing a thermoplastic resin and magnetic powders. The new material is to combine resins such as PMMA or PE with magnetic powder taken from Nickel, Cobalt, NiZn Ferrite, and MnZn Ferrite and together with a coupling agent. The new material is shown in Fig 11.

Fig. 11: Different sizes and shapes of polymer-boned magnetic core

The new material has the advantages of non-brittle, flexible shape, lower loss, lower cost and simpler manufacturing procedure. The material can also be recycled as it is plastic based.

B. Coreless transformer

At very high frequency operation, the permeability of the magnetic core of the transformer can be reduced and at some stage, an air-core can be used [46-47]. At present, as the switching frequency cannot be moved to several or tens of megaHetz, the operation frequency of air-core transformer based power converter has been reduced slightly. For air core transformers, self-resonance can be used to minimize the magnetizing current in the external circuit.

VII. FUTURE POWER ELECTRONICS FOR DC

Power electronics provides simple and higher efficiency power processing for DC-DC operation. The future development of DC power electronics will have the following trends:

A. Energy saving and environment

Energy saving and development of new energy are the most important global concern. Power electronics provides efficient power processing methodologies. Today, power electronics has been used in many alternative energy sources. Power electronics has found its application in wind power generation, photovoltaic, energy storage, hydropower, and power quality compensation. It can also be seen that higher power circuit topologies and devices are being further developed for demanding applications.

B. New switching devices

Power electronics heavily depends on the power devices. The rapid development in power electronics is partly because of the new devices. The higher speed, low on-state resistance or voltage, capability of handling high power are the trend of the last 20 years' development in switching devices. In 80's Mosfet, IGBT, MCT are popular devices and are still popular. In recent years, integrated gate-commutated thyristor (IGCT) is available with forward and reverse blocking features. The successful development of IGBT is replacing Gate turn-off thyristor (GTO). Silicon Carbide (SiC) is the large bandgap (3eV) material device and is now believed to bring power electronic device to higher performance. [48-50]. It provides all the above good performance as well as high junction temperature. Its thermal conductivity is good (5W/cm°C)[50]. Gallium Nitride (GaN) is also considered for power switching device. It has higher bandgap (3.4eV) and good thermal conductivity of over 1.3 W/cm°C. It is expected that the new devices will bring new revolution of power electronics.

C. New materials and passive devices

Power electronics strongly depends on passive components, which are also affected by new devices. The development of ferrites provides a new method of temporary energy storage, maintaining high efficiency of more than 99% in the magnetic devices. Higher saturation level and lower loss in hysteresis, eddy current and residual losses are needed. The new magnetic material such as polymer bonded magnetic device has proved to be efficient at high frequency. The use of CoNiFe alloy has been reported [52]. Recent devices such as ultra-capacitors allow high energy density and reduce transients which affect the battery life time. Higher temperature magnetic energy storage is also expected to provide new opportunity and application of power electronics.

D. Standards and safety

International standard is usually addressed to safety and creating a balance among different parties. Over the years, a number of new standards such as EMC and energy saving guidelines have forced power electronics to work in new methods. For example the Restriction on Hazardous Substances (RoHS) [53] which came into force on 1 July 2006, has changed the manufacturing and components procurement for all the power conversion design and production.

E. Cross disciplines

Power electronics is a supporting technology. Besides power processing, power electronics has found new applications in medical electronics, automotives, lightings and building services. It is clear that any discipline or technology that requires power and motion control is likely to work with power electronics to improve the overall performance in size, stability and dynamic performance.

F. Integration

The demand by intelligence and high power density is a development trend. There are intelligent power modules (IPM) that integrate the gate drive and protection into power devices. It simplifies application design of the power stage of the motor drive, inverter and power converter. Intelligent power electronics module (IPEM) that integrates the power electronics circuit with sensors and controllers has been reported [54]. The integration of magnetics into power devices [52] is also a trend. The integration of the power electronics into motors and batteries is developing. The in-wheel motor shown in Section IIB is a step of integration of intelligent motor. Another example is the embeddedment of battery management system (BMS) and voltage regulation into the battery.

VIII. Conclusion

An overview of the DC-DC power conversion is given. The paper discussed the recent development in DC-DC power converters, DC distribution, DC driven motor, electric vehicle and magnetics. A number of new converters including the tapped and switched-capacitor have been discussed. It outlines the major differences between new converters and conventional converters. The DC distribution and the AC distribution have also been compared. The paper finally summarises the latest power electronics applications, discusses the present development in DC power electronics and provides a future direction of the DC power conversion.

Acknowledgment

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BIOGRAPHY

K.W.E.Cheng obtained his BSc and PhD degrees both from the University of Bath in 1987 and 1990 respectively. Before he joined the Hong Kong Polytechnic University in 1997, he was with Lucas Aerospace, United Kingdom as a Principal Engineer and led a number of power electronics projects.

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An Efficient Switching Algorithm for the Implementation of Synchronous Space Vector Modulation for an Induction Motor Drive with (V/f) Control

K.A.S. Mallikarjuna Rao[1] Sunita Nadampalli[2] V.T. Somasekhar[3]

Abstract – In this paper, an improvisation to an existing switching algorithm is described for the implementation of synchronized space vector modulation for a 3-phase, 2-level VSI driven induction motor with V/f control. A useful corollary is derived for this specific situation from an existing general algorithm. This corollary considerably alleviates the computational burden on the digital controller. The reduction of the computational time to determine the switching times of individual phases of the inverter is obtained by employing an appropriately devised lookup table. The elegance of the improvised algorithm lies in the fact that the elements of the lookup table could be employed for any modulation index, when the inverter is operated in the region of linear modulation. The proposed algorithm is experimentally implemented on a TMS 320F243 DSP platform and the results are presented.

Keywords – Two-level inverter, space vector modulation, induction motor drive, V/f control, effective time.

I. INTRODUCTION

Figure 1 shows a 3-phase, 2-level voltage source inverter (VSI). Owing to its simplicity and ruggedness, it has become a natural choice in various AC drives. With the advancements in the Pulse Width Modulated (PWM) control schemes, the harmonic spectrum of the output voltage can be maneuvered to contain a pronounced fundamental component and to transfer the harmonic energy to the components of higher frequency. This is desirable, as it is relatively easier to filter out the components of higher frequency.

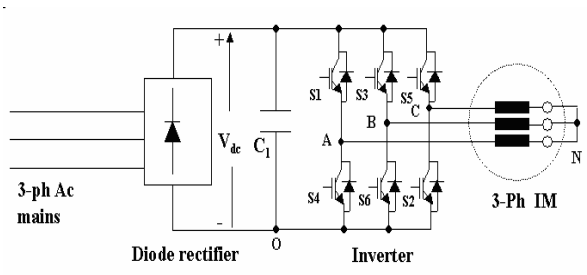

Fig.1: A conventional Induction motor drive with 2-level inverter

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Several PWM scheme are reported in the literature [1-12], of which the sine-triangle PWM (SPWM) and the space vector modulation (SVM) have aroused a particular interest in academia as well as in practicing engineers. Of these two modulation schemes, SVM yields a superior spectral performance [4]. Also SVM enhances the DC bus utilization by about 15% compared to SPWM [4]. Several methods to implement SVM are reported in the literature.
In SVM, the instantaneous reference phase voltages (denoted as v_a^*, v_b^* and v_c^*) are converted into a corresponding space vector v_{sr} defined as:

$$v_{sr} = v_a^* + v_b^* e^{j2\pi/3} + v_c^* e^{-2\pi/3} \quad (1)$$

The reference space vector v_{sr} is expressed in rectangular form as:

$$v_{sr} = v_\alpha + jv_\beta \quad (2)$$

It is expressed in the polar form as:

$$v_{sr} = |v_{sr}| \angle \theta \quad (3)$$

where

$$|v_{sr}| = \sqrt{v_\alpha^2 + v_\beta^2} \text{ and } \theta = \tan^{-1}(\frac{v_\beta}{v_\alpha}) \quad (4)$$

The quantities v_{sr} , v_α , v_β and θ are shown in Fig 2. A three phase, 2-level VSI is capable of assuming 8 states. Of these, six states allow power transfer from the DC-link to AC side. Hence they are called the active states. The other two states are termed as null states, as all the three phases on the AC side are short circuited either to the positive bus or to the negative bus. Consequently, there is no power flow from the DC-link to the AC side. The null vectors are located at the center of the hexagon. The switching states corresponding to each vertex are also shown in Fig.2. For example, the state-1 is identified as (+ - -). This means that for this state the top switch in phase-A leg (S_1 in Fig.1) is turned on so that the output terminal of phase-A is connected to the positive bus of the DC-link. Similarly, the phase-B and phase-C terminals are connected to the negative bus of the DC-link by turning on the switches S_6 and S_2 in state '1'. From Fig..2 it is evident that the hexagon is subdivided into six identical sectors. The central theme of SVM is to synthesize the reference voltage space vector v_{sr} in the average sense with the eight states offered by the inverter, using the criterion of volt-second balance.

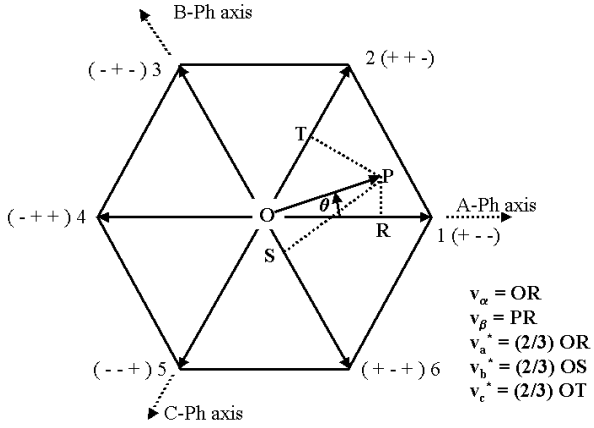

Fig. 2: Space vector diagram of a 3-ph, 2-level inverter

To this end, the instantaneous reference phase voltages are sampled at regular intervals. The sampling time period is denoted as T_s. The modulation index, denoted as m_i, is defined as:

$$m_i = \frac{|v_{sr}|}{V_{dc}}$$

where V_{dc} is the DC-link voltage.

The time intervals T_{ga}, T_{gb} and T_{gc} respectively denote the time periods for which the corresponding phase terminal is connected to the positive bus. For the rest of the paper, they are referred as the 'inverter-leg switching time periods'.

In conventional method of implementing SVM, the sector in which the tip of the reference space vector is situated is first determined. Using the criterion of the volt-second balance, the periods corresponding to the switching of the active vectors along the leading edge (denoted as T_1 and T_2 respectively) of that sector during that sampling time period are then determined [4]. There exists an exclusive relationship between the active vector switching time periods (T_1 and T_2) and the inverter leg switching time periods (T_{ga}, T_{gb} and T_{gc}) in a given sector. Using these relationships the time periods T_1 and T_2 are translated into the gating signals of the individual inverters. This method is thus cumbersome and time consuming. Reference [13] describes an elegant switching algorithm, which uses only instantaneous phase reference voltages to implement SVM. For the rest of this paper this algorithm is referred as the 'Kim-Sul, algorithm, in the honor of its inventors. In the following section, the Kim-Sul algorithm is briefly reviewed.

II. THE KIM-SUL ALGORITHM

As stated earlier, this algorithm operates only with the instantaneous reference voltages. The elegance of this algorithm lies in the fact that sector identification is not required to implement the SVM and the generation of gating signals is automatically accomplished.

In sector1, the switching periods for the active vectors T_1 and T_2 may be expressed in terms of the instantaneous values of the reference phase voltages v_a^*, v_b^* and v_c^* as [13]:

$$T_1 = \frac{T_s (v_a^* - v_b^*)}{V_{dc}}; \qquad T_2 = \frac{T_s (v_b^* - v_c^*)}{V_{dc}} \tag{5}$$

The switching time periods proportional to the instantaneous values of the reference phase voltages, termed imaginary switching times, are defined as [13]

$$T_{as} = \left(\frac{T_s}{V_{dc}}\right) v_a^*; T_{bs} = \left(\frac{T_s}{V_{dc}}\right) v_b^*; T_{cs} = \left(\frac{T_s}{V_{dc}}\right) v_c^* \tag{6}$$

From (1) and (2) the active vector switching times T_1 and T_2 in sector1 may be expressed as:

$$T_1 = T_{as} - T_{bs} \;;\; T_2 = T_{bs} - T_{cs}; \tag{7}$$

Extending this procedure for the other sectors, the active vector switching times T_1 and T_2 for the respective sectors may be expressed in terms of the imaginary switching times T_{as}, T_{bs} and T_{cs} for a particular sampling time period. The effective time T_{eff} is the time during which the active vectors are switched in a sector and is given by $(T_1 + T_2)$. This may be determined as the difference between the maximum and minimum values among T_{as}, T_{bs} and T_{cs}. The time duration T_o is the time for which a null vector is applied, may be obtained from T_1 and T_2 as:

$$T_o = T_s - (T_1 + T_2) = (T_s - T_{eff}) \tag{8}$$

where

$$\begin{aligned} T_{eff} &= \max\{T_{as}, T_{bs}, T_{cs}\} - \min\{T_{as}, T_{bs}, T_{cs}\} \\ &= T_{\max} - T_{\min} \end{aligned} \tag{9}$$

The offset time, T_{eff} required during a given sampling time period to distribute the null vector symmetrically at either end of the effective time period with half the duration $(T_o/2)$ each (or place the effective time period exactly at the center of the sampling time period) is given by [13]:

$$T_{offset} = (T_o/2) - T_{\min} \tag{10}$$

The actual switching times for each inverter leg can be obtained by the time shifting operation as follows:

$$\begin{aligned} &T_{ga} = T_{as} + T_{offset}; T_{gb} = T_{bs} + T_{offset} \\ &T_{gc} = T_{cs} + T_{offset} \end{aligned} \tag{11}$$

To achieve minimum switching, the vectors are switched in the sequence 8-1-2-7 with the time duration of $T_o/2 - T_1 - T_2 - T_o/2$ for one sampling time duration and in the sequence 7-2-1-8 during the next sampling time period, when tip of the reference vector is in sector 1. The former sequence is called the 'ON' sequence and the later sequence is called 'OFF' sequence. These two sequences are alternatively used. Since the time periods T_{gx} (x = a,b,c) denote the time duration for which a given phase is connected to the positive bus, transitions occur in the

respective phases after the time duration of T_{gx} from the beginning of the sampling time period for all the samples with 'OFF' sequence. However for the 'ON' sequence, transitions occur in respective phases after T'_{gx} (x = a,b,c) from the beginning of the sampling time period where

$T'_{gx} = T_s - T_{gx}$ (x = a,b,c)

The procedure outlined in the previous paragraphs is graphically depicted in Fig.3, assuming that the sample is situated in sector-1.

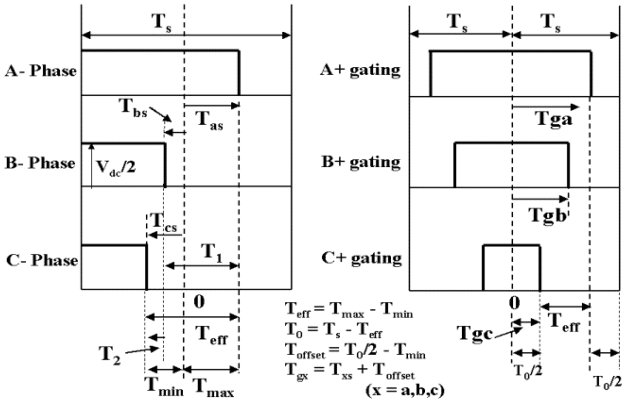

Fig. 3: Implementation of the space-phasor modulation scheme using the instantaneous values of the ref. phase voltages – v_a^*, v_b^* and v_c^*.

III. The Proposed Algorithm

A. The Algorithm

With synchronized PWM, a fixed number of samples are used for any fundamental frequency. This is achieved by making T_s as a variable. This would ensure that the location of the first sample of the previous cycle and the location of the first sample of the current cycle are exactly aligned. Assuming that the reference phase voltages are sampled n_{sam} times in the fundamental cycle which has a time period T,

$$T_s = \frac{T}{n_{sam}} = \frac{1}{f n_{sam}} \tag{12}$$

where f is the frequency of the fundamental component. A very useful simplification results if the inverter is operated with synchronized SVM and the induction motor is driven with V/f control. The expressions for the imaginary switching times T_{as}, T_{bs} and T_{cs} are reproduced below for an easy reference.

$$T_{as} = \left(\frac{T_s}{V_{dc}}\right) v_a^*; T_{bs} = \left(\frac{T_s}{V_{dc}}\right) v_b^*; T_{cs} = \left(\frac{T_s}{V_{dc}}\right) v_c^* \tag{13}$$

Substituting equ. (8) in equ. (9)

$$T_{as} = \left(\frac{1}{n_{sam} V_{dc}}\right)\left(\frac{v_a^*}{f}\right); T_{bs} = \left(\frac{1}{n_{sam} V_{dc}}\right)\left(\frac{v_b^*}{f}\right);$$

$$T_{cs} = \left(\frac{1}{n_{sam} V_{dc}}\right)\left(\frac{v_c^*}{f}\right) \tag{14}$$

when the induction motor is operated with V/f control and the inverter is modulated with Synchronous SVM, the imaginary switching times remain the same in the range of linear modulation for various modulation indices. This is because:

- When the inverter is operated with Synchronized SVM, n_{sam} is constant.
- When the induction motor is operated with (V/f) control the quantities enclosed in braces namely

(V_a^*/f), (V_b^*/f) and (V_c^*/f) remain constant irrespective of the modulation index in the range of linear-modulation. Hence for a given space angle of space vector θ, irrespective of the value of modulation index the following statements are true when the inverter is operated in the range of linear modulation:

- T_{as}, T_{bs} and T_{cs} are constant.
- $T_{\max}$ and $T_{\min}$, the maximum and minimum values among T_{as}, T_{bs} and T_{cs} respectively are constant. This observation is based on the fact that T_{as}, T_{bs} and T_{cs} are phase shifted by 120^0 with respect to each other as v_a^*, v_b^* and v_c^* are thus phase shifted.
- $T_{eff} = T_{\max} - T_{\min}$, the effective time is constant.

The above observations may be used to derive a useful corollary to simplify Kim-Sul algorithm.

According to Kim-Sul algorithm, T_o (Null state period) =

$T_s - T_{eff}$ and T_{offset} (Offset period) $= \frac{T_o}{2} - T_{\max}$

$$T_{offset} = \left(\frac{T_s - T_{eff}}{2}\right) - T_{\min} = \frac{T_s}{2} - \left(\frac{T_{\max} - T_{\min}}{2}\right) - T_{\min}$$

$$T_{offset} = \frac{T_s}{2} - \left(\frac{T_{\max} + T_{\min}}{2}\right) \tag{15}$$

Hence the inverter-leg switching time period for the A-phase i.e. T_{ga} is given by $T_{ga} = T_{as} + T_{offset}$ and the substitution of eqn.15 yields

$$T_{ga} = \frac{T_s}{2} + \left\{ T_{as} - \left(\frac{T_{\max} + T_{\min}}{2} \right) \right\} \tag{16}$$

Hence

$$T_{ga} = T_{const\_a} + \frac{T_s}{2} \tag{17}$$

for OFF sequence.

However, as explained in section-2, during the 'ON' sequence

$$T_{ga} = T_s - T_{ga} = T_{const\_a} - \frac{T_s}{2} \tag{18}$$

for ON sequence

where

$$T_{const\_a} = T_{as} - \left(\frac{T_{\max} + T_{\min}}{2} \right) \tag{19}$$

T_{const_a} is defined as that component of actual switching time (T_{ga}) that is independent of modulation index and only depends on space angle (θ) of space vector. Similarly, T_{const_b} and T_{const_c} are defined as that component of actual switching times (T_{gb} and T_{gc}) which are independent of modulation index and only depend on space angle (θ) of space vector.

B. Relation between T_{const_a}, T_{const_b} and T_{const_c}

As T_{as}, T_{bs} and T_{cs} are directly proportional to v_a^*, v_b^* and v_c^* respectively, T_{as}, T_{bs} and T_{cs} can be represented as three vectors which are displaced in phase by 120˚ with each other like v_a^*, v_b^* and v_c^*. From the Fig. 2 it is evident that, after affecting a phase shift of $\pm$120˚ or $\pm$240˚, the positions of vectors interchange among them. Hence, $T_{\max}$ and $T_{\min}$, which are defined as maximum and minimum among T_{as}, T_{bs} and T_{cs} remain constant after $\pm$120˚ and $\pm$240˚ of phase shift.

The above observation can be represented in equations as:

$$T_{\max}(120^0 + \theta) = T_{\max}(240^0 + \theta) = T_{\max}(\theta) \tag{20}$$

$$T_{\min}(120^0 + \theta) = T_{\min}(240^0 + \theta) = T_{\min}(\theta) \tag{21}$$

From Fig.4 it can be observed that

$$T_{bs}(\theta) = T_{as}(240^0 + \theta) \tag{22}$$

$$T_{cs}(\theta) = T_{as}(120^0 + \theta) \tag{23}$$

From equation (19)

$$T_{const\_a}(120^o + \theta) = T_{as}(120^0 + \theta) - [\{(T_{\max}(120^o + \theta) + T_{\min}(120^o + \theta)\}/2]$$

From equations (20), (21) and (23)

$$T_{const\_a}(120^o + \theta) = T_{cs}(\theta) - \{T_{\max}(\theta) + T_{\min}(\theta)\}/2 = T_{const\_c}(\theta) \tag{24}$$

From equation (19)

$$T_{const\_a}(240^o + \theta) = T_{as}(240^o + \theta) - (T_{\max}(240^o + \theta) + T_{\min}(240^o + \theta))/2$$

From equations (20), (21) and (22)
i.e.

$$T_{const\_a}(240^0 + \theta) = T_{bs}(\theta) - (T_{\max}(\theta) + T_{\min}(\theta))/2 = T_{const\_b}(\theta) \tag{25}$$

Hence T_{const_a}, T_{const_b} and T_{const_c} are phase shifted by 120˚. A variable T_{const} is defined as that component of actual switching time (T_{ga}), which is independent of modulation index and only depends on phase angle (θ) of space vector. Equations (26), (27) and (28) express T_{const_a} , T_{const_b} and T_{const_c} in terms of T_{const} .

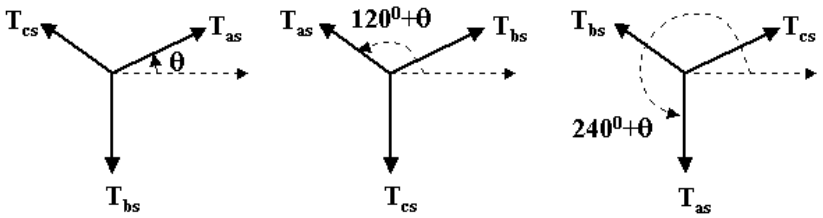

Fig. 4: Phasor diagram of T_{as}, T_{bs} and T_{cs}

$$T_{const\_a}(\theta) = T_{const}(\theta) \quad (26)$$

$$T_{const\_b}(\theta) = T_{const}(240^0 + \theta) \quad (27)$$

$$T_{const\_c}(\theta) = T_{const}(120^0 + \theta) \quad (28)$$

In synchronized SVM, the numbers of samples are constant irrespective of frequency. Hence the space angle 'θ' takes a fixed set of values. The values of T_{const} at those fixed values can be computed offline. By a simple addition or subtraction of the value of $\frac{T_s}{2}$ depending on the sequence to T_{const}, one can obtain actual switching time to a-phase. As actual switching times are phase shifted by 120º, actual switching times of the other two phases can also be determined.

From the above discussion, it is evident that the Kim-Sul algorithm can be further simplified when the inverter is operated with synchronized SVM and the induction motor with (V/f) control.

The Modified Kim-Sul algorithm can formally be stated as follows:

- Off-line calculation of T_{const} values of the output voltage at the prefixed values of θ and storing these values in the form of an array.
- Calculation of T_{ga} by simply adding $T_s/2$ to T_{const} for OFF sequence.
- Calculation of T_{ga} by simply subtracting $T_s/2$ from T_{const} for ON sequence.
- Calculation of T_{gb} and T_{gc} by accessing the elements from the T_{const} array, which are phase shifted by $(+240^0)$ and $(+120^0)$ respectively (Fig.4).

IV. Experimental Results and Discussion

A 3-ph, 2-level inverter controlled by the proposed algorithm has been implemented on a TMS320F243 DSP platform. A (V/f) controlled induction motor drive is considered for experimentation. The induction motor rating is 5HP, 415 V (line-line).

The time period of the fundamental component of the motor phase voltage is divided into 48 samples irrespective of the time period. This means that the angular difference between successive samples is 7.5^0 (i.e. $360^0/48$).

The radius of the biggest circle that can be inscribed in the hexagon shown in Fig.2 corresponds to the limit of linear modulation. With (V/f) control, this operating condition would also correspond to the operation with rated frequency. From Fig. 2 it is evident that this operating condition corresponds to the case wherein the magnitude of the reference voltage space vector, denoted by $|\mathbf{v_{sr}}|$, is equal to $\sqrt{\frac{3}{2}}V_{dc}$. At any other magnitude of $|v_{sr}|$ lesser than $\sqrt{\frac{3}{2}}V_{dc}$, the frequency of the fundamental component is linearly related to the rated frequency.

The required DC-link voltage should be such that, the inverter outputs the rated peak phase voltage corresponding to the case when $|v_{sr}| = \sqrt{\frac{3}{2}}V_{dc}$. For an induction motor with a rated phase voltage of 230V (RMS), the peak voltage is 325V (i.e. $\sqrt{2}$ *230V).

Hence the required DC link voltage is given by:

$$\left(\frac{2}{3}\right)\sqrt{\frac{3}{2}}V_{dc} = 325 \text{ or } V_{dc} = 563\text{V} \quad (29)$$

In equation (29), the factor (2/3) arises from the fact that the length of the space vector is (3/2) times the peak of the individual phase voltages.
From the above discussion it is evident that the operating frequency (f_0) and the time period (T_0) of the fundamental component for a given modulation index are given by:

$$f_0 = \frac{v_{sr} * 50}{\left(\frac{\sqrt{3}}{2}\right) * V_{dc}} Hz \Rightarrow T_o = \frac{1}{f_o}$$

$$\text{i.e. } T_0 = \frac{\left(\frac{\sqrt{3}}{2}\right) * V_{dc}}{(v_{sr} * 50)} \quad (30)$$

As there are 48 samples per cycle, the time per one sample i.e. sampling time period (T_s) is given by:

$$T_s = \frac{T_o}{48} = \frac{\left(\frac{\sqrt{3}}{2}\right) * V_{dc}}{(|v_{sr}| * 50 * 48)} \quad (31)$$

A. *Experimental results with m_i =0.4 (40% modulation)*

The experimental waveform of the pole voltage (v_{AO}), the common-mode voltage content of the pole voltages (dropped across the AC-neutral point 'N' and the point 'O' in Fig. 1) and the phase voltage (v_{AN}) of the 3-phase two-level inverter operated in linear modulation (40% modulation) are shown in Fig. 5a, 5b and 5c respectively. The maximum phase voltage is given by $\frac{2}{3} * V_{dc}$ i.e. (0.667*563) = 376V.

The experimental results confirm this assertion, as is evident from Fig. 5. Fig. 6a shows the sample averaged 'T_{ga}' waveform applied to A-phase leg of the inverter for 40% modulation operation. It may be noted that it resembles that of the sample averaged pole voltage (v_{AO}). The time period of this waveform corresponds to the one given by equation 30. Substituting $|v_{sr}| = 0.4V_{dc}$ in eqn. 30, one gets T_o = 43.3 ms. The experimental result, reinforce this assertion. Fig. 6b shows the waveforms of v_α and v_β, corresponding to the case of linear-modulation. As one might expect, these waveforms are sinusoidal, phase shifted to each other by 90^0. Fig. 6c shows the locus of the tip of the reference vector in the $\alpha - \beta$ plane, corresponding to this case.

B. Experimental results for Over-modulation

The experimental waveform of the pole voltage (v_{AO}), the common-mode voltage content of the pole voltages (dropped across the AC-neutral point 'N' and the point 'O' in Fig. 1) and the phase voltage (v_{AN}) of the 3-phase two-level inverter corresponding to the case of over-modulation are shown in Fig. 7a, 7b and 7c respectively. Whenever the tip of the reference vector **OP** is situated outside the hexagon shown in Fig. 2, the imaginary switching times T_{as}, T_{bs} and T_{cs} are so adjusted as to bring the revised sample on to the periphery of the hexagon. Whenever it is detected that the null time duration $T_o < 0$, it is forced to zero and the values of the imaginary switching times are readjusted following the procedure described in [13]. In this case, the values to be loaded into the counters of the DSP are directly read from a *separate* lookup table, corresponding to the case of over-modulation. Fig. 8a shows the sample averaged 'T_{ga}' waveform applied to A-phase leg of the inverter for over-modulation. The inverter operates with a constant frequency of 50Hz, as the frequency is clamped to the rated frequency if the inverter operates in the region of over-modulation. Fig.8b shows the waveforms of v_α and v_β, corresponding to the case of over-modulation. As one might expect, these waveforms are non-sinusoidal, though they are phase shifted to each other by 90^0. Fig. 8c shows the locus of the tip of the reference vector in the $\alpha - \beta$ plane, corresponding to this case. The waveforms of v_a, v_β for a modulation index of 93% (i.e. $|v_{sr}| = 0.93V_{dc}$) are shown in Fig. 9a. In this case, the tip of the reference vector is partly situated within the hexagon shown in Fig. 2, resulting in the circular part of the locus and partly on the periphery of the hexagon. The samples situated within the hexagon are synthesized by switching two active vectors in the nearest proximity and two null vectors (with the redundancy of the null states) resulting in the circular part of the locus as $T_o > 0$ in this case. However, for the samples situated outside the hexagon, $T_o < 0$. Since it is impracticable to have a negative value for the switching period of the null vector, it is forced to zero filling the entire sampling time period with the effective time interval, T_{eff} [13]. This means that in the latter case, only the two active vectors situated in the nearest proximity to the tip of the reference vector. Thus, the tip of the reference vector is forced to lie in the periphery of the hexagon as demonstrated in Fig. 9b.

C. Advantage with the proposed corollary

As mentioned earlier, a corollary to the Kim-Sul algorithm for the implementation of space vector modulation is derived in this paper. This corollary is applicable for the case of under-modulation, when the induction motor is operated with v/f control. The proposed corollary is based on the observation that the imaginary switching times T_{as}, T_{bs} and T_{cs} remain unaltered for a given θ, even though the modulation index is varied in the aforementioned condition. Instead of computing the imaginary switching times T_{as}, T_{bs} and T_{cs} online, the corresponding values of T_{const} are computed offline and are stored in a lookup table (Table-1 for an easy reference). To this value, the value of $T_s/2$ is either added or subtracted, depending on the sequence to be implemented to directly generate the gating waveforms of the individual devices. For over-modulation, a separate lookup table is employed (Table-2), with the amendment suggested in [13]. In other words, if the sample is situated within the hexagon shown in Fig. 2, the inverter leg switching timings T_{ga}, T_{gb} and T_{gc} are computed using T_{const} obtained by reading off Table-1, while they are read off the Table-2, if they are situated outside the hexagon. Fig. 10 shows the reduction in the time of computation with the proposed modification. To discern the difference clearly, the computation time is increased by a factor of eight by introducing 8 wait states between each instruction of the interrupt subroutine. The time period between each interrupt is equal to the sampling time period. The time periods for a given sample are computed one sampling time period ahead, i.e. the periods calculated in the current sampling time are implemented in the subsequent sampling time interval. The upper trace of Fig. 10 shows the time of computation with the proposed corollary, while the lower trace shows the time of computation with the conventional Kim-Sul algorithm. From the top trace, it may be noted that the time of computation is 50μs with the proposed modification, while it is about 80μs with the conventional Kim-Sul algorithm. This means that the actual times of computation are $1/8^{th}$ of these timings as 8 wait states are deliberately introduced between each instruction to measure these time periods accurately. The experimental condition corresponds to the modulation index of 0.8, for which the sampling time period is 451μs (eqn.31). From the above figure it is evident the computation has become faster by a factor of (80-50)/80, i.e. by about 37%.

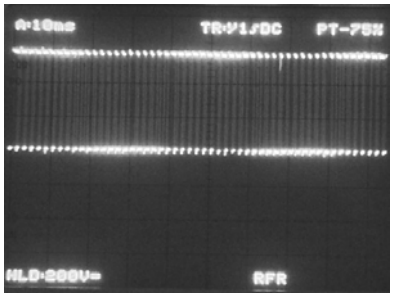

Fig. 5a: Experimental waveform of the pole voltage (Scale: time axis: 10ms/div, Voltage axis: 200V/div.)

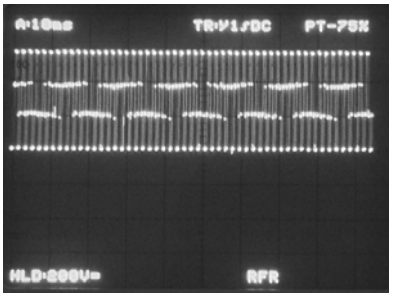

Fig. 5b: Waveform of the common-mode voltage (Scale: time axis: 10ms/div and Voltage axis: 200Vdiv.)

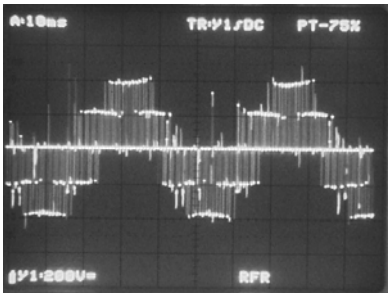

Fig. 5c: Experimental waveform of the phase voltage (time: 10ms/div and Voltage: 200V/div.)

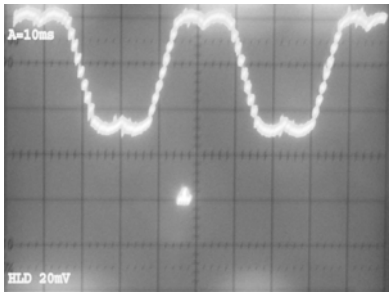

Fig. 6a: The waveform of sample averaged T_{ga} at a modulation index of 40% (Time axis: 10ms / div.)

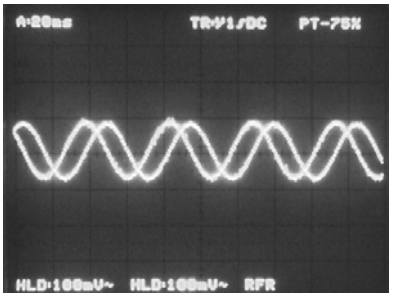

Fig. 6b: The waveforms of v_a and v_β at a modulation index of 40% (Time axis: 20ms / div.)

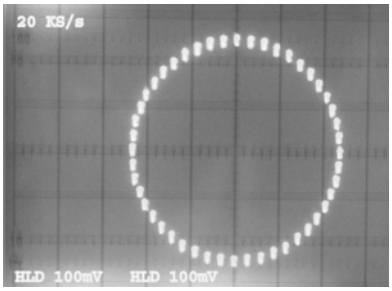

Fig. 6c: The locus of the tip of the reference vector at a modulation index of 40%

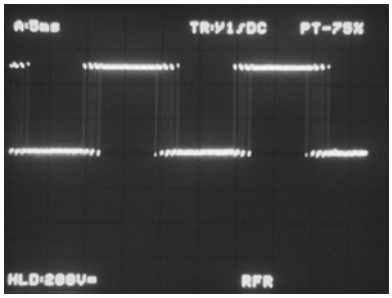

Fig. 7a: Waveform of the pole voltage for over-modulation (Scale: time axis: 5ms/div and Voltage axis: 200V/div.)

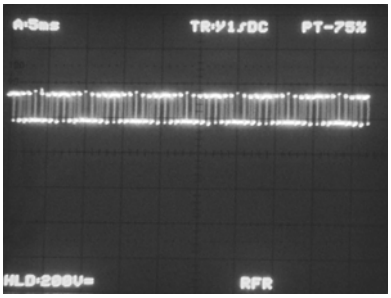

Fig. 7b: Waveform of the common-mode voltage for over-modulation (Scale: time axis: 5ms/div and Voltage axis: 200V/div.)

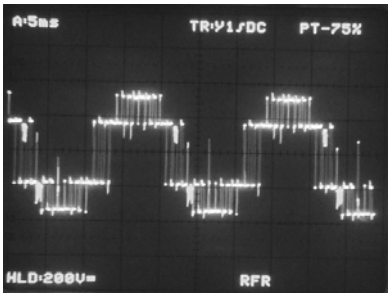

Fig. 7c: Waveform of the phase voltage for over-modulation (Scale: time axis: 5ms/div and Voltage axis: 200V/div.)

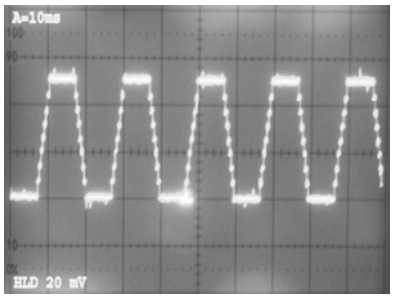

Fig. 8a: The waveform of sample averaged T_{ga} for over- modulation (Time axis: 10ms / div.)

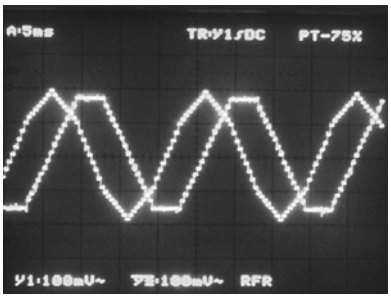

Fig. 8b: The waveforms of v_a and v_β for over-modulation (Time axis: 5ms / div.)

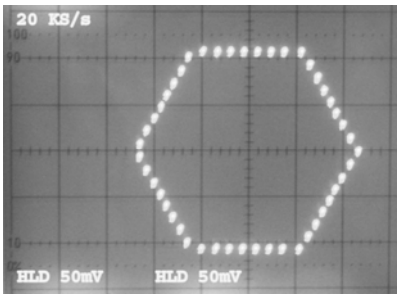

Fig. 8c: The locus of the tip of the reference vector for over-modulation

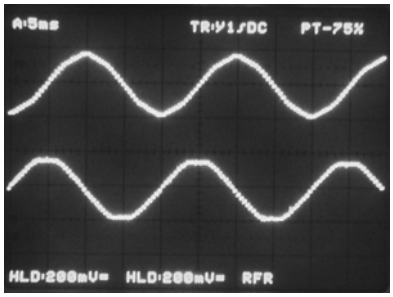

Fig. 9a: The waveforms of v_α and v_β at a modulation index of 93% (x-axis: 5ms /div)

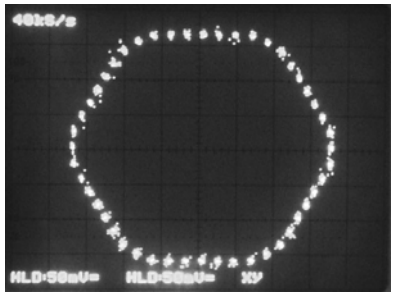

Fig. 9b: The locus of the tip of the reference vector at a modulation index of 93%

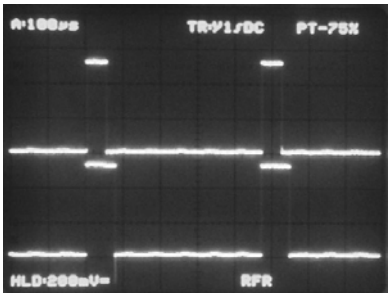

Fig. 10: The time of execution with the proposed corollary (upper trace) and with the conventional algorithm (lower) (Time scale: 100µs/div)

V. Conclusion

In this paper, a corollary to the Kim-Sul algorithm is derived, which is useful in implementing the synchronized SVM for a 3-phase, 2-level inverter driving an induction motor with (V/f) control. This corollary reduces the computational overhead on the digital controller by about 37%. An elegant lookup table is devised, which could be used for any modulation index, while the inverter is operated within the range of modulation. The Kim-Sul algorithm with this corollary is experimentally implemented on a TMS320F243 DSP platform. The experimental results validate the proposed corollary to the Kim-Sul algorithm.

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Investigation of DC-DC Converter Topologies for Future Microprocessor

K. Rajambal [1] P. Sanjeevikumar [2] G. Balaji [3]

Abstract – Future generation microprocessors are expected to exhibit much heavier loads and much faster transient slew rates. Today's Voltage Regulator Module (VRM) will need a large amount of extra decoupling and output filter capacitors to meet future requirements, which basically makes the existing VRM topologies impractical. This paper is concerned with the investigation into topologies capable of meeting future VRM requirements. Three such topologies, the Interleaved Quasisquare-wave (QSW) topology, the Phase-shift buck (PSB) converter and the ZVS self-driven 12-V voltage regulator, are identified and the performance comparison of these three 12-V VRM topologies is presented. Based on simulation results, the optimum topology with high efficiency and fast transient response is identified.

Keywords – Buck, interleaved, phase shift, QSW, self-driven, voltage regulator module.

I. INTRODUCTION

Since the early 80s, computer industry has experienced rapid expansion. Processors are becoming faster and more powerful. Accordingly, their power consumption has increased dramatically. To decrease power consumption and increase the speed, the next generation of computer microprocessors will operate at significantly lower voltages and higher currents than today's generation. In order to provide the power as quickly as possible, the voltage regulator (VR), a dedicated DC/DC converter is placed in close proximity to power the processor. Moreover, the total voltage tolerance will become much tighter. Generally, the Voltage Regulator Module (VRM) is required to operate with a high efficiency. All these requirements pose very serious design challenges. Table 1 shows the specifications for current and future VRMs [1].

A typical structure of a microprocessor power system is shown in Fig. 1. The processor, which is represented by a current source i_L, is powered up from a power supply or voltage regulator module with regulated output voltage V_o. To reduce the effect of the interconnect inductance L_{interc} between the output of the power supply and the processor, decoupling capacitance C_{decoup} is placed right across the processor power supply pins. The most dramatic load transients occur in the processor transition from the sleep mode to the active mode and vice versa, as illustrated in Fig. 2. Moreover, the transition between the sleep and active modes occurs in a very short period of time, resulting in extremely high slew rates di_L/dt [2]. This paper presents the design procedure and simulation results of the three 12-V VRM topologies namely the Interleaved Quasisquare-wave (QSW) topology,

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Table 1: Present and future VRM specifications

	Present	Future
Output Voltage	2.1~3.5V	1~3V
Input Voltage	5V	12V
Load Current	0.3~13A	1~50A
Output Voltage Tolerance	±5%	±2%

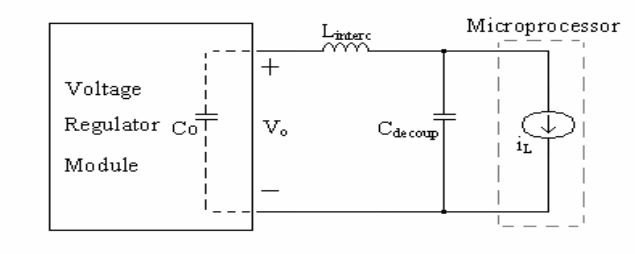


Fig. 1: Microprocessor power system structure

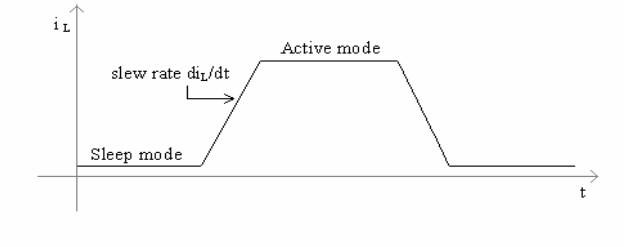


Fig. 2: Load waveform during transients

the Phase-shift Buck (PSB) converter and the ZVS self-driven 12-V voltage regulator along with their performance comparison. Section II, III and IV respectively discusses in detail the principle of operation of the three 12-V VRM topologies along with their simulation results. Finally, section V and VI respectively contains the comparison of these three 12V VRM topologies for future microprocessors and the conclusion. The best VRM topology with high efficiency and fast transient response is identified. The main aim is to maintain the output voltage of the VRM at desired constant voltage (1.5V) when the load varies from no-load (1A) to full-load (50A) and vice versa.

II. INTERLEAVED QUASI-SQUARE-WAVE TOPOLOGY

Fig. 3 shows the Quasi-Square-Wave (QSW) circuit and the operating principle of QSW topology is presented in Fig. 4 [1]. When Q1 turns on, the input voltage charges the inductor current from negative to positive. After Q1 turns off, and before Q2 turns on, the inductor current flows through Q2's body diode. Then Q2 can turn on at zero voltage. After Q2 turns on, the inductor current is discharged to negative. After Q2 turns off, and before Q1 turns on, the inductor current flows through the Q1 body diode. Then Q1 can turn on at zero voltage. In the QSW topology, both the top switch and bottom switch can turn on at zero voltage.

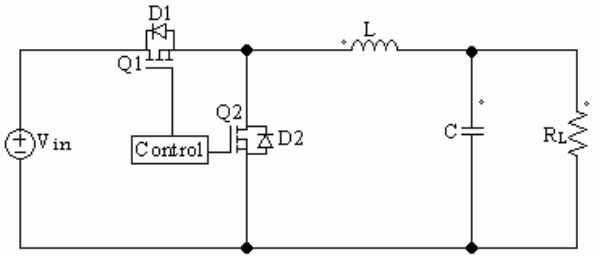


Fig. 3: Quasi-Square-Wave (QSW) topology

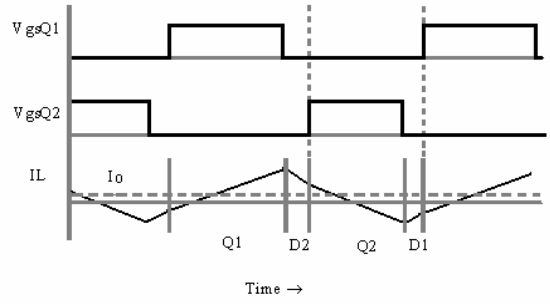


Fig. 4: Operating principle of QSW topology

The QSW topology keeps the VRM output inductor current peak to peak value is two times the full load current, which makes the inductor current go negative in all load ranges. Its inductor design is according to:

$$L = \frac{(V_{in} - V_o) \times D}{2 \times I_o \times f_s} \quad (1)$$

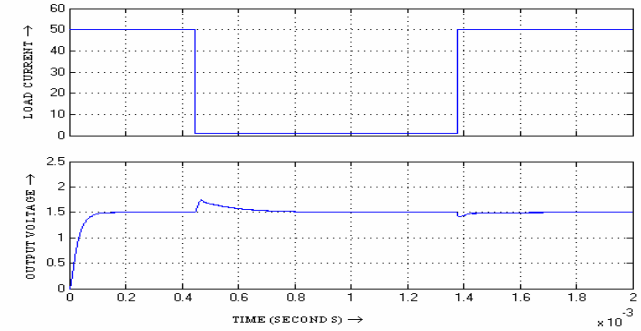


Fig. 5: Simulation results of QSW topology

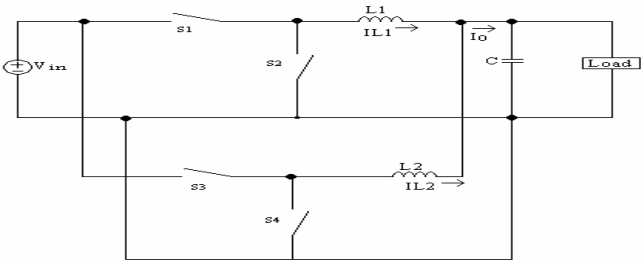


Fig. 6: Interleaved QSW topology

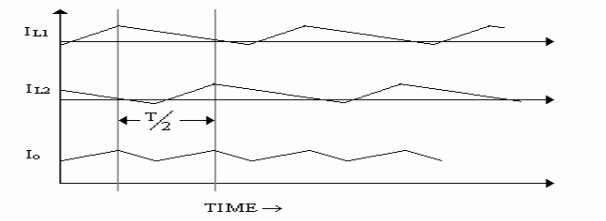


Fig. 7: Current ripple canceling effect of interleaved QSW

Fig. 5 shows the simulation results of the QSW topology at 50 A load and 1 MHz switching frequency using PSIM software. In order to meet both the steady state and transient requirements, interleaved QSW VRM topology is presented in Fig 6. The interleaved QSW topology naturally cancels the output current ripple and still maintains the fast transient response characteristics of the QSW topology as shown in Fig. 7. Generally, the interleaving technique is implemented by paralleling a number of converter cells (phases), and by phase-shifting (interleaving) their drive signals [3]. In this work 2 converter are parallel and interleaved in their driving pulses. The main benefit of interleaving is the decreased magnitude and the increased frequency of the output voltage ripple; the latter is equal to the product of the single-phase switching frequency and the number of the interleaved phases. Fig. 8 shows the simulation results of the interleaved QSW topology. From the simulation results, it is clear that the interleaved QSW topology gives the better performance than the QSW topology and the output voltage is maintained constant at 1.5V, for a variation in load current from no-load (1A) to full-load (50A).

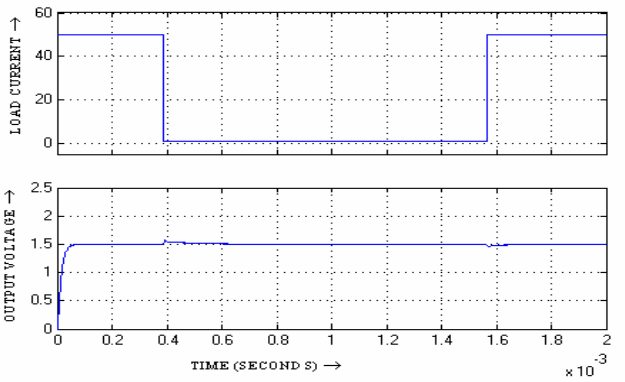


Fig. 8: Simulation results of the interleaved QSW topology

III. Phase-Shift Buck Converter Topology

Due to the very low output voltage, the duty cycle is very narrow, and is predicted to be smaller than 0.1 in the future. This extreme duty cycle impairs the VR's efficiency and imposes obstacles for the transient response. Also, control-wise, to generate the very narrow duty cycle, the control IC must incorporate a very fast comparator, which may cause some cost increase. The PSB converter applies the transformer concept to this non-isolated application; therefore, the extreme duty cycle is extended and many benefits are gained. PSB converters can also achieve ZVS turn-on of the top switch, which enables them to achieve high efficiency at high switching frequencies and high current [4]. The proposed phase-shift buck (PSB) converter is shown in Fig. 9. The PSB converter can be controlled in a traditional PWM fashion or a phase-shifted fashion. The traditional PWM control leads to hard switching of the top switches *Q1~Q4*, while phase-shift control allows soft switching of *Q1~Q4*, which is desirable at high switching frequency. The voltage conversion gain of the phase-shifted buck converter is given by equation 2 [4]

$$\frac{V_o}{V_{in}} = \frac{D}{(n+1)} \quad (2)$$

Through the choice of n, a more desirable duty cycle can be obtained. For example, V_{in}=12V and V_o=1.5V, D is 0.25 when n=1. This duty cycle is twice that of a buck converter. The operating principle of PSB converter is shown in Fig. 10.

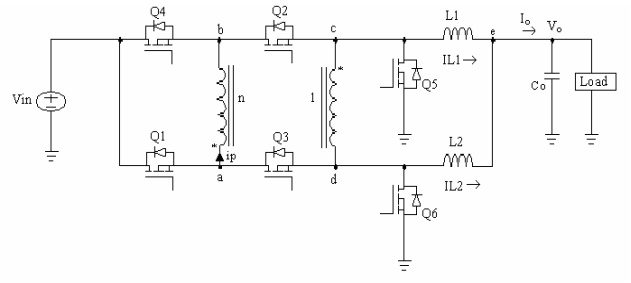


Fig. 9: The proposed phase-shift buck converter

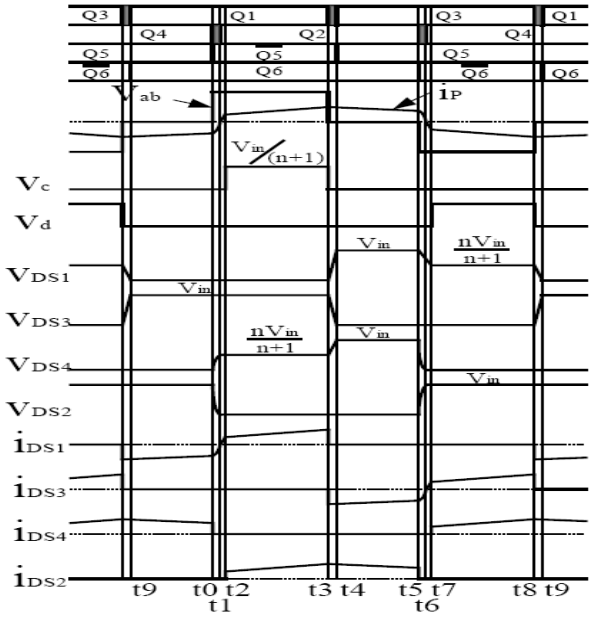
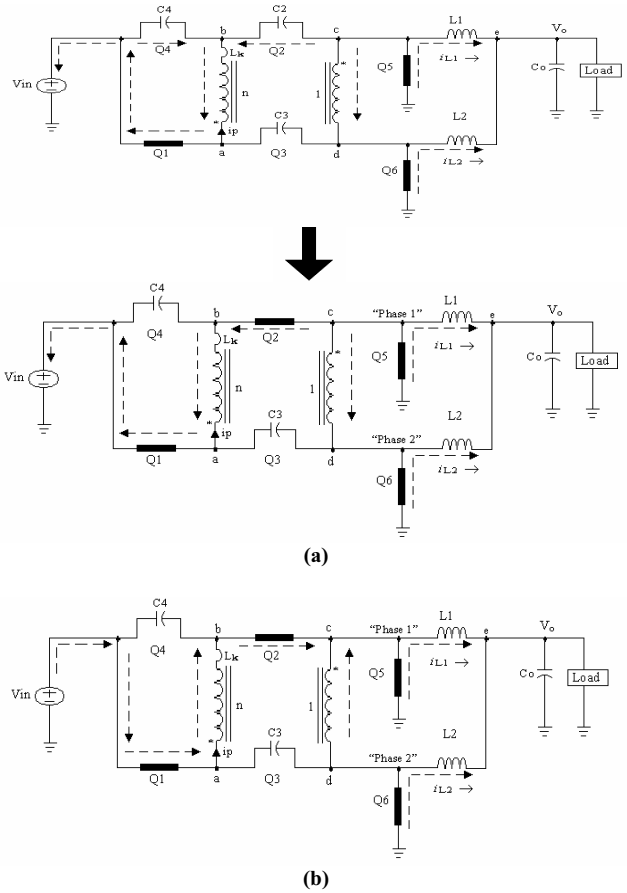
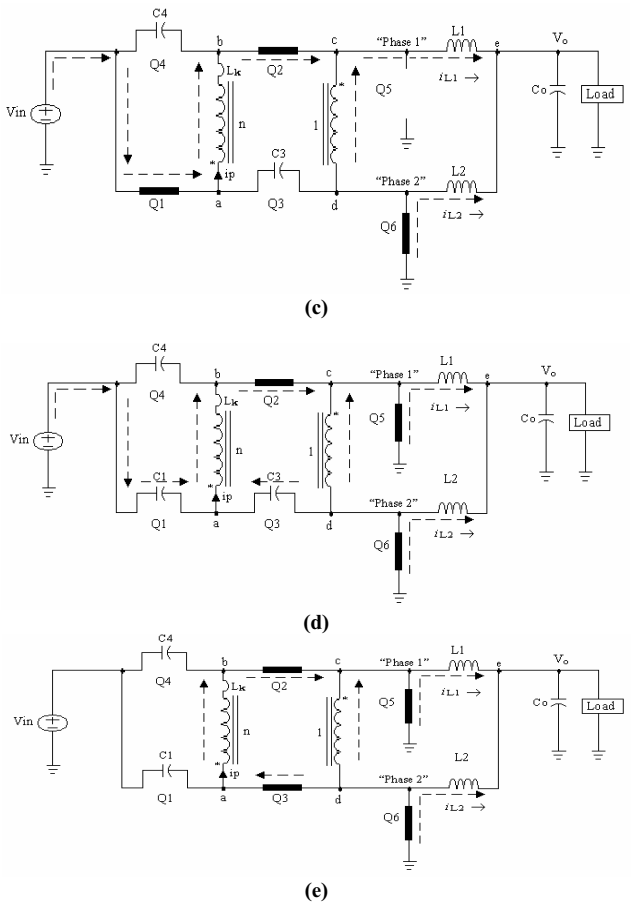


Fig. 10: The operating principle of PSB converter



(a)

(b)



(c)

(d)

(e)

Fig. 11: Subintervals of the Circuit Operation: (a) t_0~t_1 (b) t_1~t_2 (c) t_2~t_3 (d) t_3~t_4 (e) t_4~t_5

Fig. 11(a) shows the subinterval t_0~t_1. Before t_0 the circuit is in the freewheeling mode and the transformer is shorted. The primary current i_p is flowing from node "b" to "a". At t_0, *Q4* is turned off. However, i_p continues flowing due to the existence of *Lk*, therefore *C2* is discharged and *C4* is charged in a fashion determined by the *L-C* resonance formed by *Lk* and the parallel of *C2* and *C4*. Given sufficient energy stored in *Lk*, *C2* can be fully discharged, after which i_p flows through the body diode of *Q2*. Fig. 11(b) shows the subinterval t_1~t_2. At t_1, *Q2* is turned on. Because i_p is flowing through the body diode of *Q2*, *Q2* is turned on at zero-voltage condition, which eliminates the turn-on loss. In the meantime, *Q5*and *Q6* are still carrying current for freewheeling, which means the transformer is still shorted. Thus the voltage across nodes "a" and "b" is applied to *Lk* and builds up i_p in the direction from "a" to "b". As a result, the current through *Q5* decreases until at t_2 it reaches zero. Fig. 11(c) shows the subinterval t_2~t_3. This is a power transfer mode. The transformer acts as an autotransformer and L_1 is being charged while L_2 is being discharged. The transformer primary current i_p is flowing from node "a" to "b". Fig. 11(d) shows the subinterval t_3~t_4. At t_3, *Q1* is turned off, but the transformer primary current i_p continues flowing from node "a" to "b". Because i_p is the reflected output inductor current, *C3* is discharged and *C1* is charged linearly until at t4 when *C3* is fully discharged so i_p flows through the body diode of *Q3*. Fig. 11(e) shows the subinterval t_4~t_5. This is a freewheeling mode. Switches *Q2*, *Q3*, *Q5* and *Q6* are on so the transformer is shorted. From t_5~t_0, another half-period starts, and the operation principle is the same except for polarity changes as shown in Fig. 11 and Fig. 12.

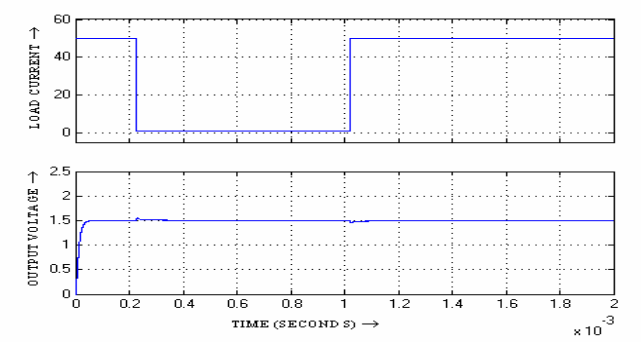


Fig. 12: Simulation results of the phase-shift buck converter

From the simulation results shown in Fig. 12, it is clear that the phase-shift buck converter topology gives better transient response than the interleaved QSW topology.

IV. ZVS Self-Driven 12-V VR Topology

The concept of synchronous rectifier devices being self-driven was widely used in isolated topologies, where the voltage across the secondary winding can be used as the gate driving source for the rectifiers [5]-[10]. The main benefit of self-driven synchronous rectifier devices is that the driving circuitry is simplified, and partial driving energy can be recycled which results in a low-cost, high-efficiency solution. The self-driven topology is basically a buck-derived multiphase interleaving soft switching topology, which can use self-driven technology easily, save driving loss and achieve zero voltage switching (ZVS). The self-driven topology is shown in Fig. 13. In order to achieve ZVS and also to find suitable voltage waveforms in the power stage to drive the synchronous rectifier MOSFETs, a complementary control strategy for *Q1* ~ *Q4* is used. The switch timing diagram for the switches *Q1* ~ *Q4* and secondary synchronous rectifier switches *Q5* ~ *Q6* are shown in Fig. 14. The operation modes of the proposed circuit are shown in Fig. 15. The on time of *Q1* is complementary to that of *Q3*, with a fixed dead time to achieve ZVS as shown in Fig. 14. The same is true of the switches *Q2* and *Q4*. Here, the output voltage is regulated by control of the duty cycle of *Q2* and *Q3*. The larger the duty cycle is, the higher the output voltage will be.

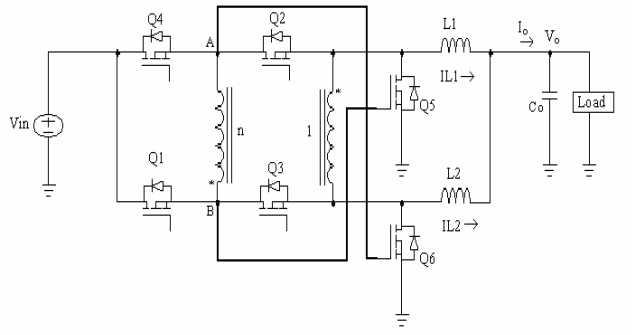


Fig. 13: ZVS self-driven 12-V Voltage Regulator

Based on the switch-timing diagram, there are eight operating modes during one switching cycle. Fig. 14 illustrates the equivalent circuits for Mode1 to Mode 4. During the other half of the switching cycle, the circuit operates in the same way as in Mode1 to Mode 4.

A. Mode 1 [T_0 ~ T_1]

Q1 and *Q2* are on. The voltage at point B is actually the input voltage, which is 12 V. Because point B is directly connected to the gate of *Q5*, *Q5* is self-driven to be on. On the other hand, since *Q2* and *Q5* are both on, point A is connected to the ground which automatically keeps *Q6* off during this operating mode. The energy is transferred from the input to the output through the transformer.

B. Mode 2 [T_1 ~ T_2]

Q2 turns off at T_1, and the reflected output current discharges and charges the output capacitor of *Q4* and *Q2*, respectively. Meanwhile, because *Q5* stays on during this interval, the drain-to-source voltage of *Q4* will drop to zero so that *Q4* can be turned on under ZVS. Where n_p is the transformer turn's ratio; C_{eq} is the sum of the output capacitance of *Q2* and *Q4* plus the gate-to-source capacitance of *Q6*; V_{in} is the input voltage; $I_{o\text{-}min}$ is the minimum load current at which the ZVS can still be achieved. The gate capacitor of *Q6* serves as a lossless snubber of *Q2*.

C. Mode 3 [T_2 ~ T_3]

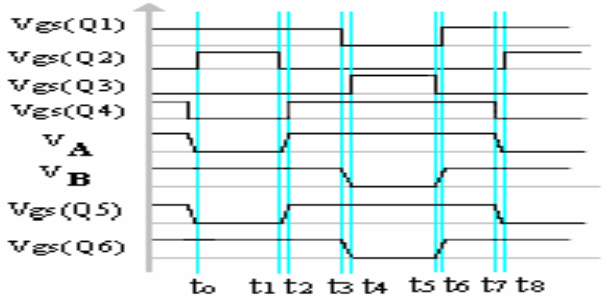
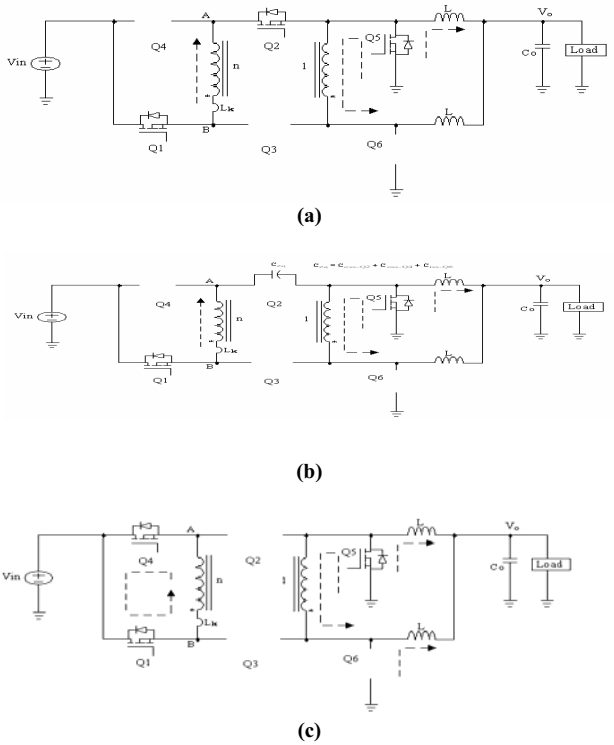
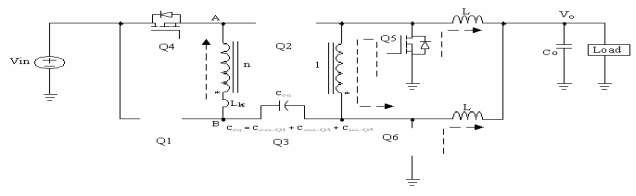


Fig. 14: Control strategy of ZVS self-driven 12-V VR





(d)

Fig. 15: Operation modes of the ZVS self driven 12-V VR: (a) Mode 1 [$T_0 \sim T_1$] (b) Mode 2 [$T_1 \sim T_2$] (c) Mode 3 [$T_2 \sim T_3$] (d) Mode 4 [$T_3 \sim T_4$]

The energy stored in the transformer leakage inductor freewheels through *Q1* and *Q4*. Since both point A and point B are connected to the input, *Q5* and *Q6* are on during this mode, which provide the current freewheeling paths for the synchronous rectifier.

D. Mode 4 [$T_3 \sim T_4$]

Q1 turns off at T_3. The leakage inductor of the transformer resonates with the output capacitors of *Q1* and *Q3*, and similarly, the gate capacitor of Q5 joins the resonance because it is in fact in parallel the output capacitor of *Q3*. In order to achieve ZVS for *Q3*, two conditions are necessary: one is the appropriate dead time between Q1 and *Q3*, which is one-fourth of the self-resonant period; the other condition is that the energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output capacitances as well as the gate capacitance of *Q5*. These two conditions can be expressed as

$$T_{d2} = \frac{\pi\sqrt{L_k C_{eq}}}{2} \tag{3}$$

$$I_{o-\min} = \frac{2n_p C_{eq} V_{in}^2}{L_k} \tag{4}$$

where L_k is the leakage inductance of the transformer reflected to the primary side; $I_{o\text{-}min}$ is the minimum output current needed to achieve ZVS. From *T4* to *T8*, another half-period starts, and the operation principle is the same except for polarity changes. It should be noted that not only can the proposed circuit achieve ZVS, but also the voltage waveform at point A and B are exactly those desired to drive the synchronous rectifier MOSFETs. Simulated waveforms of the output voltage and the load current are shown in Fig. 16. A self-driven dc/dc converter for non isolated 12V VR is proposed [11]-[17]. ZVS of all the MOSFETs is achieved to reduce the switching loss. By adding a transformer, the proposed topology extends its duty cycle so that the switching loss is further reduced. This innovative self-driven concept eliminates the need for synchronous rectifier drivers which saves cost [18]-[21].

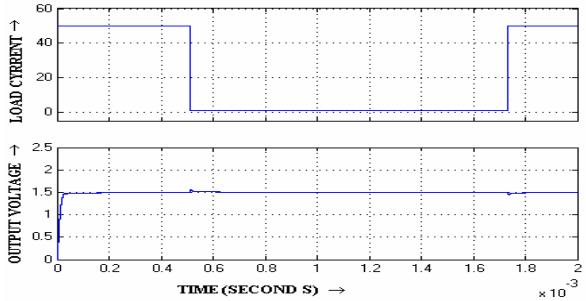


Fig. 16: Simulated waveforms of the output voltage and the load current

Table 2: Comparison of the three VRM topologies at 1MHz

Name of the VRM topology	Efficiency	Settling time
Interleaved Quasi-Square topology	75.3%	30µs
Phase-Shift Buck topology	82.9%	16µs
ZVS self-driven 12-V VR topology	88.1%	14µs

The power circuit of ZVS self-driven 12-V VR topology is shown in Fig. 17. The feedback (F.B.) is taken at the voltage divider circuit at the output side. The firing pulses for the MOSFET are generated using circuit shown in Fig. 18. A pulse width modulator 3525 is used to generate two PWM pulses. By varying the resistance at point2 of 3525, we set the reference point.

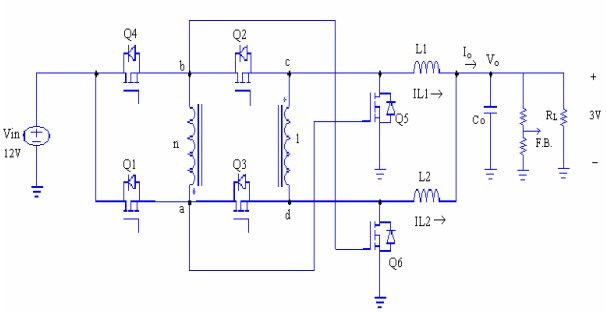


Fig. 17: Power circuit of ZVS self-driven 12-V VR topology

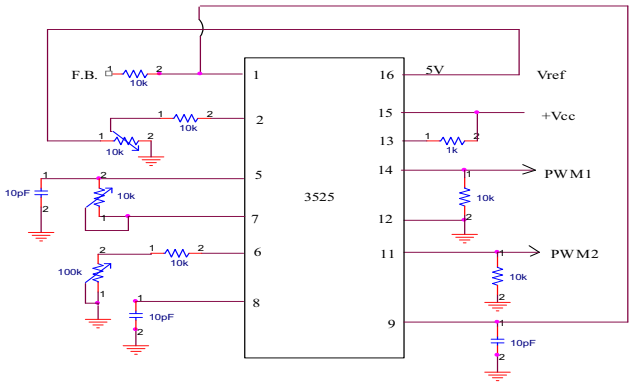


Fig. 18: Pulse generation circuit

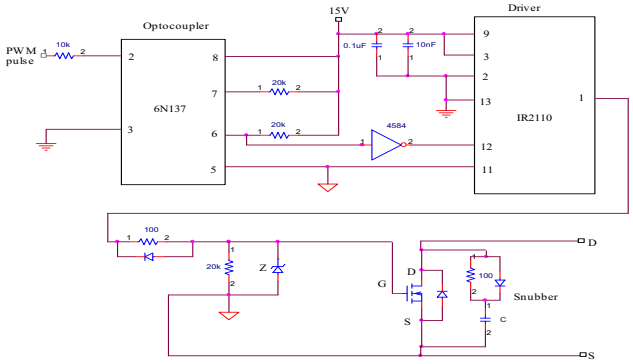


Fig. 19: Opto-coupler and driver circuit

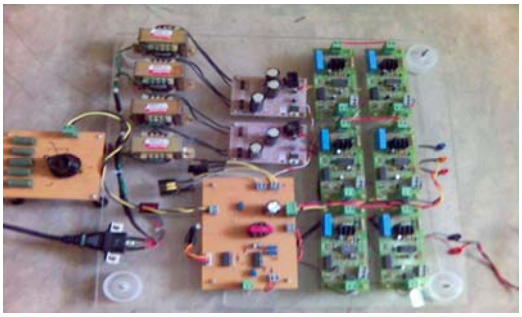


Fig. 20: Hardware of ZVS self-driven 12-V VR topology

V. Design and Implementation of ZVS Self-Driven 12V VR Topology

By adjusting the resistance between point5 and point7 of 3525, we get the requisite dead time. We attain the required frequency by adjusting the variable resistor of 100k connected at point 6 of 3525. The optocoupler is used for the isolation purpose. The PWM pulse coming from 3525 is given to point 2 of the optocoupler 6N137 as shown in Fig. 19. The output waveform of the optocoupler is the inverted version of the applied waveform. To get original waveform, we are using a NOT gate 4584. The driver IR2110 is utilized to get the original PWM pulse with required current limit. The output pulse from the IR2110 is used to drive the gate of the mosfet. The mosfets used are IRF840 (manufactured by (IRF) International Rectifier Company). The positive regulator IC used is 7815. Inductance = 100µH and Capacitance = 5µF are used for the simulation and hardware analysis. The hardware version of the ZVS self-driven 12-V VR topology is shown in Fig. 20. The hardware results are shown in the Fig. 21 to Fig. 26. The specifications followed to get these results are input voltage of 12V, output voltage of 3V, full load current of 2A and switching frequency of 25 kHz.

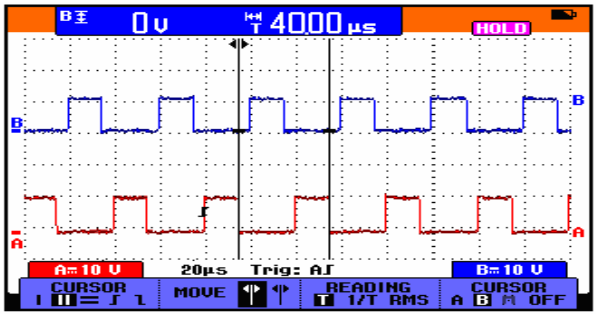


Fig. 21: Firing pulses for mosfets Q1:Ch.A and Q4:Ch.B [(10V/div)(timebase:20*u*s/div)]

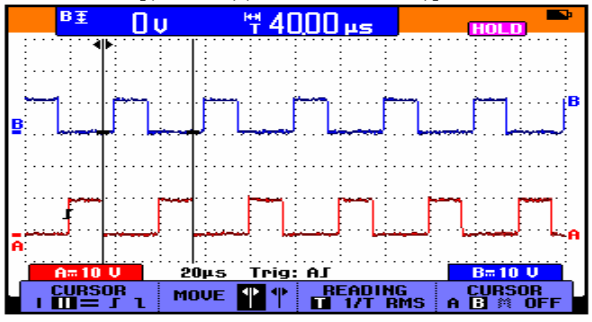


Fig. 22: Firing pulses for mosfets Q3:Ch.A and Q2:Ch.B [(10V/div)(timebase:20us/div)]

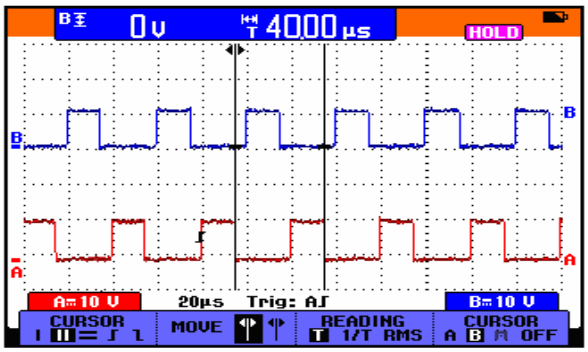


Fig. 23: Firing pulses for mosfets Q6:Ch.A and Q5:Ch.B [(10V/div)(timebase:20us/div)]

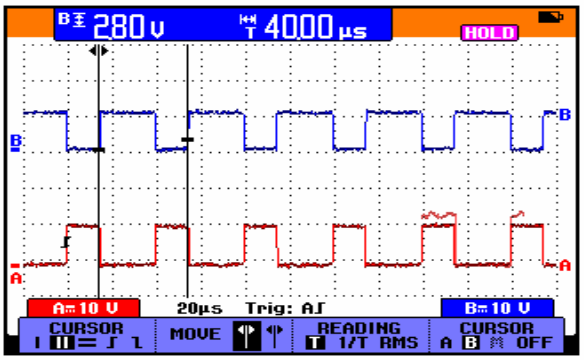


Fig. 24: Optocoupler input: Ch.A and output: Ch.B [(10V/div)(timebase:20us/div)]

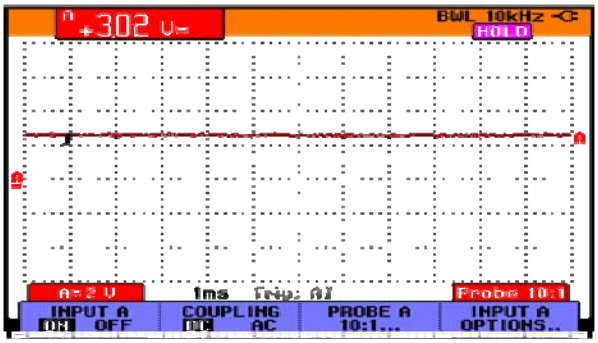


Fig. 25: Output voltage at no-load [(2V/div)(timebase:1ms/div)]

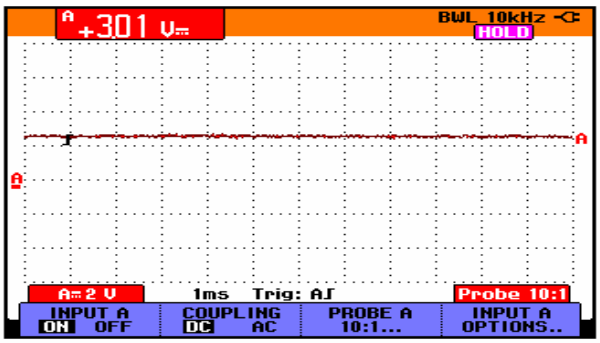


Fig. 26: Output voltage at full-load [(2V/div)(timebase:1ms/div)]

VI. Hardware Results

Fig. 21, Fig. 22 and Fig. 23 show the hardware results of the firing pulses for the mosfets Q1 and Q4, Q3 and Q2 and Q6 and Q5 respectively. Fig. 24 shows the Optocoupler input and output. Fig. 25 and Fig. 26 show the output voltage at no-load and full-load respectively.

VII. Comparison Of The Simulation Results And The Hardware Results

The simulation results and the hardware results are compared as shown in Table 3. The output voltage in volts at no-load, 25%, 50%, 75% and 100% of the full-load are presented here. The %error between the hardware results and the simulation results is calculated and is given in the table.

Table 3: Comparison of the simulation results and the hardware results

% of full-load	Hardware Results: Output voltage in volts	Simulation results: Output voltage in volts	% error
No-load	3.02	3.0	0.66
25%	3.02	3.0	0.66
50%	3.01	3.0	0.33
75%	3.01	3.0	0.33
100%	3.01	3.0	0.33

VIII. Conclusion

The simulation models for the three different VRM topologies for future microprocessors are developed. The performance of the three VRM topologies is studied through simulation. It is observed from the simulation results that the ZVS self-driven 12-V voltage regulator topology offers better performance in terms of efficiency and settling time. The topology is implemented in hardware. It is found that the output voltage is maintained constant at desired voltage level (3V) irrespective of the variations in load from no-load to full-load value, thus validating the simulation results.

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Comparative Study of PWM Inverters Fed 3-Phase Induction Motor

Y.R. Manjunatha. [1] M.Y.Sanavullah.[2]

Abstract – In this paper the performance of three-phase induction motor, fed from SPWM & MSPWM inverters are discussed. Computer simulations are used to compare the performances. The 3 phase induction motor model is simulated with sinusoidal excitation. The line current, output power, and efficiency are compared with the experimental results. The simulated results are very close to the practical values and the difference is less than 10%. The torque developed by the motor, when fed with SPWM-inverter and that of MSPWM-inverter are compared. The distortion in the developed torque in both the cases is compared. From the simulation results it is observed that, the average value of torque developed by the motor is same when the motor is fed with SPWM and MSPWM inverters. But the distortion is less when the motor is excited with MSPWM inverter.

Keywords – PWM inverters, induction motor drive, 3-phase induction motor, SPWM inverter, MSPWM-inverter.

I. INTRODUCTION

In many modern adjustable-speed drives the demand is for precise and continuous control of speed, or position with long-term stability, good transient performance, and high quality efficiency. In power electronics, various pulse-width modulation (PWM) techniques are widely employed to control the output of static power converters. The reason for using PWM techniques is that they provide voltage and/or current wave-shaping customized to the specific needs of the application under consideration. Generally, two classes of PWM techniques for static power converters can be identified. The programmed or optimal PWM techniques that produce switching patterns based on optimization of specific performance criteria are the first. 'The other class is based on certain low-frequency reference or modulating waveform, which is compared with a high-frequency carrier waveform. These techniques are known as carrier PWM techniques [1]. To illustrate the main idea associated with the carrier PWM techniques, the sinusoidal pulse-width modulation (SPWM) technique. It is based on the principle of comparing a triangular carrier signal with a sinusoidal reference waveform [2].

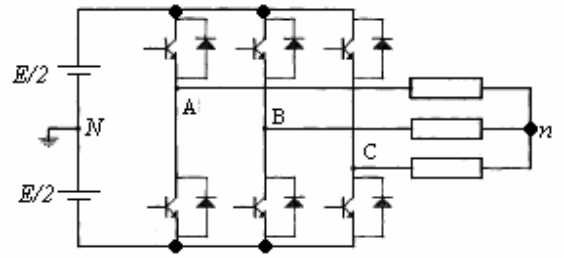

Fig. 1: Voltage source inverter

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Although the implementation of this technique is relatively simple, there are two drawbacks when compared with the six -step inverter as follows:

- Attenuation of the fundamental component of the output waveform or in other words the maximum line-to-line amplitude voltage is 0.866 pu ;
- high switching frequency, when compared with the six-step inverter, which means increased stresses on converter semiconductor elements.

To overcome these problems, improved PWM techniques have been proposed in the technical literature over the last 35 years. There are numerous technical papers dealing with PWM control in inverter-rectifier systems. Furthermore, when the microprocessors became available, significant work is reported in [3]-[6] where problems associated with the on-line computation of the switching signals had to be dealt with. However, some proposed techniques improve only the gain of the modulator, and some others improve the gain and provide reduction in the effective switching frequency. Converter effective switching frequency is defined as the number of current interruptions normalized over the output period (7-9).

In this paper a new scheme is proposed called, modified sinusoidal PWM pattern to improve the gain of the pulse-width modulator. However, this PWM technique that provides not only increased gain, but also a reduction in the effective switching frequency, since switching elements are kept inactive for a specified interval. For instance, when the neutral point of the load is floating in a voltage source inverter, converter phase legs can be "relaxed' to achieve lower effective switching frequency by avoiding intersections for some interval. This can be done by employing a special carrier waveform. Therefore, switching losses and resulting stresses of the PWM converter for the same carrier frequency are potentially reduced when comparing with continuous PWM techniques. The objective of this paper is to present and critically discuss and compare the influence of these modulation techniques on 3- phase induction motor.

II. SPWM TECHNIQUE AND ITS INFLUENCE ON 3-PHASE INDUCTION MOTOR

In sinusoidal pulse width modulation a high frequency triangular carrier wave v_c is compared with a sinusoidal reference wave v_r of the desired frequency. The intersection of v_c and v_r waves determines the switching instants and commutation of the modulated pulse. The carrier and reference waves are mixed in a comparator. When he sinusoidal reference wave has magnitude higher than the triangular wave, the comparator output is high otherwise it is low. The ratio of v_r / v_c is called the amplitude modulation index (m_a) and it controls the harmonic content of the output voltage waveform.

$$m_a = \frac{V_{r.}}{V_c} \quad (1)$$

The pulse widths and the RMS value of voltage depend upon $\frac{v_r}{v_c}$. The frequency of reference wave decides the output frequency. The carrier frequency decides number of pulses per half cycle. More the number of pulses the smoother is the waveform.
The RMS value of output voltage can change from 0 to maximum value by changing the modulation index.

The RMS value of output voltage is

$$V_0 = V_d[\sum_{M=1}^{p}\left(\frac{M}{\pi}\right)]^{\frac{1}{2}} \quad (2)$$

where 'p' is number of pulses per half cycle.

$$V_0 = \sum_{m-1}^{p} C_n \sin n\omega t \quad (3)$$

where $C_n = \sqrt{A_n^2 + B_n^2}$

The voltage waveform can be expanded in to Fourier series.

$$A_n = \sum_{m=1}^{p}\left(\frac{2V_d}{n\pi}\right)[\sin n(\alpha_m + \delta_m) - \sin(n\alpha_m)] \quad (4)$$

$$B_n = \sum_{m=1}^{p}\left(\frac{2V_d}{n\pi}\right)[\cos(n\alpha_m) - \cos n(\alpha_m + \delta_m) \quad (5)$$

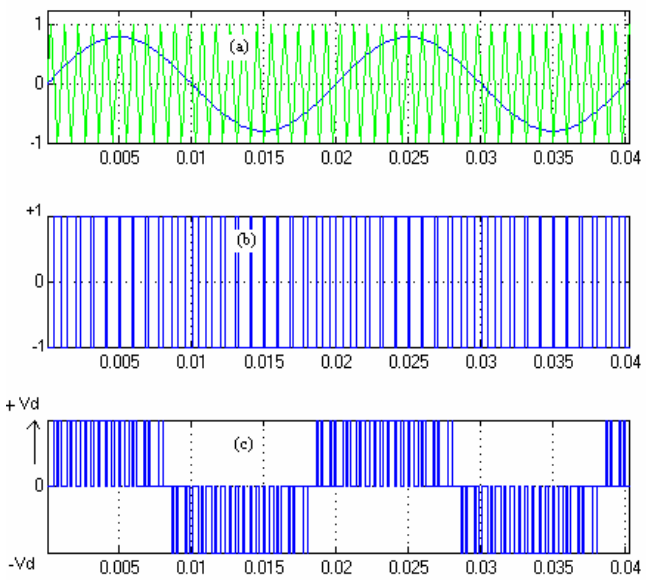

Fig. 2: a) Reference and carrier waveforms. b) line-to-neutral voltage. C) line-to-line output voltage

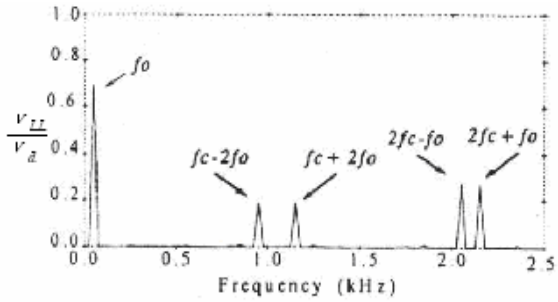

Fig. 3: Harmonic spectrum of line-to-line voltage

In the linear region ($m_a \le 1.0$), the fundamental-frequency component in the output voltage varies linearly with the amplitude modulation ratio m_a. Fig. 2 and Fig. 3 show the waveforms of SPWM and harmonic spectrum of line-to-line voltage, respectively. The peak value of the fundamental-frequency component in one of the inverter leg is,

$$(V_{AN})_1 = m_a \frac{V_d}{2} \quad (6)$$

The line-to-line rms voltage at the fundamental frequency, due to 120^0 phase displacement between phase voltages can be written as

$$V_{LL,rms} = \frac{\sqrt{3}}{\sqrt{2}}(V_{AN})_1 \quad (7)$$

$$= \frac{\sqrt{3}}{2\sqrt{2}} m_a V_d \quad (8)$$

$$= 0.612 m_a V_d \quad (m_a \le 1.0) \quad (9)$$

From equation 9 we observe that the fundamental rms value of output voltage varies linearly with the modulation index.

III. Modified Sinusoidal Pulse Width Modulation

The technique of generation of waveform is the further improvement of the sinusoidal pulse modulation. In SPWM technique it is observed that the pulse width in the range of 60^o to 120^o does not vary much and is constant for a longer duration. Instead of providing the number of pulses in the 60^o to 120^o interval by comparing a reference wave with the carrier wave a single pulse of that duration is introduced in that space so that the switching losses of the power transistor is reduced during this interval and there by improving the wave form as suitable for induction motor drives .So to generate the gating pulses for the switching devices the carrier wave is applied during the first and last 60^o intervals per half cycle. This type of modulation is known as Modified Sinusoidal Pulse Width Modulation (MSPWM). This type of switching the sine wave reserves components with minimal number of switching there by giving a grater performance and efficiency of the inverter.

The number of pulses 'q'in the 60^o is normally related to the frequency ratio by $\frac{f_C}{f_0} = 6q$.

In a three phased Delta /Star connected network, even harmonic are absent in star connected network the third harmonic and its multiples will be absent. The remaining present are 5^{th}, 7^{th} 11^{th}, 13^{th}, etc which can be eliminated by properly positioning the pulses in the first and last 60^o intervals of the half cycle. Any number of unwanted harmonics at the out put of the single phase inverter can be eliminated by introducing the number of symmetrically placed voltages notches i.e., by suitably modifying the MSPWM wave form to calculate the positioning of the notches we will consider the Fourier analysis of the output voltage waveform which is given by

$$V_0 = \sum_{n=1,3,5}^{\infty} B_n \sin \omega t. \quad (10)$$

where

$$B_n = \frac{4V_s}{\pi}[\int_0^{\alpha_1} \sin n\omega t\, d\omega t + \int_{\alpha_2}^{\frac{\pi}{2}} \sin n\omega t\, d\omega t + ...] \quad (11)$$

Considering only for two notches

$$B_n = \frac{4V_s}{\pi} \frac{1 - \cos n\alpha_1 + \cos n\alpha_2}{n} \quad (12)$$

The third and fifth harmonics would be eliminated if

$$1 - \cos 3\alpha_1 + \cos 3\alpha_2 = 0$$

$$1 - \cos 5\alpha_1 + \cos 5\alpha_2 = 0$$

Solving the above equations by iterations we get

$\alpha_1 = 17.83^0$ and $\alpha_2 = 37.07^0$

Therefore the MSPWM technique can be applied to generate the notches, which would eliminate certain harmonics effectively in the output voltage.

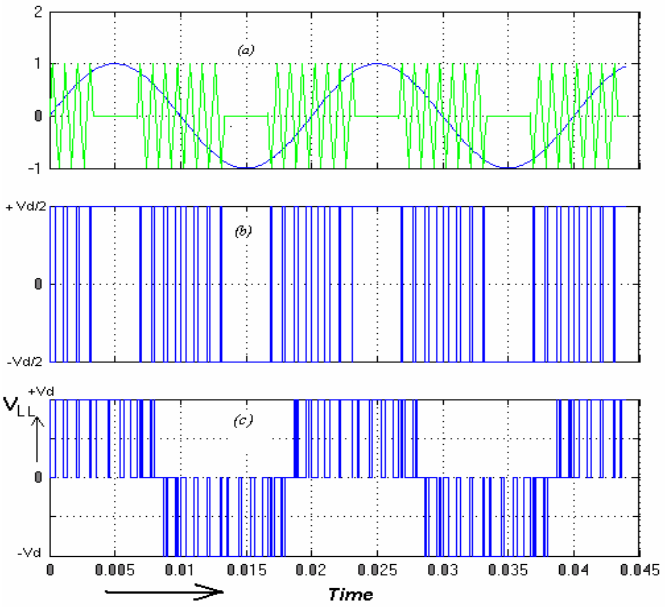

Fig. 4: a) Reference and carrier waveforms. b) line-to-neutral voltage. c) line-to-line output voltage

Fig. 4 and Fig. 5 show the waveforms of MSPWM technique and harmonic spectrum of line-to-line voltage, respectively. Here the carrier frequency f_c is 1050Hz. modulation index m_a is 0.8 and reference signal frequency is 50 Hz. The DC bus voltage is 508 volts. Modulation index is varied from 0 to 1 (Linear modulation) to vary the rms value of the output voltage.

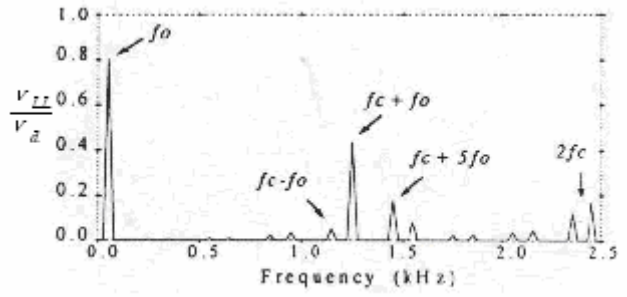

Fig. 5: Spectrum of line-to-line output voltage

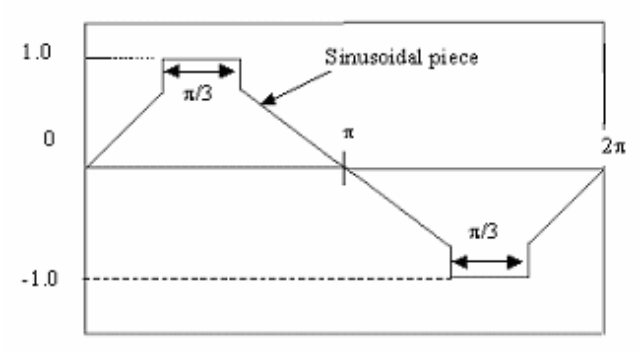

Fig. 6: Reference waveform for MSPWM technique

Referense wave form for MSPWM tecnique is as shown above and is defined as,

$$f_A(\omega t) = \begin{cases} m\sin(\omega_0 t) & 0 \le \omega_0 t \le \frac{\pi}{3} \\ 1 & \frac{\pi}{3} \le \omega_0 t \le \frac{2\pi}{3} \\ m\sin(\omega_0 t) & \frac{2\pi}{3} \le \omega_0 t \le \pi \end{cases} \quad (13)$$

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T \left(v(t)\right)^2 dt} \quad \text{(General Form)} \quad (14)$$

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T \left(f_A(\omega t)\right)^2 dt} \quad (15)$$

$$V_{rms} = \sqrt{\frac{1}{\pi}\left[\int_0^{\frac{\pi}{3}} (m_a \sin\omega_0 t)^2 d\omega_0 t + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} (1)^2 d\omega_0 t + \int_{\frac{2\pi}{3}}^{\pi} (m_a \sin\omega_0 t)^2 d\omega_0 t\right]} \quad (16)$$

$$V_{rms} = \sqrt{\frac{1}{3}\left(m_a^2 + 1\right)} \quad (17)$$

$$V_{rms} = 0.816\ m_a V_d \quad (18)$$

If $m_a = 1$,

$$V_{rms} = 0.816\ V_d$$

From equation (14)-(18), we observe that the fundamental rms value of output voltage varies linearly with the modulation index.

IV. Experimental Results

To experimentally validate the proposed MSPWM technique, mathematical models of three-phase SPWM & MSPWM inverter have been developed and simulated using MATLAB. A 3-phase induction motor is selected with the specifications shown in the table below.

Table 1: Specifications of the motor

Type of the motor	3-ϕ Induction motor
Rated output power	3.7 kW (5 HP)
Rated line-to-line voltage	415 V
Rated current	8.4 A
Number of poles	4
Frequency of the supply voltage	50 Hz
Rated speed	1485 rpm
Type of winding	Y-connected

The parameters of this motor are calculated by conducting No-load test, Blocked Rotor test and Retardation test. This motor model is simulated using MATLAB and the simulated results are compared with that of practical results. It is found that these two results are very close to each other. Then the motor model is simulated with the proposed SPWM and MSPWM inverters. Table 2 shows the readings of load test from no-load to full-load.

Table 2: Experimental results of motor on load test at rated voltage (415V)

I_L Amps	W_1 Watts	W_2 Watts	T_L N-m	N rpm	I/p Watts	O/p Watts	%η
4.5	1000	-800	0	1480	200	0	0
4.9	1400	-500	2.53	1463	900	387.6	43
5.5	1700	-100	7.6	1413	1600	1124.5	70.2
6.1	2100	0	10.96	1376	2100	1579	75.2
6.8	2400	700	15.18	1320	3100	2098	67.6

Table 3: Simulation results of motor model on load test at rated voltage (415V)

S.No.	I_L Amps	T_L N-m	N rpm	O/p Watts	I/p Watts	%η
1.	4.52	0	1482	0	195	0
2.	4.6	2.53	1463	287	859	45
3.	5.3	7.6	1423	1133	1523	74
4.	5.7	10.96	1448	1547	2048	75.5
5.	6.7	15.18	1293	2055	3034	67.7

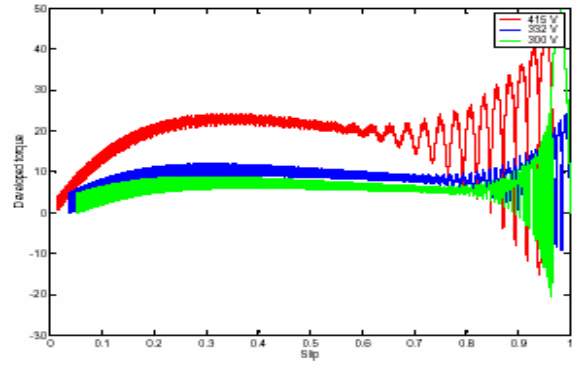

Fig. 7: Slip-Torque chars. of the motor for different voltages fed from SPWM inverter

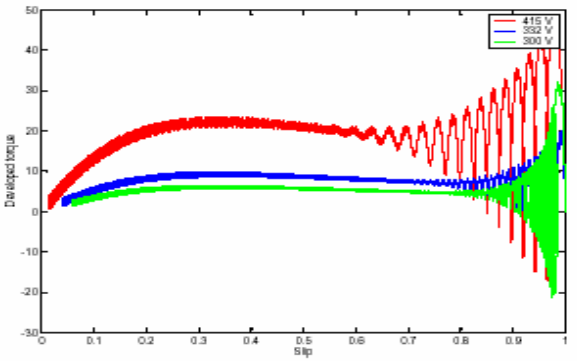

Fig. 8: Slip-Torque chars. of motor fed with MSPWM inverter for different voltages

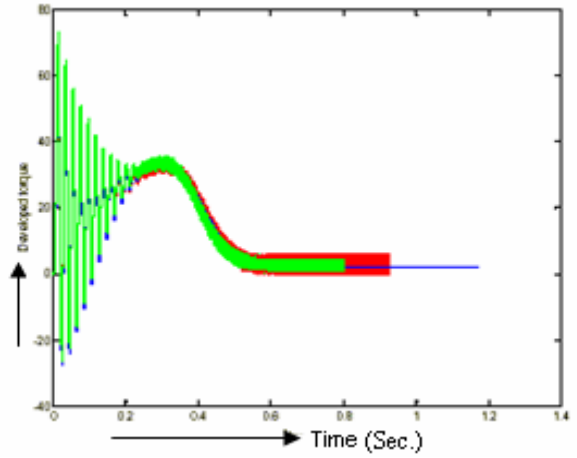

Fig. 9: Torque developed by the motor fed with sine voltage, SPWM and MSPWM inverters

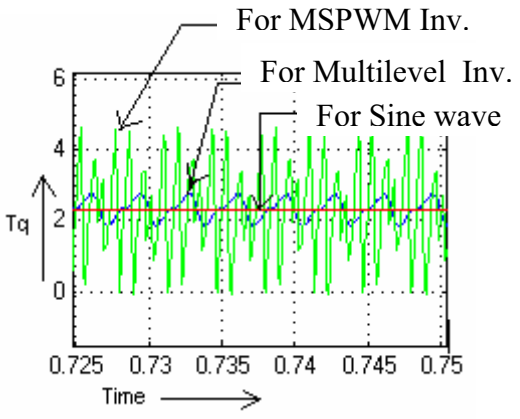

Fig. 10: Torque developed by the motor in steady state fed with sine voltage, SPWM and MSPWM inverters

V. CONCLUSION

The comparison is made on the basis of ripple in the developed torque of the motor on steady state. Fig. 9 and 10 shows simulation results of the torque developed by the motor excited at rated voltage with sinusoidal voltage, SPWM-inverter and MSPWM-inverter. All the three graphs have been plotted on the same axis. The blue colour graph is plotted for sinusoidal excitation, red colour graph is plotted for SPWM inverter excitation, and green colour graph is plotted for MSPWM inverter excitation at rated voltage. From the graph it is observed that, the average value of torque developed by the motor is same when the motor is fed with SPWM and MSPWM inverters. But the ripple (distortion) magnitude is more when the motor is excited with SPWM inverter compared with that of MSPWM inverter (*i.e.* There is 75% reduction in the ripple magnitude). Hence MSPWM technique is the best suitable for a 3-phase induction motor compared to SPWM inverter technique.

Fig. 10: Photograph of Experimental setup

In the fig. 10, there are three rows of switching devices. Each row consists of four devices (i.e. one full bride inverter), one bridge is used for Sinusoidal PWM technique, one bridge is used for Modified SPWM technique and the second row of three bridges are used for multilevel inverter technique. The Multilevel inverter techniques are not discussed in this paper.

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BIOGRAPHIES

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Intelligent Control of Parallel Loaded Resonant Converter fed PMDC Motor

T.S. Sivakumaran. S.P. Natarajan.

Abstract – The Permanent Magnet DC (PMDC) motor has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability and maintenance free operation. A Parallel loaded Resonant Converter (PRC) which is a subset of DC-DC converters can be operated with either zero-voltage turn – on (above resonant frequency) or zero-current turn-off (below resonant frequency) to eliminate the turn-on or turn-off losses of the semiconductor devices. This paper presents simulation and real time implementation of PI and Fuzzy Logic Controllers (FLC) for speed control of a PRC fed PMDC motor on light load. The control algorithm developed ensures tracking of the reference speed and rejection of system disturbances by successive measurements of the motor speed. The results from (i) simulation of PI and fuzzy logic controls using MATLAB software and (ii) TMS320F2407 DSP based hardware implementation show that FLC performs effectively for the chosen PMDC motor system.

Keywords - PI control, fuzzy logic control, parallel loaded resonant converter (PRC).

I. Introduction

Load resonant converters [1-6] are soft-switched DC-DC converters. A Parallel loaded Resonant Converter (PRC)[1-4] which is a subset of load resonant converters can be operated with either zero-voltage turn – on (above resonant frequency) or zero-current turn-off (below resonant frequency) to eliminate the turn-on or turn- off losses of the semiconductor devices. Due to the reduced switching losses, this converter is particularly suited for high power and high frequency operation. The operating frequency of a PRC usually varies over a wide range to regulate the output. This results in a penalty in filter design and poor utilization of magnetic components. Instead of frequency modulation control, the resonant converters can also be regulated by phase shift control where the duty ratio D is modulated and the switching frequency is kept constant. Power electronic systems like PRC have non-linear characteristics. Considerable research work reported very recently in [3-6] discuss about control of load resonant converters operated only as power supplies.

Since soft-switching techniques can also be applied for DC motor drives, the performances of PI control and Fuzzy Logic Control (FLC) for a PRC fed PMDC motor are compared in this work using MATLAB based simulation as well as TMS320F2407 DSP based implementation [7].The results are presented and analyzed.

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II. Parallel Loaded Resonant Converter Fed PMDC Motor

The system comprises a full-bridge inverter, resonant tank circuit, bridge rectifier, filter circuit, PMDC motor and eddy current type mechanical load as shown in Fig. 1 The resonant circuit consist of series inductance L_s and parallel capacitor C_p. Q_1-Q_4 are switching devices having base /gate turn-on and turn-off capability. D_1 to D_4 are anti-parallel diodes across these switching devices. The MOSFET (say Q_1) and its anti-parallel diode (D_1) act as a bidirectional switch. The gate pulses for Q_1 and Q_2 are in phase but 180 degree out of phase with the gate pulses for Q_3 and Q_4. The positive portion of switch current flows through the MOSFET and negative portion flows through the anti-parallel diode. The voltage across the points AB is rectified and fed to motor load through low pass filter L_f - C_f. In the analysis that follows, it is assumed that the converter operates in the continuous conduction mode and the semiconductors have ideal characteristics. The parameters of the chosen DC motor are: 12V, 1500 rpm, 18Watts, R_a=160Ω, L_a=1.6mH, J=1Nm^2, B=0.5 Nm/rads^{-1}.

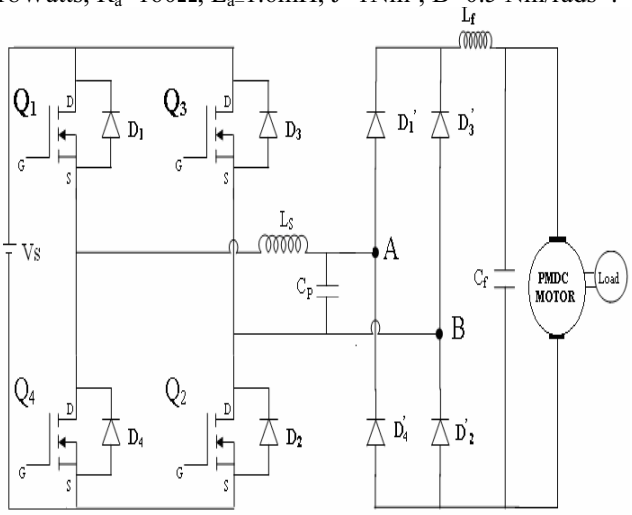

Fig. 1: Schematic diagram of full-bridge PRC fed PMDC motor

III. Open- Loop Converter Dynamics

The open-loop converter system (Fig. 2) comprises the power stage modeled in the above section. The inputs to the power stage are supply voltage Vs and duty ratio D and the output is Vo. Generally, Vs is maintained at a constant value.

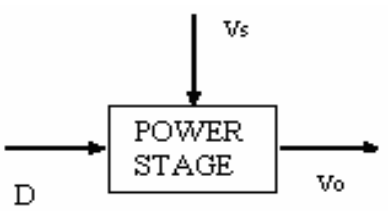

Fig. 2: Block diagram of open loop converter

IV. Design of Conventional Controller

Many industrial processes are non-linear and are thus complicated to be described mathematically. However, it is known that a good many non-linear processes can satisfactorily be controlled using PID controllers provided the controller parameters are tuned well. Practical experience shows that this type of control has a lot of sense since it is simple and based on three basic behavior types or modes: proportional (P), integrative (I) and derivative (D). Instead of using a small number of complex controllers, a larger number of simple PID controllers can be used to control complex processes in an industrial assembly in order to automate such processes. Controllers of different types such as P, PI and PD are today basic building blocks in control of various processes. In spite of simplicity, they can be used to solve even a very complex control problem, especially when combined with different functional blocks, filters (compensators or correction blocks), selectors etc. A continuous development of new control algorithms insure that the PID controller has not become obsolete and that this basic control algorithm will have its part to play in process control in foreseeable future. It can be expected that it will be a backbone of many complex control systems. While proportional and integrative modes are also used as single control modes, a derivative mode is rarely used in control systems.

PI controller forms the control signal in the following way:

$$U(t) = K_p[e(t) + 1/T_i \int e(\tau)d\tau] \quad (1)$$

The tuning of this controller is done by the reaction curve method. Controller tuning involves the selection of the best values of K_p and T_i. This is often a subjective procedure and is certainly process dependent. In this work K_P=2.5 and T_i=5 are the values of the controller settings tuned to provide satisfactory response of the converter.

V. Design of Fuzzy Logic Controller

The derivation of fuzzy control rules is heuristic in nature (Table 1) and based on the following criteria:

- When the output of the converter is far from the set point, the change of duty cycle must be large so as to bring the output to the set point quickly.
- When the output of the converter is approaching the set point, a small change of duty cycle is necessary.
- When the output of the converter is near the set point and is approaching it rapidly, the duty cycle must be kept constant so as to prevent overshoot.
- When the set point is reached and the output is still changing, the duty cycle must be changed a little bit to prevent the output from moving away.
- When the set point is reached and the output is steady, the duty cycle remains unchanged.
- When the output is above the set point, the sign of change of duty cycle must be negative and vice versa.

Fuzzy memberships NL, NM, NS, ZE, PS, PM, PL are defined as negative large, negative medium, negative small, zero, positive small, positive medium and positive large.

VI. Simulation Results

The regulatory responses obtained by simulation using Matlab software with PI and fuzzy controls under supply and load disturbances are presented in this section. The simulated speed and armature current of PRC (Table 2) fed PMDC motor with PI control and set speed =750 rpm under sudden (10%) line disturbances (27V-30V-27V) on no load are shown in Fig. 3. The corresponding results with PI control and sudden load torque changes from 0.0981Nm to 0.10791Nm are shown in Fig. 4. Fig. 5 shows results on no load with fuzzy control for set speed =750 rpm and sudden (10%) line disturbances (27V-30V-27V). Corresponding responses for sudden load torque changes from 0.0981Nm to 0.10791Nm at t=0.02sec with 750 rpm set speed are shown in Fig. 6. Triangular memberships functions (Table 1) and centroid method of defuzzification are used in the FLC of this work.

Table 1: Fuzzy rule base

e \ ce	NL	NM	NS	ZE	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	Z
NM	NL	NL	NL	NM	NS	Z	PS
NS	NL	NL	NM	NS	Z	PS	PM
ZE	NL	NM	NS	Z	PS	PM	PL
PS	NM	NS	Z	PS	PM	PL	PL
PM	NS	Z	PS	PM	PL	PL	PL
PL	Z	PS	PM	PL	PL	PL	PL

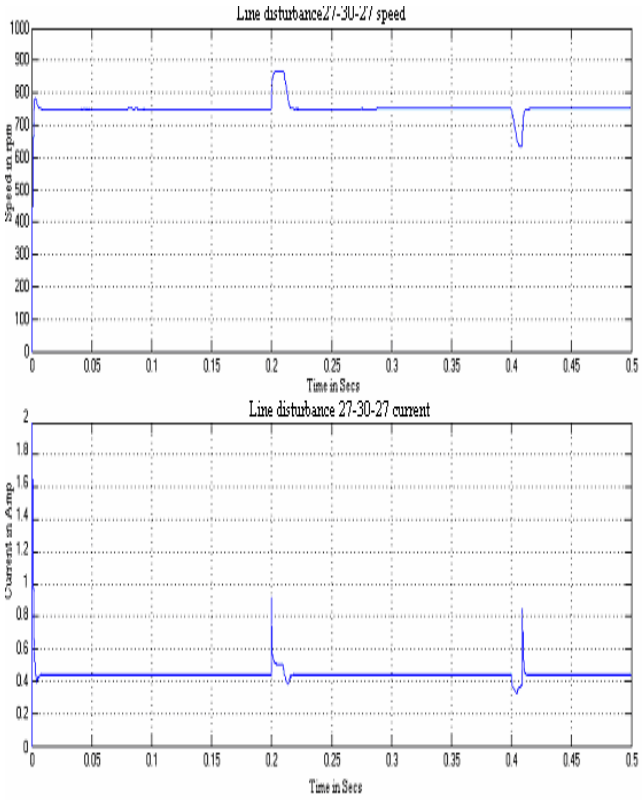

Fig. 3: Simulated transients in speed and current of PMDC motor on no load with sudden line disturbances (27V-30V-27V) at t=0.2sec and t=0.4sec with set speed 750 rpm

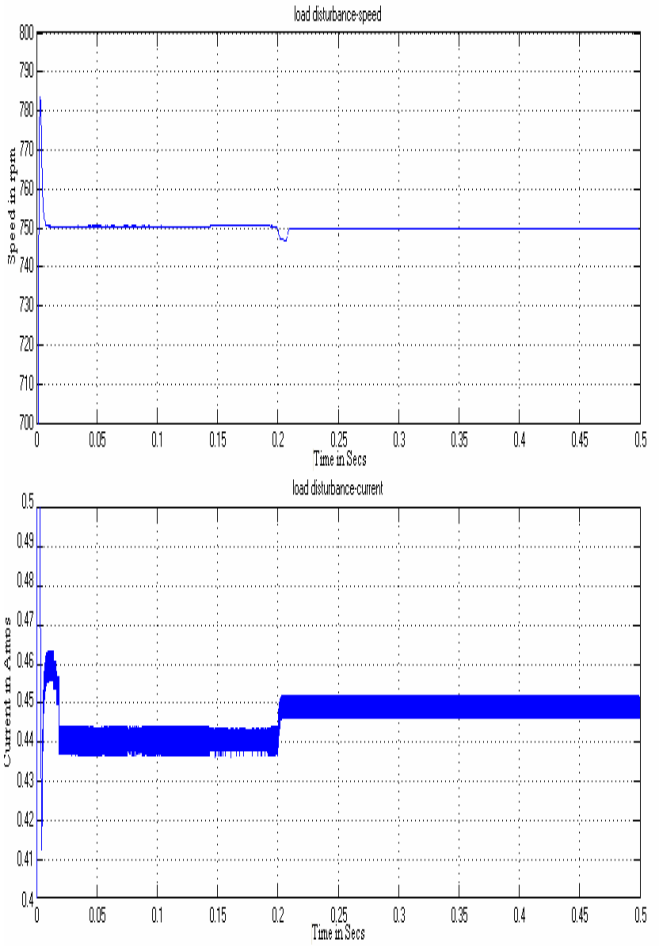

Fig. 4: Simulated speed and current of motor for sudden load torque changes from 0.0981Nm to 0.10791Nm at t=0.2sec with set speed 750 rpm

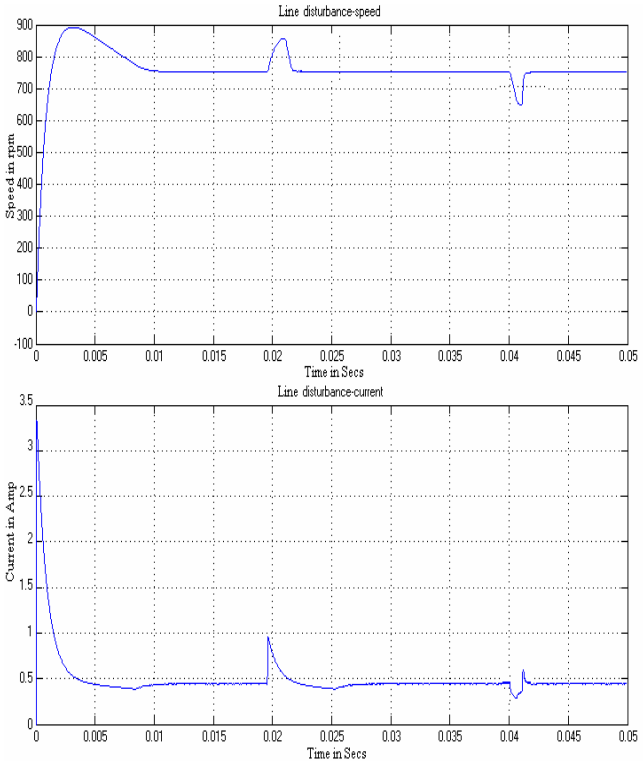

Fig. 5: Simulated transients in speed and current of PMDC motor on no load with sudden line disturbances (27V-30V-27V) at t=0.02sec and t=0.04sec with set speed 750 rpm

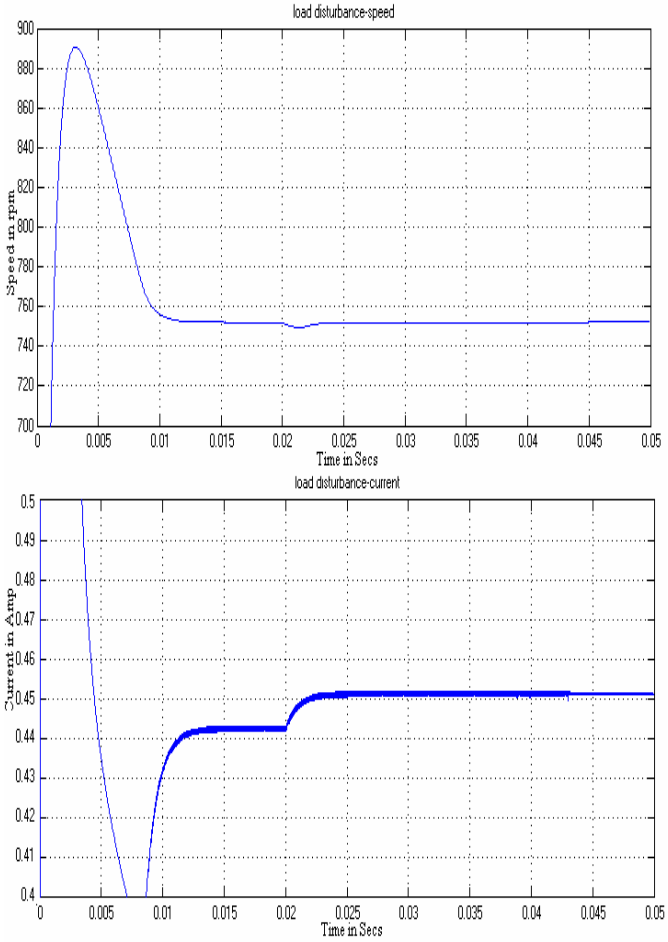

Fig. 6: Simulated speed and current transients for sudden load torque changes from 0.0981Nm to 0.10791Nm at t=0.02sec with set speed 750 rpm

VII. DSP Based Controllers

Hardware implementation of the PI and fuzzy controls for PRC fed PMDC motor carried out in this work using TMS320F2407 DSP is shown in Fig. 7. The PI and fuzzy controllers are designed to detect the speed variation (ω_e) using the ADC of the TMS320F2407 DSP. A drop in the actual speed (ω) triggers the controllers to increase the duty ratio of the converter thereby increasing the speed of the motor to reach the set point (ω^*). The actual speed after suitable signal conditioning is fed to the on-chip ADC of DSP. The signal conditioning circuit converts the actual speed to (0-3V) range to be fed as input to ADC. The error (ω_e) between the required speed (ω^*) and actual speed (ω) are manipulated by the TMS320F2407 DSP based controller to provide an appropriate change in duty ratio of the firing pulses to the MOSFETs so as to maintain the speed constant in spite of line and load variations.

The event manager module of the TMS320F2407 DSP generates the firing pulses. Optocouplers HCPL 4506 provides isolation between the event manager module of DSP and gates of MOSFETs. The PWM signal from the DSP is not capable of driving MOSFET. In order to strengthen the pulses, IR 2110 driver is used for each firing pulse. Fig. 8 shows the PWM pulses for Q_1 and Q_2 of PRC. Fig. 9 shows the experimental start up transient of the speed and current of parallel loaded resonant converter

fed PMDC motor. Fig. 10 shows the experimental responses for speed and current of the PRC fed PMDC motor on no load with PI control for step changes in supply voltage from 27V to 30V and vice versa. The next figure shows the corresponding transients for step load changes from 0.0981Nm to 0.10791Nm. The experimental regulatory responses for speed and current of PRC fed motor on no load with FLC for step changes in supply voltage from 27V to 30V and vice versa are displayed in Fig. 12. The corresponding regulatory responses for step load torque changes from 0.0981Nm to 0.10791Nm are portrayed in Fig. 13. The experimental waveforms after appropriate signal conditioning are obtained using 100MHz digital storage oscilloscope through software SW205-2 (Ver 1.4) with settings as in Figs. 8-13. The reference is marked with arrow at the right side. A 0.22 Ω, 5W current sensing resistor has been used.

Table 2: Circuit parameters of the test converter

PARAMETER	VALUE
Inductor L_s	101.7μH
Capacitor C_p	98.4nF
Capacitor C_f	45.4μF
Inductor L_f	1.44mH
Input voltage V_s	(0-30)V
Switching frequency f_s	60kHz
Duty ratio D	0.25-0.99
MOSFETs	IRFP9240
DIODEs	UF5042

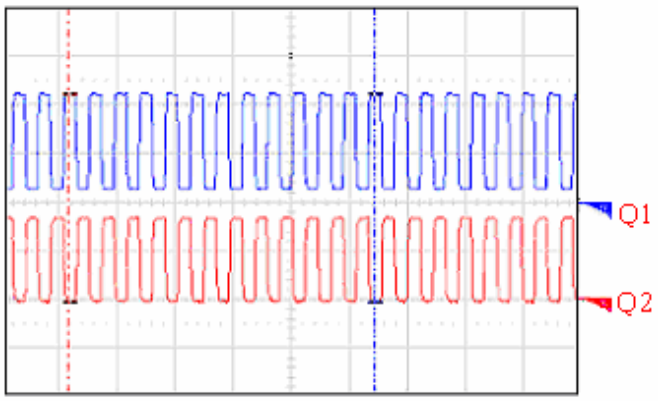

Fig. 8: PWM pulses for Q_1 (upper trace) and Q_2 (lower trace) of parallel loaded resonant converter feeding PMDC motor

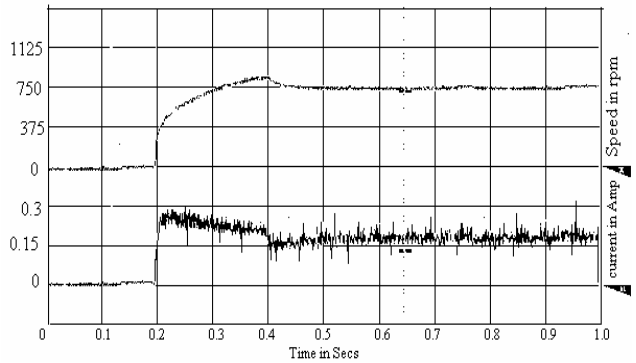

Fig. 9: Experimental start up transients of the speed and current of parallel loaded resonant converter fed PMDC motor

PI Controller

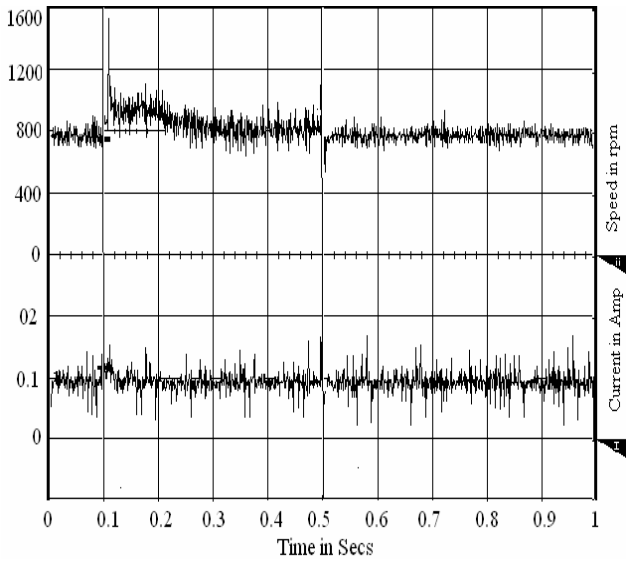

Fig. 10: Experimental transients in speed and current of motor on no load for step changes in supply voltage from 27V to 30V and vice versa

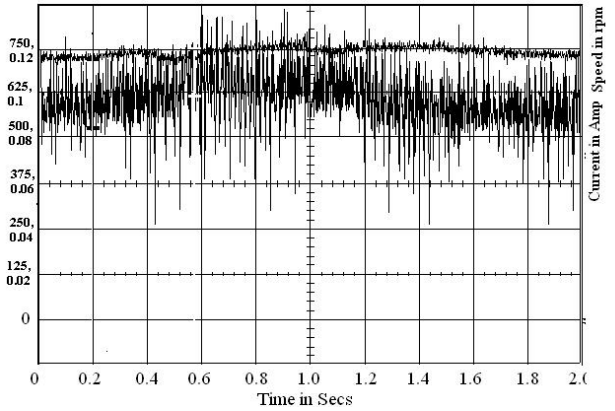

Fig. 11: Experimental transient responses of the speed and current of motor for step load changes from 0.0981Nm to 0.10791Nm

VIII. Conclusion

Armature current and peak overshot in speed are found to be larger in the simulated start-up of the PMDC motor on no load under sudden supply disturbances and sudden load disturbances with FLC than with the PI controller (Figs. 3-6). Such behaviors are not found to be present in the experimental responses (Figs. 10-13). Considerable noises due to switching are found to be superimposed only on experimental responses. The simulation and experimental results closely match and show that the proposed PI and fuzzy controllers regulate satisfactorily the speed of PRC fed PMDC motor irrespective of line and load disturbances. These establish the validity of the developed controllers that effectively reject disturbances in speed and load while achieving fast tracking of the speed. Performance evaluation of simulated controllers is carried out using speed related performance indices as reported in Table 3. It is found that FLC performs better for the chosen PMDC motor system.

Table 3: Performance evaluation of controllers for PRC fed PMDC motor using MATLAB

CONTROLLERS	Supply disturbances				Load disturbance	
	Supply increase (10%)		Supply decrease (10%)		Load changes from 0.0981Nm to 0.10791Nm	
	Peak overshoot (%)	Settling time (msecs)	Peak overshoot (%)	Settling time (msecs)	Peak overshoot (%)	Settling time (msecs)
PI	20	20	20	16.67	0.4	10
FUZZY	16	2.7	16	1.92	1.3	3.85

Fuzzy Controller

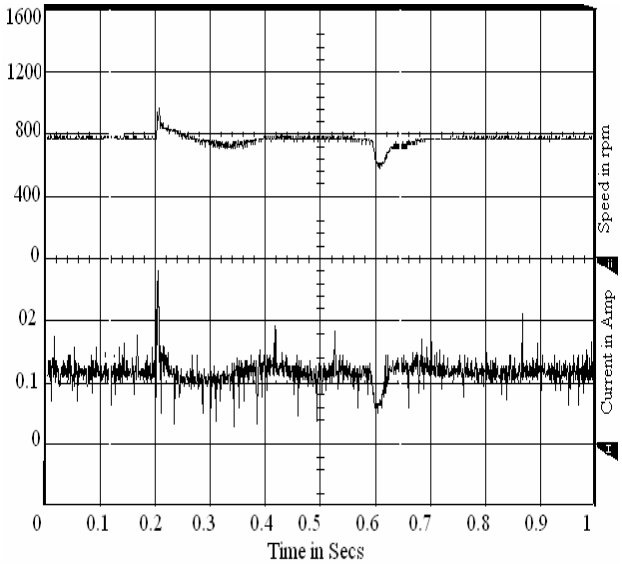

Fig. 12: Experimental transient responses of the speed and current of motor on no load for step changes in supply voltage from 27V to 30V and vice versa

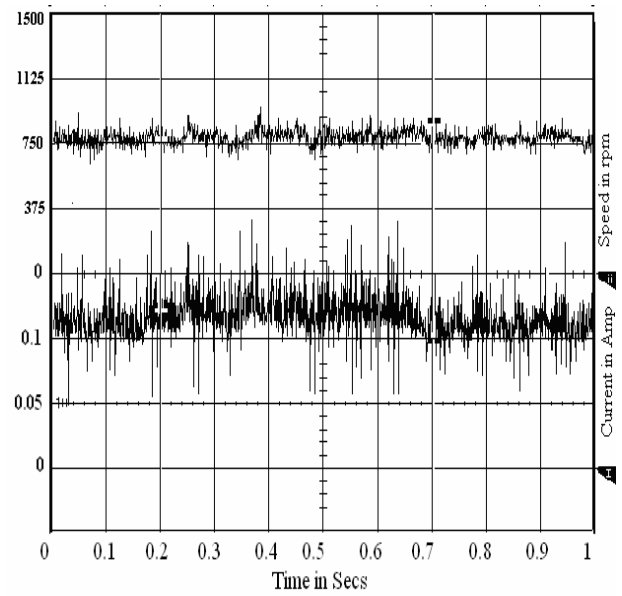

Fig. 13: Experimental transients in speed and current of motor for step load torque changes from 0.0981Nm to 0.10791Nm

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BIOGRAPHIES

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journals. His research interests are in modeling and control of DC-DC converters and multiple connected power electronic converters, control of Permanent Magnet Brushless DC motor, embedded control for multi level inverters and matrix converters etc. He is a life member of Instrument Society of India and Indian Society for Technical Education. He has completed an AICTE sponsored R & D project on "Investigations on Controllers for Permanent Magnet Brushless DC motor.

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Characterisation of Remote Loading Systems using a Nonlinear Analytical and Numerical Method

N. M. Murad [1] A. Celeste [1]

Abstract – Remote loading systems using an electromagnetic beam is affected by discontinuous piecewise constant loading voltage. The characteristics of these remote dynamic systems under charge are investigated. Varied behaviour of the systems with discontinuous charge is found due to environment perturbation compared to systems under continuous voltage charge with a wired link. A theoretical and numerical analysis is done in order to obtain the responses of the systems to various piecewise constant charge voltage under different initial conditions. Also, for such piecewise systems, the conditions of oscillation and the stability are given.

Keywords – Remote energy saving, nonlinear-dynamic loading systems, discontinuous charge voltage, piecewise constant variables, oscillation, numerical simulation.

I. INTRODUCTION

Generally, in many remote electronic systems, loadings acting on the remote systems are discontinuous and can be considered as piecewise constants in first approximation. But, the energy stocking could be often chaotic or non linear and is produced by piecewise discontinuous disturbances. Due to the characteristics of the discontinuous charge, loading of a dynamic system disturbed by the piecewise constant voltage shows an entirely different behavior from that of the corresponding continuous system. For example, the loading of the systems acted by piecewise constant loaded voltage can be very sensitive to initial conditions even for the linear dynamic systems. The peculiar behavior will be demonstrated for several linear and nonlinear dynamic systems under piecewise constant charges.

In a wireless sensor network, the dynamic system will be an intelligent node with an autonomous battery. This last is a remote loading with the help of an electromagnetic beam. Several mathematical methods exist to characterize these phenomena. Differential equations with piecewise constant arguments of retarded and advanced types such as $q([t])$ or $q([t \pm n])$ were proposed [1-8]. However, in the current literature, there is still a lack of systematic studies on the properties of charging of the remote dynamic systems subjected to piecewise loading voltage. A novel piecewise constant argument $[Nt]/N$ for analytically and numerically solving the second order differential equations which govern the nonlinear dynamic systems exerted by piecewise constant voltages is introduced [8]. With this piecewise constant argument, the gap between the dynamic systems subjected to continuous loadings and the systems under piecewise charges was filled.

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With the help of the piecewise constant argument $[Nt]/N$, the present work investigates the dynamic systems subjected to piecewise constant loading voltage with focus on the extraordinary behaviour of remote charging systems. Theoretical analysis of the properties of loading of remote dynamic systems under a piecewise constant charge voltage will be undertaken. For the safe of clarification the results of the corresponding loadings of the systems will be studied numerically and graphically with various combinations of coefficients in the equations of loading and different initial conditions so that the behaviour of the systems under piecewise constant voltage may be visualized and comprehensively understood. Throughout the present work, the exponential matrices to be derived characterize the oscillatory behavior of a system subjected to piecewise constant voltage.

This paper is organizer as follow. Mathematical formulation of the remote loading systems is expressed in section II for an approximate solution to a strongly non-linear second order differential equation [9-12]. Then, in section III, the loading of remote dynamical systems under sinusoidal piecewise constant voltage is studied and shown a divergent oscillatory behaviour. A stable remote loading system with constant amplitude could be obtained if the remote system gets low capacitance (section IV). In the section V, oscillatory loading of the dynamic systems will then be examined with the help of the diagrams of charge and piecewise constant voltage charge against time. The solutions obtained for the systems will be compared with those of the corresponding continuous systems. Finally, conclusions are made.

II. MATHEMATICAL FORMULATION

Characterization of a remote loading system could be physically governed by a differential equation (1) with piecewise constant arguments (PCA) originated by Cooke, Shah and Wiener [2, 7] reformulated in our case as

$$L\ddot{q} + R\dot{q} + C^{-1}q = F(t) \quad (1)$$

where

- L is the inductance of the system,
- R is the resistor coefficient,
- C is the capacitance,
- $F(t)$ is an excitation function.

Here, the relation $R^2 > 4LC^{-1}$ is assume in equation (1). In our case the PCA becomes an equation with piecewise constant voltage (PCV). The value of the PCV shown in the equation (1) can be calculated for any given time. The analysis of the properties of loading starts with these initial conditions

$$q(t = t_0) = q_0 \text{ and } \dot{q}(t = t_0) = i(t = t_0) = i_0 \quad (2)$$

Let's choose an arbitrary time segment $[Nt]/N \le t < ([Nt]+1)/N$ where $[\bullet]$ represents a function of greatest integer and N is an integer which controls the size of the time period on which the external charge is a constant. Then, solution of the linear system described by equation (1) is readily available. This entails that the loading in any time interval represents a portion of a linear charging. At the ending point of an interval, the charge and current of the system are given by $q(([Nt]+1)/N)$ and $\dot{q}(([Nt]+1)/N)$ respectively.

For the loading of the next time interval, these particular results become in turn the starting conditions or the local initial conditions. The loading in the follow-up intervals can then be consequently obtained with the local initial conditions and so on.

Considering that the remote loading of the system is continuous, i.e., $q(t)$ and $\dot{q}(t)$ are continuous on $t \in [0,\infty]$, the following conditions of continuity must be satisfied

$$\begin{cases} q_{[Nt]}\left(\dfrac{[Nt]}{N}\right) = q_{[Nt]-1}\left(\dfrac{[Nt]}{N}\right) \\ \dot{q}_{[Nt]}\left(\dfrac{[Nt]}{N}\right) = \dot{q}_{[Nt]-1}\left(\dfrac{[Nt]}{N}\right) \end{cases} \tag{3}$$

III. Loading of Remote Dynamical Systems Under Sinusoidal PCV

Considering, the remote loading system is excited by a piecewise sinusoidal voltage, the following function must satisfied $F(t) = \rho\cos\left(\omega\dfrac{[Nt]}{N}\right)$ where ρ is the amplitude of the piecewise constant charge. So, the remote system is acting by a sinusoidal varying PCV. It is independent of the charge $q(t)$. The solution of equation (1) for the entire time range considered can be derived as equation (4) with the continuity conditions and the solutions for each of the time intervals

$$q(t) = e^{-\alpha\left(t-\frac{[Nt]}{N}\right)}\cdot A\cdot B + \frac{\rho}{\omega_0^2}\cos\left(\omega\frac{[Nt]}{N}\right)e^{-\alpha\left(t-\frac{[Nt]}{N}\right)}\cdot \left[e^{-\alpha\left(t-\frac{[Nt]}{N}\right)} - \cos\left(\tau\left(t-\frac{[Nt]}{N}\right)\right) - \frac{\alpha}{\tau}\sin\left(\tau\left(t-\frac{[Nt]}{N}\right)\right)\right] \tag{4}$$

where $\omega_0 = (LC)^{-\frac{1}{2}}$, $\alpha = \dfrac{R}{2L}$, $\tau = \sqrt{\omega_0^2 - \alpha^2}$ and the matrix A is written as

$$A^T = \begin{bmatrix} \cos\left(\tau\left(t-\dfrac{[Nt]}{N}\right)\right) + \dfrac{\alpha}{\tau}\sin\left(\tau\left(t-\dfrac{[Nt]}{N}\right)\right) \\ \dfrac{1}{\tau}\sin\left(\tau\left(t-\dfrac{[Nt]}{N}\right)\right) \end{bmatrix} \tag{5}$$

Also, the matrix B in equation (4) takes the following form

$$B = e^{-\alpha\frac{[Nt]}{N}}D^{[Nt]}\begin{bmatrix} q_0 \\ i_0 \end{bmatrix} + \sum_{m=1}^{[N_t]}\frac{\rho}{\omega_0^2}e^{-\alpha\frac{m}{N}}D^{m-1}\begin{bmatrix} e^{\frac{\alpha}{N}}-\cos\frac{\tau}{N}-\frac{\alpha}{\tau}\sin\frac{\tau}{N} \\ \left(\dfrac{\alpha^2}{\tau}+\tau\right)\sin\dfrac{\tau}{N} \end{bmatrix}\cos(\omega([Nt]-m)) \tag{6}$$

And the square matrix D has the form like

$$D = \begin{bmatrix} \cos\dfrac{\tau}{N} + \dfrac{\alpha}{\tau}\sin\dfrac{\tau}{N} & \dfrac{1}{\tau}\sin\dfrac{\tau}{N} \\ -\left(\dfrac{\alpha^2}{\tau}+\tau\right)\sin\dfrac{\tau}{N} & \cos\dfrac{\tau}{N} - \dfrac{\alpha}{\tau}\sin\dfrac{\tau}{N} \end{bmatrix} \tag{7}$$

A simple case of remote loading without damping is studied by substituting the values of system parameters and time into the analytical solution equation (4). Then, the remote loading of the systems governed by equation (1) could be seen in figure 1 with the help of [13].

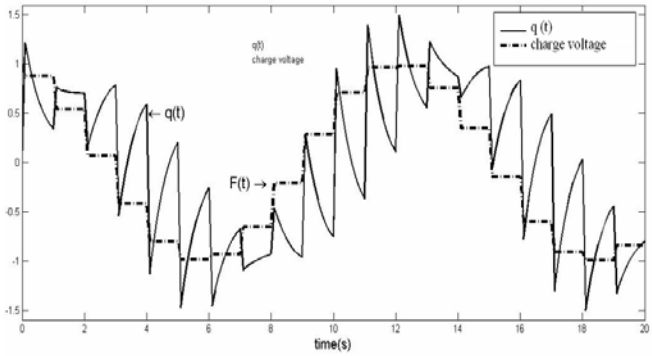

Fig. 1 : Charge and piecewise constant voltage acting on a remote loading system versus time with L=1, R=1, N=1, C=1, $\rho = 1$, $\omega = 1$

Fig. 1 expresses the charge versus time and also the piecewise constant voltage based on the solution of equation(1). One seen that the curve of charge is continuous everywhere for $t \ge 0$ under the discontinuous piecewise constant charge. Moreover, the charge shows slope discontinuities at the integer points of time. The discontinuities are a consequence of the discontinuous piecewise constant voltage acting on the system. In addition, charge plot follows asymptotically an oscillatory behavior. When *F(t)* decreases from maximum peak to the minimum peak, the remote system tends to take charge. Unlike when *F(t)* increases, the system tends to unload. It could be seen one second delay between the charge and *F(t)* due to the inertia of the system to load.

IV. Stable Remote Loading System with Constant Amplitude

Under certain conditions, the remote dynamic system subjected to piecewise constant voltage may behave as a simple loading system with stable remote loading of constant amplitude. Here a similar system is considered as section III, but with a higher C ($C > 1$).

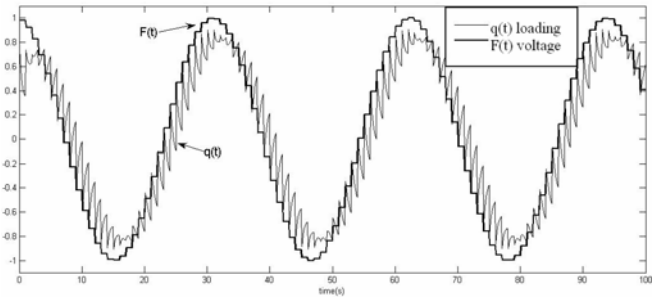

Fig. 2 : Charge and the corresponding piecewise constant voltage acting on a remote loading system with L=4, R=3, N=1, C=5, $\rho = 1$, $\omega = 0.2$.

From figure 2, this remote loading system shows a stable oscillatory loading under the same conditions as previous section and after a relatively long time from t=0. Even though the shapes of the stepwise charges are different from period to period, the waveforms of the charge are repeating precisely with a period of 2π. When the external piecewise constant charge is charge related, the complete solution for a time interval of the system must first be obtained so that the end conditions for this interval, and the starting conditions of the consecutive interval, may be determined accordingly. Also, a higher C makes stable the remote loading system with constant amplitude.

V. Remote Damped Loading System Subjected to a PCV

Generally, loading of a remote dynamic system subjected to a PCV displays a dramatically different behavior from those of the corresponding system exerted by continuous voltage. Compare a damped loading system subjected to a PCV described by the equation of charge:

$$L\ddot{q} + R\dot{q} + C^{-1}q = \rho q\left(\frac{[Nt]}{N}\right) \tag{8}$$

with a similar linear loading system governed by the following equation of charge

$$L\ddot{q} + R\dot{q} + C^{-1}q = \rho q(t) \tag{9}$$

where R, L, C and ρ are constants of the system's physical properties. Equations (5) and (6) verify $R^2 > 4LC^{-1}$. The solution of the linear system in equation (6) is readily available and the solution of equation (5) can be derived as follows:

$$q(t) = e^{-\alpha t}\left\{(1-\rho C)\left[\cos\left(\tau\left(t-\frac{[Nt]}{N}\right)\right)+\frac{\alpha}{\tau}\sin\left(\tau\left(t-\frac{[Nt]}{N}\right)\right)\right]\right.$$
$$\left.+\frac{\rho C}{\tau}e^{-\alpha\left(t-\frac{[Nt]}{N}\right)}\sin\left(\tau\left(t-\frac{[Nt]}{N}\right)\right)\right\}G^{[N_t]}\begin{bmatrix}q_0\\ i_0\end{bmatrix} \tag{10}$$

In equation (10), the constants α and τ are the same as those defined in equation (4) and the square matrix G takes the form

$$G=\begin{bmatrix}\rho Ce^{-\alpha}+(1-\rho C)\cos\left(\tau-\frac{\alpha}{\tau}\right)\sin\tau & \frac{\sin\tau}{\tau}\\ -(1-\rho C)\left(\frac{\alpha^2}{\tau}+\tau\right)\sin\tau & \cos\left(\tau-\frac{\alpha}{\tau}\right)\sin\tau\end{bmatrix} \tag{11}$$

A. Simple case without resistive load

A no resistive loading remote system is governed by the following differential equation

$$L\ddot{q} + C^{-1}q = \rho q\left(\frac{[Nt]}{N}\right) \tag{12}$$

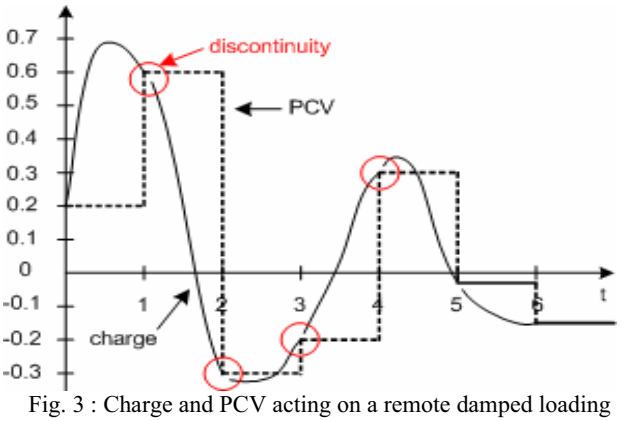

Fig. 3 : Charge and PCV acting on a remote damped loading system versus time with L=1, R=0, N=1, C=0.25, $\rho = 1$, $\omega = 0.2$

The charge of such remote loading system shows discontinuity at the integer point of time (Fig. 3). As displayed, the PCV exerting on the system has the same value as the charge at the integer point of time, and the corresponding loading in this case is asymptotically convergent.

B. Comparison of constant amplitude continuous loading system versus PCV loading system

Continuous system and the PCV remote loading system is compared under constant amplitude (Fig. 4). The loading with the PCV $F(t) = -10q\left(\frac{[Nt]}{N}\right)$ diverges asymptotically. Conversely, the charge under the continuous voltage $-10q(t)$ is damped out rapidly with time.

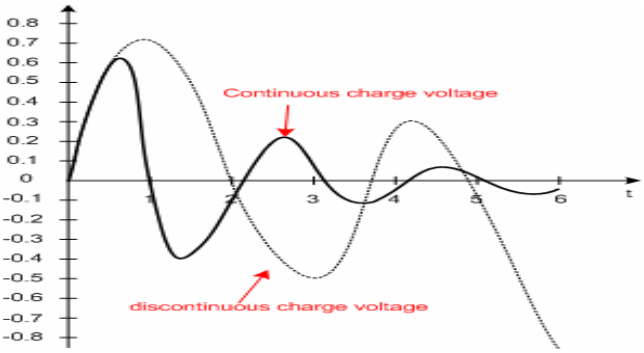

Fig. 4 : Comparison of the loading of the system subjected to PCV versus continuous charge voltage with L=1, R=1, N=1, C=0.66, $\rho = -10$

C. Comparison of sinusoidal continuous loading system versus sinusoidal PCV loading system

For the remote loading systems subjected to known forms of piecewise constant and continuous voltage respectively, such as $\rho\cos\left(\omega\frac{[Nt]}{N}\right)$ and $\rho\cos(\omega t)$ which are merely time dependent, the comparison is also evident. As an example, the lading of the system governed by equation (1) is compared with the following system subjected to a continuous voltage,

$$L\ddot{q}(t) + R\dot{q}(t) + C^{-1}q(t) = \rho\cos(\omega t), \tag{13}$$

as shown in Fig. 5. It can be observed that the loading of the system subjected to the continuous voltage and system

under the PCV oscillates and becomes a damped steady-state oscillation with identical shape as time increases up to t=4s. After this time, the waveform of the PCV loading system becomes divergent.

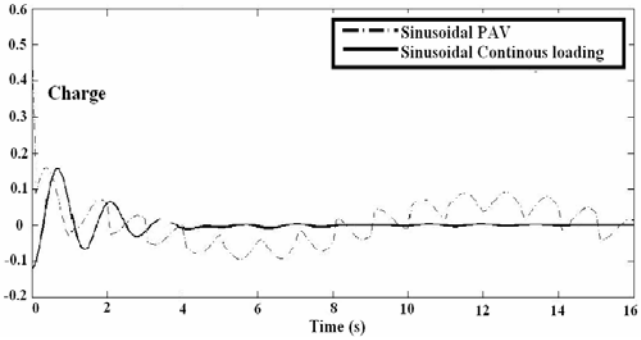

Fig. 5 : Comparison of the loading of the system subjected to piecewise constant voltage versus continuous charge voltage with L=1, R=0.5, N=1, *C*=20, $\rho = 1$, $\omega = 0.5$

VI. Conclusion

This study is conducted to investigate the characteristics of the remote loading of the linear and nonlinear dynamic systems subjected to piecewise constant charges voltages. Solutions for the remote dynamic systems with PCV are developed with the piecewise constant argument $\frac{[Nt]}{N}$. Moreover, the systems expressed in equations (1) and (5) may also be continuous systems when N tends to infinity as described in [3]. The solutions in the form of equations (4) and (10) with finite *N* values are unique and become the specific piecewise constant systems as those studied in [1, 2, 5]. As such, the solutions in the forms of equations (4) and (10) bridge the gap between the piecewise constant systems and continuous systems. Extraordinary behaviours of the remote dynamic systems are found in the study in comparing with the dynamic systems under continuous voltages, hence the difficulty in finding appropriate physical interpretation of the model.

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Biographies

N. M. Murad was born in Saint Denis of La Réunion, France in 1974. He received his PhD in communication & electronics at the Ecole Nationale Supérieure des Télécommunications (Telecom Paris), in 2001. From 1998 to 2001, as an engineer R&D in radio operator mobile it worked at Alcatel CIT where it prepared his doctoral thesis with Télécom Paris in parallel.
Between 2001 and 2003, he worked as a teacher and research at the University of La Reunion where he had co-responsibility on the coupling between energy and telecommunication project with Dr. Celeste. During 2004 to 2007, he is an assistant professor researcher at the 3IL school of engineer and researcher at the XLIM/OSA.
Since September 2007, he is an assistant professor researcher at the University of Reunion. Its research relates to the numerical communication, the signal and information theory with a specific accent on the wireless communications (UMTS, CDMAone, LMDS, 802.16,…), spread spectral techniques, synchronisation, MIMO system, spatial and polarization diversity, wireless energy transportation, wireless mobile network and wireless sensor network.

Alain Celeste was born in Lyon, France, in 1965. In 1987, he graduated as an Engineer in Physics from the National Institute of Applied Sciences (INSA), in Toulouse, France. In 1990, he received a Ph.D. in Solid State Physics from the University of Toulouse, for his work on resonant tunnelling in semiconductor heterojunctions. He then started to work on microwave characterization of dielectric materials using waveguide loading techniques, during his military service. Since 1994, he is an Assistant Professor at the University of La Reunion, in charge of the Wireless Power Transmission research field and teaching digital electronics and microprocessor architecture. His current interests are wireless power transmission for remote power provision to smart sensors and communicating devices.

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