A Fast Space-Vector Pulse with Modulation Method for Diode-Clamped Multi-level Inverter fed Induction Motor

P. Satish Kumar [1] J. Amarnath [2] S.V.L. Narasimham [3]

Abstract – This paper presents a fast space-vector pulse width modulation (SVPWM) method for five-level inverter. In this method, the space vector diagram of the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. After decomposition, all the remaining necessary procedures for the three-level SVPWM are done like conventional two-level inverter. The proposed method reduces the algorithm complexity and the execution time. It can be applied to the multi-level inverters above the five-level also. The experimental setup for three-level diode-clamped inverter is developed using TMS320LF2407 DSP controller and the experimental results are analyzed. The results have been good agreement with the published work.

Keywords – Five-level inverter, space vector pulse wide modulation, diode clamped inverter.

I. INTRODUCTION

Recent developments in power electronics and semiconductor technology have led improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have become popular and considerable interest by researcher are given on them. Three-level voltage fed PWM inverters are recently showing popularity for multi-megawatt industrial drive applications. The main reason for this popularity is that the output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion and large voltage between the series devices is easily shared [1]. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently [2], [3]. This technique results in higher magnitude of fundamental output voltage available compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states [4].

In SVPWM method the output voltage is approximated by using the nearest three output vectors that the nodes of the triangle containing the reference vector in the space vector diagram of the inverter. When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location.

The paper first received 17 July 2009 and in revised form 11 March 2010. Digital Ref: A170601236

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Thus the computational complexity is greatly increasing with the increasing number of the reference vectors and it is a main limitation of the application of this typical SVPWM [6],[10]. In this paper, a new method is proposed in which the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. Thus the remaining necessary procedures for the five-level SVPWM are done like conventional two-level inverter. This modification can reduce considerably the computational time and reduce the algorithm complexity. We use the redundancy of certain vectors of the space vector diagram of the inverter in order to ensure the stabilization of the input DC voltages of the inverter.

II. FIVE-LEVEL SVPWM INVERTER

Fig.1 shows diagram of a five-level diode clamping inverter. Each leg is composed of four upper and lower switches with anti-parallel diodes. Four series *dc*-link capacitors split the *dc*-bus voltage in half, and eighteen clamping diodes confine the voltages across the switches within the voltages of the capacitors. The necessary conditions for the switching states for the five-level inverter are that the *dc*-link capacitors should not be shorted, and the output current should be continuous. As indicated in Table I, each leg of the inverter can have five possible switching states, P_1, P_2, O, N_1 or N_2. When the top four witches Sx_1, Sx_2, Sx_3 and Sx_4 ($x = a, b, c$) are turned on, switching state is P_2. When the switches Sx_2, Sx_3, Sx_4 and Sx_5 are turned on switching state is P_1. When the switches Sx_3, Sx_4, Sx_5 and Sx_6 are turned on, the switching state is O. when the switches Sx_4, Sx_5, Sx_6 and Sx_7 are turned on, the switching state is N_1. When the switches Sx_5, Sx_6, Sx_7 and Sx_8 are turned on, the switching state is N_2.

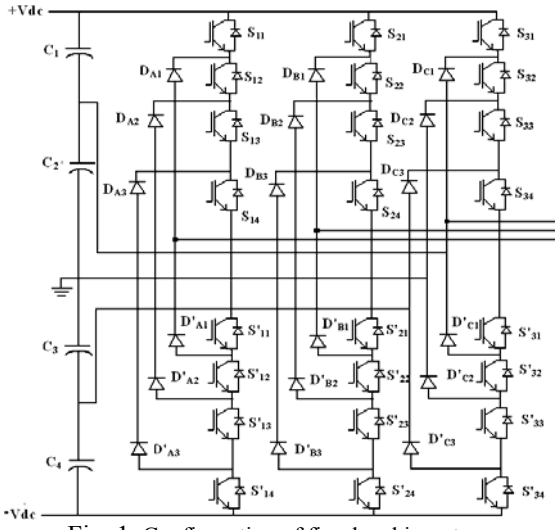

Fig. 1: Configuration of five-level inverter

Table 1: Switching states and teriminal voltages of five-level inverter

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{xo}
P_2	1	1	1	1	0	0	0	0	2E
P_1	0	1	1	1	1	0	0	0	E
O	0	0	1	1	1	1	0	0	0
N_1	0	0	0	1	1	1	1	0	-E
N_2	0	0	0	0	1	1	1	1	-2E

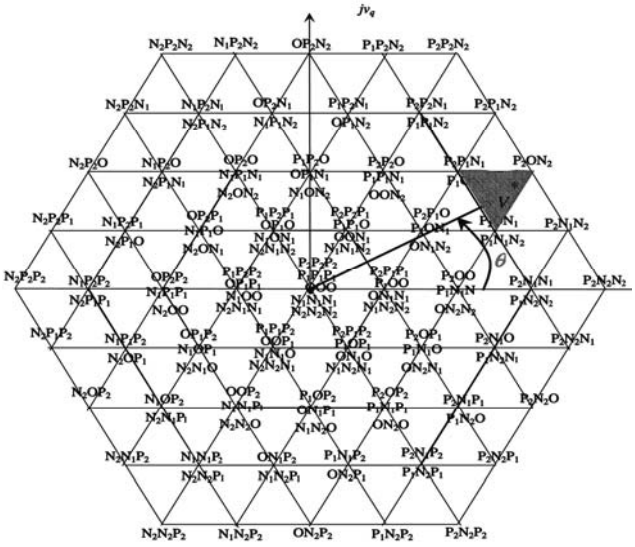

Fig. 2: Space vector diagram of five-level inverter

Fig. 2 shows the space vector diagram for five-level inverter. The output voltage space vector is identified by combination of switching states P_2, P_1, O, N_1 or N_2 of the three legs. For example, in the case of P_2ON_1, the output terminals a, b and c have the potentials $2E$, 0, and $-E$ respectively. Since five kinds of switching states exist in each leg, three-level inverter has $5^3 = 125$ switching states, as indicated in Fig. 2. The output voltage vector can take only 61 discrete positions in the diagram because some switches states are redundant and create the same space vector. In Fig. 2, it is also indicated an arbitrary reference vector V^* to be generated by the inverter.

III. FAST SPACE VECTOR PULSE WIDTH MODULATION METHOD

A. Basic Principle of Proposed SVPWM Method

The space vector diagram of multilevel inverter can be divided into different forms of sub-diagrams, in such a manner that the space vector modulation becomes more simple and easy to implement, as made in several works [5–9]. But these works do not reach a generalization of the two-level SVPWM to the case of multilevel inverters; either they divide the diagram into triangles, or into interfered geometrical forms. In this work, we present a simple and fast method that divides the space vector diagram of five-level inverter, within two steps, into several small hexagons, each hexagon being space vector diagram of two-level inverter, as shown in Fig. 3. This method is the extension of that presented in [12] for the case of three-level inverter. We have to make two simplifications: Firstly, the space vector diagram of five-level inverter is divided into six space vector diagrams of three-level inverters. Secondly, each one of these three-level inverter diagrams is divided into six space vector diagrams of two level inverters.

Thus the space vector modulation of five-level inverter becomes very simple and similar to that of conventional two-level inverter space vector modulation. To each this simplification, two steps have to be done. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the hexagons. Secondly we translate the origin of the reference voltage vector towards the centre of the selected hexagon. These steps are explained in the next section.

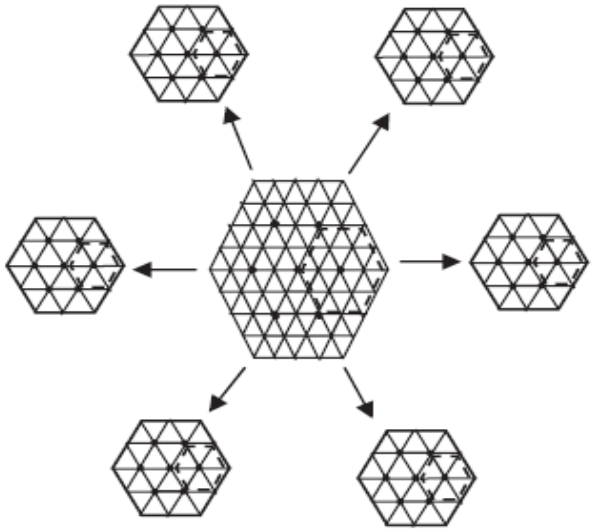

Fig. 3: Decomposition of space vector diagram of five-level inverter to six hexagons

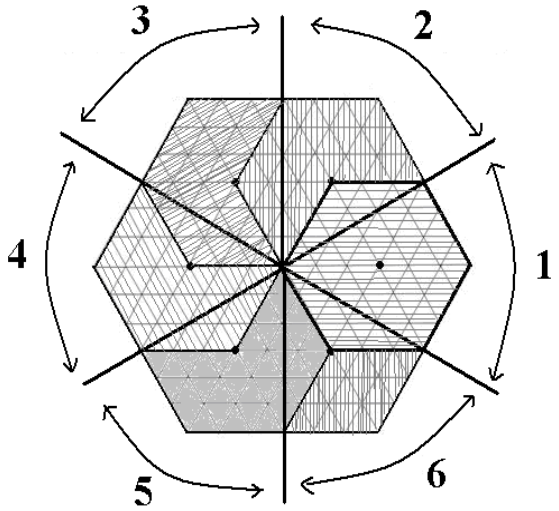

Fig. 4: Division of overlapped regions

B. First Correction of Reference Voltage Vector

Having the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that contain the five-level space vector diagram Fig. 3. There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided in equality between the two hexagons as shown in Fig. 4. Each hexagon is identified by a number s defined as given in Table 2.

Table 2: Selection of hexagons based on angle 'θ'

Hexagon 'S'	Location of reference voltage vector phase angle 'θ'
1	$-\pi/6 < \theta < \pi/6$
2	$\pi/6 < \theta < \pi/2$
3	$\pi/2 < \theta < 5\pi/6$
4	$5\pi/6 < \theta < 7\pi/6$
5	$7\pi/6 < \theta < 3\pi/2$
6	$3\pi/2 < \theta < -\pi/6$

After selection of one hexagon, we make a translation of the reference vector ***V**** towards the center of this hexagon, as indicated in Fig. 5. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table 3 gives the components *d* and *q* of the reference voltage $\mathbf{V}^{3}$* after translation, for all the six hexagons. The index (3) or (5) above the components indicate three or five-level cases respectively.

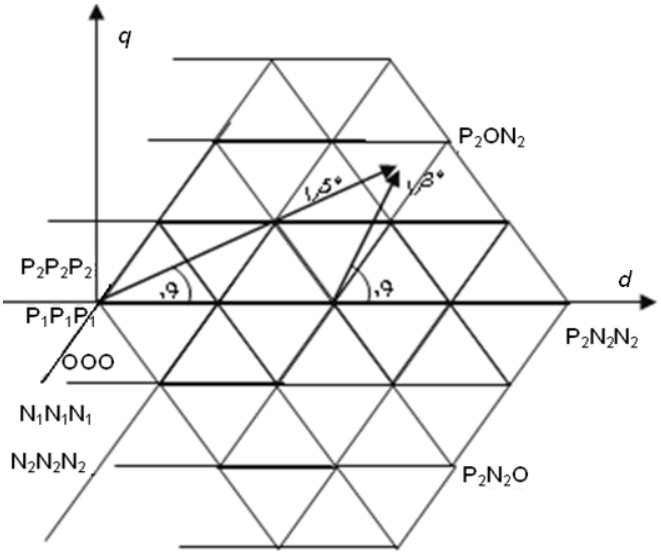

Fig. 5: First Translation of Reference Voltage Vector

Table 3: First Correction of Reference Voltage Vector

S	V_d^{3*}	V_q^{3*}
1	V_d^{5*} -1/2 cos(0)	V_q^{5*}-1/2 sin(0)
2	V_d^{5*}-1/2 cos (π/3)	V_q^{5*}-1/2 sin(π/3)
3	V_d^{5*}-1/2 cos(2π/3)	V_q^{5*}-1/2 sin(2π/3)
4	V_d^{5*}-1/2 cos(π)	V_q^{5*}-1/2 sin(π)
5	V_d^{5*}-1/2 cos(4π/3)	V_q^{5*}-1/2 sin(4π/3)
6	V_d^{5*}-1/2 cos(5π/3)	V_q^{5*}-1/2 sin(5π/3)

C. Second Correction of Reference Voltage Vector

Having the selected three-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this three-level diagram Fig. 7. Here also the overlapped regions are equally divided between the two hexagons. After selection of one hexagon, we make a translation of the reference vector V***** towards the center of this hexagon, as indicated in Fig. 7. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table IV gives the components d and q of the reference voltage V^{2}* after translation, for all the six hexagons. The index (2) or (3) above the components indicate two or three-level cases respectively.

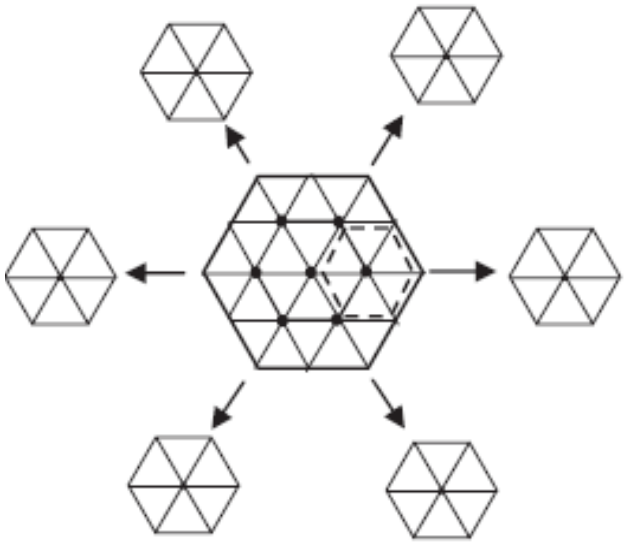

Fig. 6: Decomposition of space vector diagram of three-level inverter to six hexagons

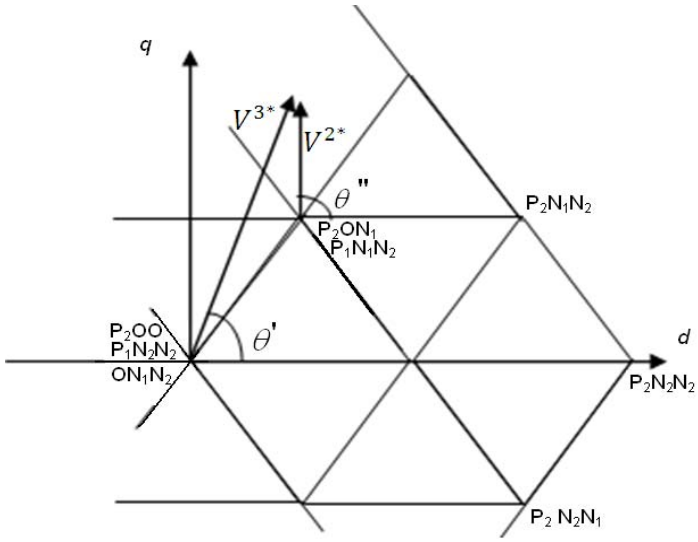

Fig. 7: Second Translation of Reference Voltage Vector

Table 4: First Correction of Reference Voltage Vector

S	V_d^{2*}	V_q^{2*}
1	V_d^{3*} -1/4 cos(0)	V_q^{3*}-1/4 sin(0)
2	V_d^{3*}-1/4 cos(π/3)	V_q^{3*}-1/4 sin(π/3)
3	V_d^{3*}-1/4 cos(2π/3)	V_q^{3*}-1/4 sin(2π/3)
4	V_d^{3*}-1/4 cos(π)	V_q^{3*}-1/4 sin(π)
5	V_d^{3*}-1/4 cos(4π/3)	V_q^{3*}-1/4 sin(4π/3)
6	V_d^{3*}-1/4 cos(5π/3)	V_q^{3*}-1/4 sin(5π/3)

D. Determination of Dwelling Times

Once the corrected reference voltage V^{2}* and the corresponding hexagon are determined, we can apply the conventional two-level space vector PWM method to calculate the dwelling times, the only difference between the two-level SVPWM and the five-level SVPWM is the factor 4 appearing at the first two equations as shown in equation 1. Since the dwelling timings of two-level inverter are divided by the value ¼. The remaining procedure is implemented like conventional two-level inverter SVPWM method and two level equivalent pulses are obtained.

$$T_1 = 4 * \left[\frac{\left| \vec{V^{2*}} \right| \cdot T_s \cdot \sin\left(\frac{\pi}{3} - \alpha \right)}{\sin\left(\frac{\pi}{3} \right)} \right]$$

$$T_2 = 4 * \left[\frac{\left| \vec{V^{2*}} \right| \cdot T_s \cdot \sin(\alpha)}{\sin\left(\frac{\pi}{3} \right)} \right] \quad (1)$$

$$T_0 = T_s - T_1 - T_2$$

E. Convertion and Sequence of the Switching States

This process is implemented by first considering each three-level decomposed space vector diagram of five-level space vector diagram based on value of 's'. Secondly, each three-level space vector diagram is further decomposed into six two-level space vector diagrams. Finally, the switching states of each two-level decomposed space vector diagrams are mapped as shown in Fig. 8 and switching states are changed in to its equivalent two-level switching states.

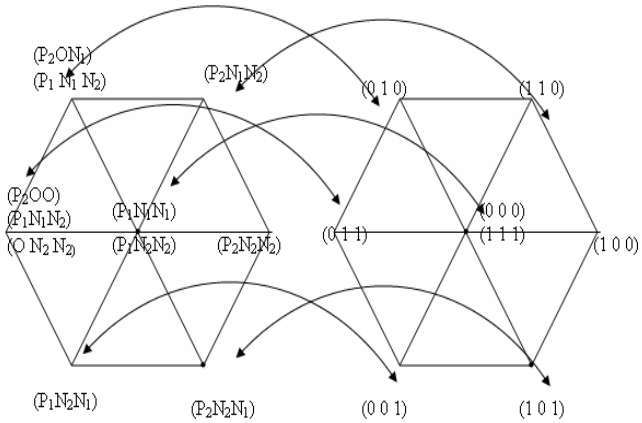

Fig. 8: Mapping of five-level switching states in to two-level switching states

The reference voltage vector V_2* is approximated using the nearest three states, which are nodes of the triangle containing the vector, identified as *X*, *Y* , and *Z*, For example, in the case of Fig. 8 , *X* is either the state P_2ON_1 or $P_1N_1N_2$, *Y* is the state P_2ON_2, while *Z* is either he state $P_2P_1N_1$ or the state P_1ON_2. The optimum sequence of these three states is selected so as to minimize the total number of switching transitions and fully optimize the harmonic profile of the output voltage. Note that from two level space vector modulation theory, it is well known that these sequences should be reversed in the next switching interval for minimum harmonic impact as given in [11-12].

Table 5: Simulation Parameters

SVPWM Parameters	Modulation index $m = 0.8$
	DC Supply voltage E = 400V
	No. of switching intervals $n = 120$
Induction motor	5.4 HP; 4 pole; 1430 rpm; $f = 50$ Hz
	$R_s = 1.405\ \Omega$; $R_r = 1.395\ \Omega$;
	$l_s = l_r = 0.005839$ H; $l_m = 0.1722$ H
SVPWM Parameters	Modulation index $m = 0.8$

IV. EXPERIMENTAL TEST SETUP

The experimental setup employed a powerful TMS320LF2407, 16-bit DSP processor working at 40 MIPS as its controller and PEC16DSMO10A, an intelligent power module (IPM) of three phase three-level diode clamped inverter. It consists of 12No's, 1200V, 50A IGBT with proper heat sink and snubber circuit. Three number of Hall Effect sensors are provided for current measurement and protection. The inverter is connected to a load of 3Ø, 0.5HP, 415V, 50 Hz, 4-pole, 1.05A, 1380 rpm induction motor and the results are obtained. The experimental setup has done only for three-level inverter as shown in Fig. 9.

Fig. 9: Experimental setup of three-level inverter

V. RESULTS AND DISCUSSIONS

In order to prove the validity of the proposed fast space vector pulse width modulation (SVPWM) method, a three phase three-level and five-level inverter fed induction motor is simulated with the simulation parameters shown in Table V. The simulation results of five-level inverter are shown in Fig. 10- 13. The gate pulses of phase A are shown in Fig. 10. The inverter output line to line voltage (V_{ab}) and its harmonic spectrum is shown in Fig. 11. The total harmonic distortion (THD) is only 0.64% and it proves the effectiveness of the proposed SVPWM method. Fig. 12 shows the load current and its harmonic spectrum. The THD of load current is decreased with increasing the level of inverter. The speed, torque and stator currents of induction motor are shown in Fig. 13. The speed and torque pulsations are reduced as comparing with two level inverter. The simulation results of three-level inverter are shown in Fig. 14 and Fig. 15. The output line to line voltage (V_{ab}) and its harmonic spectrum is shown in Fig. 14. The stator current and its harmonic spectrum of induction motor are shown in Fig. 15. In addition o the simulation results of five-level inverter, an experimental set up has developed and results are obtained for three-level inverter, when a 3Ø, 0.5HP, 415V, 50 Hz, 4-pole, 1.05A, 1380 rpm induction motor is connected as load. The output line to line voltage V_{ab} and V_{cb} are shown in Fig. 15. The induction motor load currents I_{ab} and I_{bc} are shown in Fig. 16.

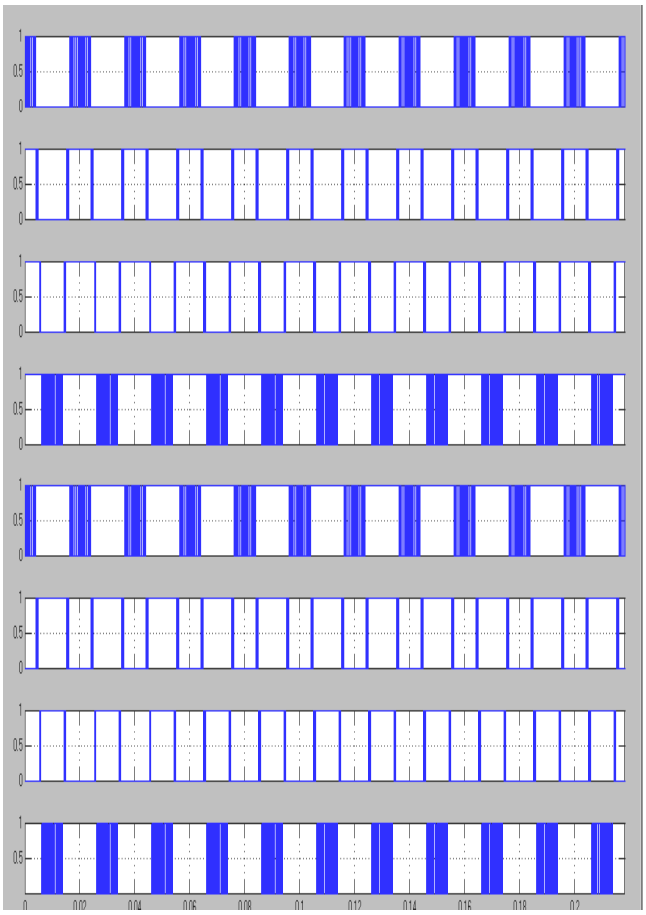

Fig. 10: Gate pulses for phase-A of five-level inverter

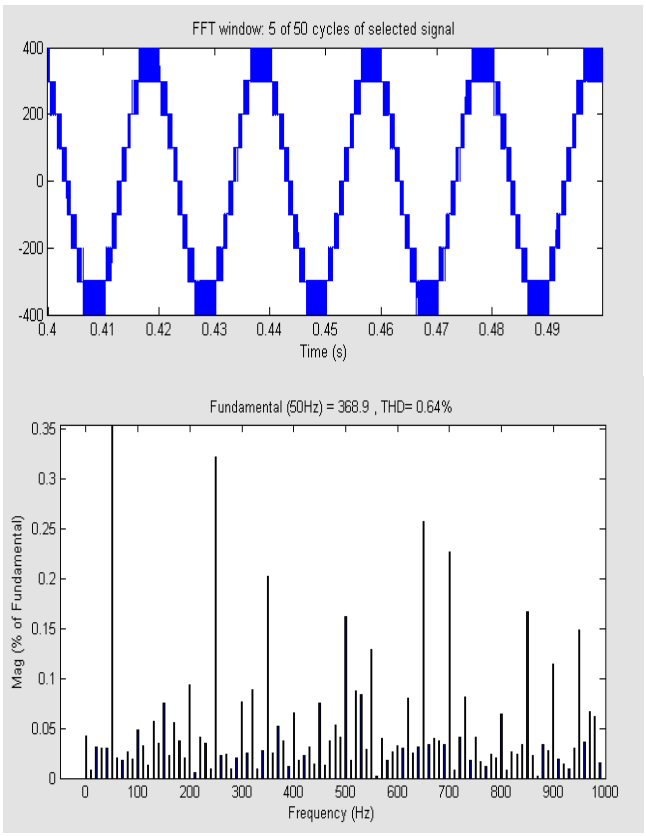

Fig. 11: The line to line voltage (V_{ab}) and its harmonic spectrum of five-level inverter

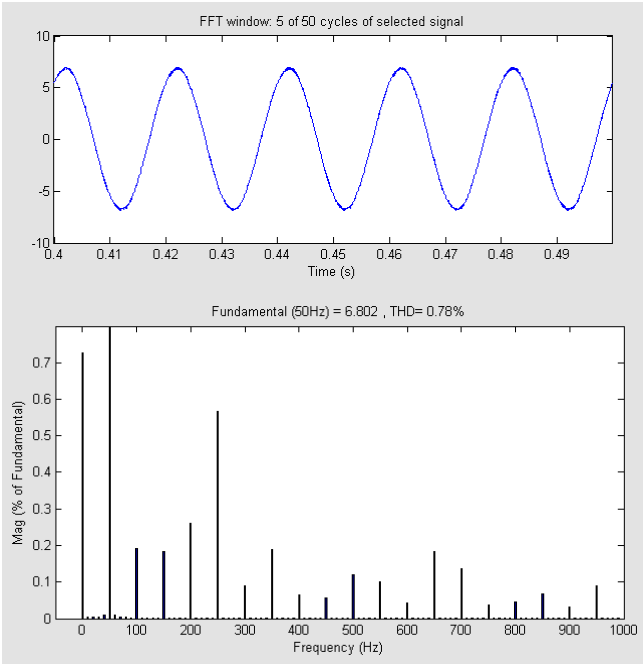

Fig. 12: The stator current I_{as} and its harmonic spectrum of five-level inverter fed induction motor

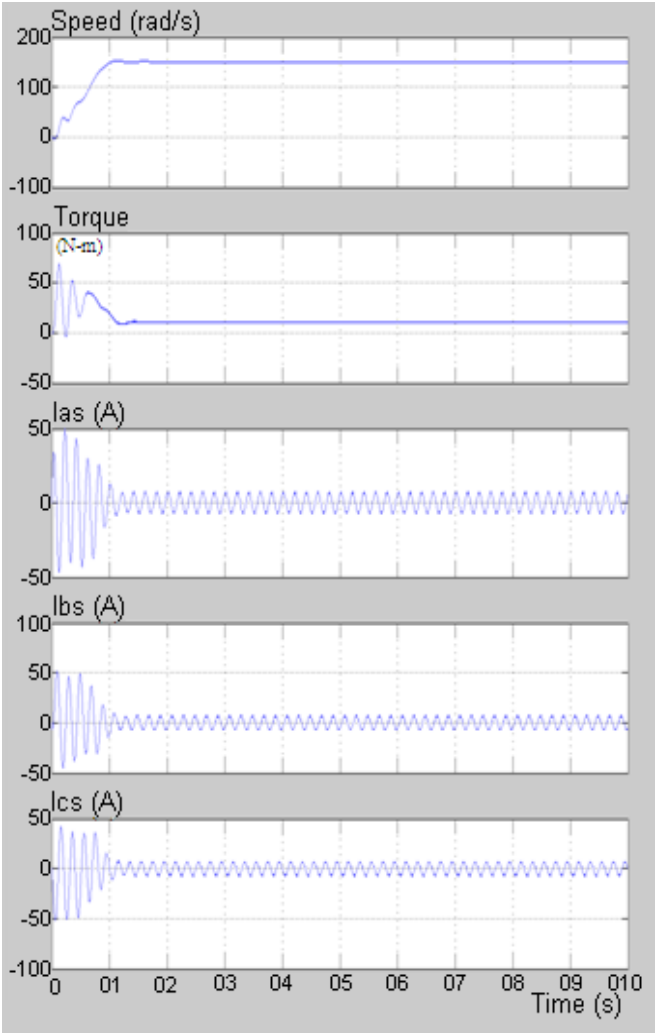

Fig. 13: Speed (N), Torque (T) and line currents Ias, Ibs, Ics of five-level inverter fed induction motor (from top to bottom)

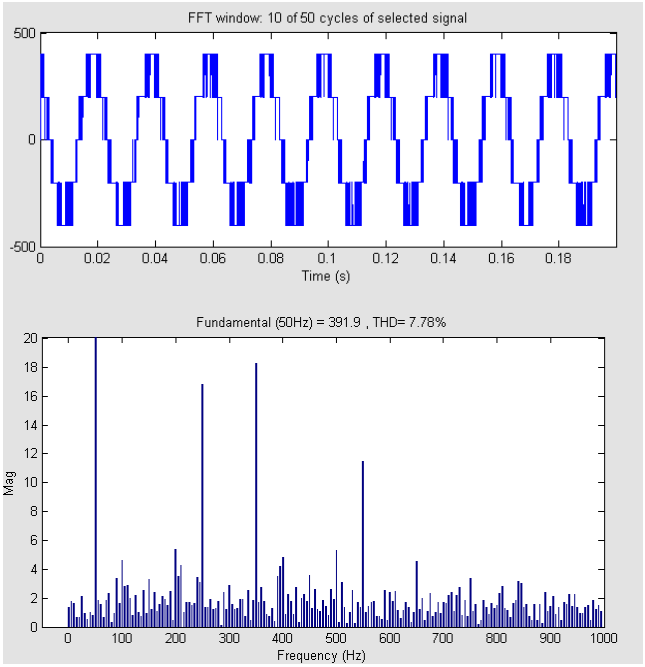

Fig. 14: The line to line voltage (V_{ab}) and its harmonic spectrum of three-level inverter

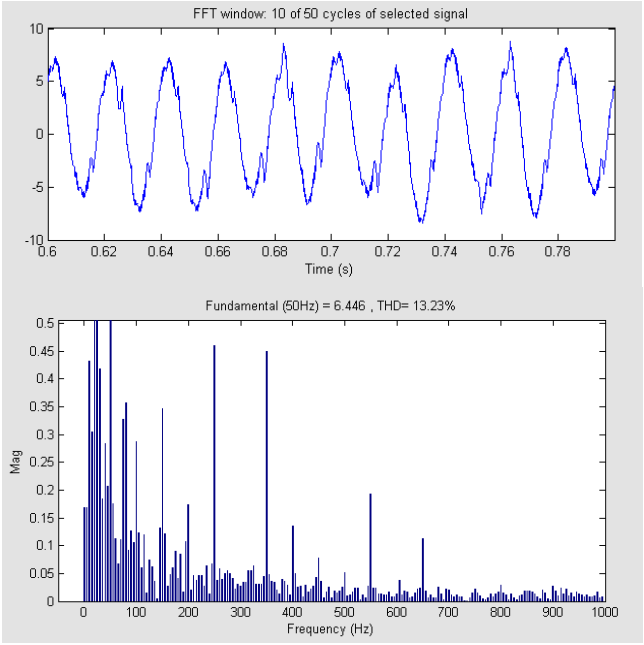

Fig. 15: The stator current I_{as} and its harmonic spectrum of three-level inverter fed induction motor

VI. CONCLUSION

In this paper, a fast space vector pulse width modulation method has been proposed and described for a five-level inverter. In this method, the space vector diagram of the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. After decomposition, all the remaining necessary procedures for the three-level SVPWM are done like conventional two-level inverter. The dwelling times of voltage vectors are calculated at the same manner as two- level inverter.

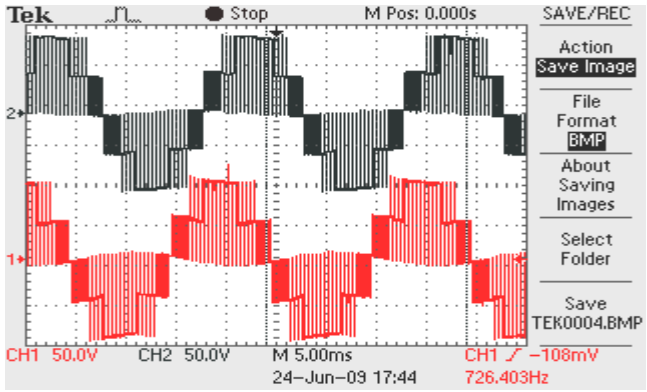

Fig. 15: The output line to line voltages V_{ab} and V_{cb} of three-level inverter

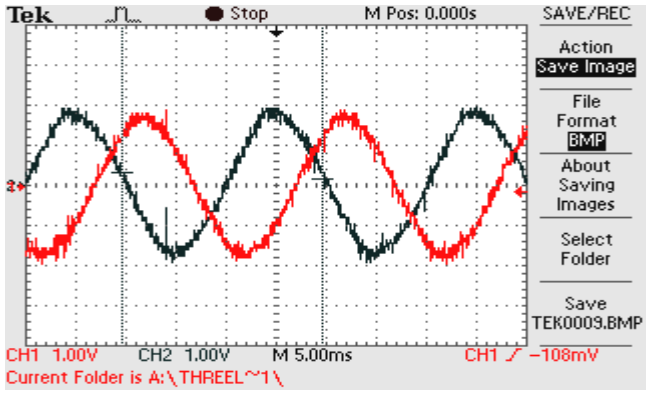

Fig. 16: The load currents I_{ab} and I_{bc} of three-level inverter fed induction motor

Thus the proposed method reduces the algorithm complexity and the execution time. It can be applied to the multi-level inverters above the five-level also. The obtained total harmonic distortion (THD) with the proposed method is only 0.64%, which is very less as compared with the other conventional methods of SVPWM techniques. The waveforms of the simulation and experimental results of three-level diode clamped inverter prove the validity of the proposed method. The results have been good agreement with the published work.

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