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Design Challenges for Distributed Power Systems

Fred C. Lee¹, Ming Xu², Shuo Wang³ and Bing Lu⁴

Abstract – Remarkable progresses have been made over the past decade in power conversion technologies, including advanced power semiconductor devices, power management ICs, innovative circuit topologies, and packaging and integrated system solutions. These technological advancements have been manifested in a wide range of products and applications with ever increasing performances, efficiency, and power density. This paper highlights some of the challenges and opportunities of power conversion technologies in the Distributed Power System (DPS) for computer, telecommunication and network products. Topics techniques to mitigate the detrimental effects of filter/converter parasitics; impacts of the operating frequency of PFC to the size and weight of EMI filter; power conversion architecture and potential simplification; high-frequency high-density AC/DC and DC/DC topologies and designs; bus converters; as well as non-isolated point-of-load converters.

I. INTRODUCTION

Widespread use of the interest and telecommunication requires infrastructure support using a more sophisticated, high-quality and reliable “power network” that naturally takes the form of distribute power generation, distribution and regulation. Such a system is expected to achieve fully controllable, fully reconfigurable, autonomous platforms and customized for ever changing applications. It is envisioned that these advanced systems will be required to provide on demand power from a required source, and required load at any rate and in any desired form. A typical distributed power system (DPS) as shown in Fig. 1, is configured to be scalable and adaptable to ever changing power requirements of computers and telecommunication equipment and systems. The front-end AC/DC converter is a standardized module with the paralleling capability to convert the AC voltage source into the 48V DC voltage bus. This DC bus voltage is often distributed via a back-plane into various circuit boards in a form of plug-in modules, or “circuit packs” in the telephone jargon, with additional point-of-load DC/DC modules locally supplying the need power levels at the appropriate voltages to the end users.

Fig 1: Distributed power system

With ever increasing in functionality and shrinking in size and weight of all forms of computer and telecommunication equipment, it is essential to pack the advanced power hungry processors onto each circuit boards together with the high quality customized and miniaturized power. The aggressive power density targets for AC/DC converters and DC/DC modules, as shown in Fig. 2[1], respectively were met in the past decade and perhaps in the foreseeable future. The typical real estate utilization of the state-of-the-art 3kW 1U telecom AC/DC with 25W/inch³ is shown in Fig. 3. From this picture, it can be easily seen that EMI filter, PFC inductor and bulk capacitors and magnetic in the DC/DC converter represent the major portion of the system.

With rapidly growing computer, telecommunication, and internet technologies and applications, power supplies, other than demanding for higher power density, must achieve higher power conversion efficiency, especially for energy saving.

In the following sections, design challenges and opportunities for EMI filter, front-end AC/DC, board mounted DC/DC will be presented. More distributed power architecture with potential cost saving and performance improvements is proposed. At the meantime, system packaging and integration technologies leading to further improvement of power density and performances are discussed.
II. EMI FILTER DESIGN CONSIDERATIONS AND CHALLENGES

In power electronics applications, electromagnetic (EMI) filter is a necessary interface between the power line and power conversion equipment, such as AC/DC and DC/DC converters operating in high frequency switching mode. They generate conducted switching noise with a spectrum that ranges from the designed switching frequency up to 30MHz. EMI standards, such as EN55022 class A, specify the frequency range (150kHz-30MHz) and noise limits which all power supplies must meet. In order to satisfy these EMI standards, one or two stages of EMI filters are usually employed. A typical one-stage EMI filter used in power supplies is shown in Fig. 4.

Due to the self- and mutual parasitics, the EMI filters do not work as well as expected at high frequencies (HF). Fig. 5(a) compares three DM insertion voltage gain curves, the curve that represents filter with ideal components, the curve that includes components together with their associated self parasitics, and the curve including self parasitics and parasitics due to the coupling of electric field or electromagnetic field referred to as mutual parasitics. It is shown that the self parasitics make DM filter’s HF performance much worse than that of an ideal filter; however, the mutual parasitics finally determines filter’s HF performance. For CM filter performance shown in Fig. 5 (b), the self parasitics, especially the winding capacitance (EPC) of inductors degrades significantly the filter high frequency performances. Investigation [2, 3] shows the mutual coupling (mutual inductance) between inductor and trace loops, between inductor and capacitor, between two capacitors significantly affect differential mode (DM) EMI filter’s high frequency performances. Equivalent series inductance (ESL) of capacitors also plays the role on the filter performances. The equivalent parallel capacitance (EPC), i.e. winding capacitance, of the inductor is a key factor detrimental to CM filter’s high frequency performances [8]. These parasitics must be minimized to improve EMI filter’s ability to attenuate high frequency noises.

The mutual inductance between inductor and trace loops can be easily reduced by reducing the loop areas. One simple method to minimize the coupling between the inductor and capacitors is to rotate the inductor winding by 90° as shown in Fig. 6 [3]. In so doing, the mutual inductance can be reduced by as high as 92% (89.3nH vs. 7.5nH). To reduce the mutual inductance between two capacitors, one simple method is simply to arrange physically the two capacitors to be perpendicular [4]. In this manner, the coupling between the two capacitors can be reduced by 66% as shown in the measurement result. An even better method is to place a 1/3 turn in parallel with one of the capacitor as shown in Fig. 7 [7].

In Fig. 7, the magnetic flux linking C2 also links cancellation turn, so the mutual inductance between two capacitors is cancelled. A 92.3% reduction (439pH vs. 19pH) is achieved in the measurement. The suggested methods illustrated in Fig. 6 and Fig. 7 can be employed at the same time to achieve even better results. Fig. 9 shows the measured insertion voltage gains with these proposed methods and compared them with the original EMI filter without incorporating any suggested methods for improvement.

Fig. 8 shows that the combination of methods suggested in Fig. 6 and Fig. 7 gives best result. A 40dB improvement achieved at 30MHz. It is well known that capacitor behaves like an inductor at high frequencies after the series resonant frequency between the capacitance and the
ESL. For a 0.47μF/400V film capacitor, the measured series resonant frequency is around 2MHz, which means this capacitor behaves like an inductor beyond 2MHz. For an electrolytic capacitor (220μF/250V), the measured series resonant frequency is even below 100kHz. If this electrolytic capacitor is used as a bulk capacitor for a converter with switching frequency above 100kHz, the capacitor actually works like an inductor even for the fundamental component of the switching waveform.

Fig. 7: Integrating cancellation turn with capacitor to cancel mutual inductance between two capacitors

Wang and Lee [9] further proposed a method to cancel the ESL of capacitors so as to significantly improve capacitor filtering performance at high frequencies. The idea is shown in Fig. 9.

Fig. 9: Illustrating the idea of ESL cancellation: (a) network with cancellation inductor and (b) the equivalent network without ESL

Fig. 9 shows that the two networks on the top are equivalent. If two capacitors are diagonally connected and the inductor L is chosen with a value equal to the ESL of the two capacitors, from ESL as shown in the bottom diagram. In the proposed concept, the L can be implemented with the PCB trace inductance. Fig. 10 shows the measured insertion voltage gains with and without ESL cancellation. It shown that after ESL is canceled, the film capacitor performance is improved significantly above 3MHz and a 27dB improvement is achieved at 30MHz when compared with two paralleled capacitors. For electrolytic capacitors, a 27dB improvement at 30MHz also demonstrated and performance improvement above 150 kHz is also noted. The performance improvement for both film and electrolytic capacitors is further verified in [9] by measuring the EMI noise of a converter using a noise separator [6] ad a spectrum analyzer.

Fig. 8: Comparison of filter performance

Fig. 10: Comparison of capacitor performance: (a) film (0.47μF/400V) and (b) electrolytic (220μF/250V)

The method for cancellation of winding capacitance EPC of an inductor was proposed recently [10, 11]. Fig. 11 shows models for DM inductors and CM inductors taking into consideration of EPR and EPC. Fig. 12 shows the ideas of winding capacitance cancellation.

If the two DM inductors are separated, i.e. not on one core, the parasitic model can be shown in Fig. 11(a). If two DM inductors are on one core then there is equivalent parasitic capacitance C_N between two inductors as shown in Fig. 11(b), since the permittivity of the core would be relatively high and the distance between two inductor windings are relatively close. For CM inductor the model is shown in Fig. 11(c).

Fig. 11: Inductor model: (a) separate DM inductor model (b) model for two DM inductors in one core and (c) CM inductor model

In order to cancel the winding capacitance of DM inductors, two extra small capacitors are needed. For separate DM inductors, two small capacitors with values equal to EPC are diagonally connected to two inductors as shown in Fig. 12(a). The cancellation mechanism can be explained by network equivalence as well as mutual capacitance theory developed in [10]. For combined DM inductors, since two windings are on the same core, the effect of C_N can be equivalent to a negative capacitor with
value of $C_N/2$ in parallel with each inductor [10, 11]. If the equivalent negative capacitance is smaller than original EPC, then the total winding capacitance is still positive. Two small capacitors with values of $EPC - C_N/2$ can be diagonally connected to two inductors to cancel it. This is shown in Fig. 12(b). However, if the total winding capacitance is negative, then two small capacitors with values of $C_N/2 - EPC$ should be parallel with two DM inductors. Ironically, in order to cancel the winding capacitance, external capacitors are needed in parallel with windings. This is shown in Fig. 12(c).

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For CM inductors, the method proposed for DM inductors can also be applied if a winding is allowed in ground path. If the winding is not desirable on ground path, the method proposed in [4] can be considered. For the method in [4], the coupling coefficient between two half windings of one side must be as high as 0.9999, which is possible to be realized in an integrated inductor structure. However, for a conventional discrete CM inductor winding structure, the coupling coefficient is around 0.99. Therefore, the idea cannot be applied, since a resonance between the leakage of two winding halves and the cancellation capacitor can cause high frequency noises.

A bifilar winding structure, which is not used in conventional CM inductors due to large EPC, is proposed for high coupling coefficient. Because two winding halves are almost in the same position, the coupling coefficient is very high. The measured value is 0.99995. Although EPC is enlarged, the EPC cancellation techniques can be employed and the performance improved.

In this section, various techniques for cancellation of both mutual parasitics and self-parasitics are introduced. A much better understanding of the basic nature of EMI noises had led to development of in the practice. Continuous research in this area will eventually lead to an understanding and development of this subject matter as a branch of science instead of art or “magic” as it is often referred to.

III. HIGH FREQUENCY HIGH DENSITY FRONT-END AC/DC

For the front-end AC/DC converters, normally they are implemented by two-stage approach. The first stage is the power factor correction (PFC) stage, which is able to provide power factor correction function and a constant voltage for the DC/DC stage input. The second stage is the DC/DC stage, which gives a regulated output voltage for the load. For the PFC stage, the single switch continuous current mode (CCM) PFC is the most widely used topology because of its simplicity and smaller EMI filter. For the whole front-end converter, the EMI noise major comes from the PFC stage. The differential mode and common mode EMI noise models for the single switch CCM PFC circuit have been derived and verified by CPES. Based on the derived the EMI noise model, the switching frequency impact on the EMI filter design of the PFC circuit is analyzed. The switching frequency selection guideline is given based on the analysis.

A. Benefits from High Frequency PFC
Based on the filter attenuation requirement, we are able to develop the relationship between the corner-frequency of the filter and the switching frequencies of the converter, as shown in Fig. 15(a) [13–15]. In these curves, the zigzag nature of the curve is caused by the EMI standard which specifies the regulation requirement beginning at 150kHz.

Fig. 15: Filter corner frequency vs. switching frequency: (a) Differential Mode (b) Common Mode

Those vertical jumps at frequencies representing the various sub-harmonics of 150kHz, such as 50kHz, 75kHz, etc. When the switching frequency is slightly lower than those frequencies, the corner frequency of the DM filter is much higher. Beyond 150kHz, the filter corner frequency will continue to increase as the switching frequency increase. From the curves, it can be seen that when the switching frequency is roughly higher than 400-500 kHz, the corner frequency of the DM filter will be higher than all the previous peaks. As it is know, higher the corner frequency means smaller the EMI filter size. Therefore, one can observer that the size reduction of the DM filter is achieved only if the switching frequency is higher than 400kHz, in comparison with that at 150kHz.

Similar observation can be made for the CM filter. From Fig. 15(b), it can be seen that irrespective to what K value is (where K is related to the circuit parasitic, the switching speed of the MOSFET and the output voltage of the PFC circuit.), when the switching frequency is higher than 400kHz, the size of CM filter will be smaller than that previously achieved at 150kHz. Further increasing of the switching frequency will continue to reduce filter size.

From the previous analysis, we can conclude that the switching frequency has great impacts on the EMI filter design. Since the EMI spec begins at 150kHz, certain frequency range should be avoided. Clearly, there is no filter size reduction achieved when the switching frequency is chosen between 150-400kHz. Since the new generation of power devices, such as CoolMOS and SiC, enable the PFC circuit to operate at a much higher switching frequency. It is possible to contemplating a switching frequency higher than 400kHz. To illustrate this point, two CCM PFC circuits were built, one operated at 100kHz and the other at 400kHz. Two EMI filters were designed, respectively to meet the EMI standard EN55022 Class B. As shown in Fig. 16, both of the converters can meet the standard at the low frequency range. For the two different EMI filter and boost inductor, we can see that 34% and 55% volume reduction is achieved respectively by pushing the switching frequency from 100kHz to 400kHz. The excessive noises at high frequencies are due to parasitics of the EMI filter as discussed in the previous section. The problem can be solved by using the suggested techniques, grounding and shielding technologies.

Fig. 16: EMI noise after filtering and EMI filter size comparison

In Fig. 17(a), the impedances of the boost inductors when designed for 100kHz PFC, there is a resonant valley at the frequency about 17MHz. At this frequency, the impedance of the boost inductor is small. Therefore, the EMI noise at corresponding frequency is high, which can be seen in Fig. 17(b) [15, 16]. But for the 400kHz boost inductor, the resonant valley is pushed beyond 30MHz, as discussed in the previous section; the filter ability to attenuate high frequency noises is compromised with the presence of parasitics. Therefore, it is important to eliminate the high frequency noise peaks. Form the experimental results, we can clear see that the benefit brought by pushing the switching frequency higher.
To get high switching frequency for PFC, CPES has evaluated different devices, CoolMOSTM and SiC diode enable much higher efficiency and higher frequency [17]. A 1kW CCM PFC using CoolMOS TM and SiC diode running at 400 kHz is demonstrated. It shows that by using the CoolMOSTM and SiC diode, the 400kHz CCM PFC can achieve the similar efficiency by using conventional devices at 100kHz switching frequency, as shown in Fig. 18.

![Fig.18: Efficiency comparison between different PFC designs](image)

### B. High frequency DC/Converter

To achieve high power density for the front-end AC/DC converters, increased switching frequency is desired. However, its effectiveness is limited by the large holdup capacitors. For the telecom and computer applications, system is required to maintain a regulated output voltage with full power for 20ms after AC input is lost. Therefore, bulky capacitors are employed to provide the needed energy during holdup time. The size of the selected bulk capacitors will directly impact the input voltage range of the down stream DC/DC converter, thus its conversion efficiency and power rating. To reduce the holdup time capacitors and improve converter power density, it is essential to select an appropriate converter topology that can achieve high efficiency with wide input voltage range, especially high efficiency at 400V input [18–20].

For conventional PWM DC/DC converters, a maximum duty cycle is designed for the minimum input (say, 300V) which occurs when the AC input power is lost. Consequently, the given circuit will operate at a smaller duty cycle when the input voltage is at around 400V. Thus, to realize a wide input range, it is inevitable that the converter efficiency is suffered at the nominal input of 400V. Fig. 19 demonstrates the efficiency of an asymmetrical half-bridge (AHB) optimally designed for a fixed input voltage at 400V. The circuit can achieve 94.5% efficiency. When the same circuit is designed to operate at 300V to 400V input range, the converter efficiency can only achieve 92% at 400V [20].

![Fig.19: Efficiency of AHB and LLC converters](image)

Instead of using PWM converters, certain class of resonant converters such as the LLC resonant converter as shown in Fig. 20(a) is able to operate with a wide input range without compromising circuit efficiency at the desired operating voltage, i.e. at 400V. Because the magnetizing inductor participates in resonant, converter voltage gain characteristic is change, as shown in Fig. 20(b).

![Fig.20: LLC resonant converter (a) Circuit topology (b) Voltage gain](image)

The LLC converter can achieve a voltage conversion ratio either higher or lower than unity. Moreover, the zero voltage switching (ZVS) can be achieved with switching frequency both lower and higher than the series resonant frequency determined by $L_r$ and $C_r$. By choosing a suitable transformer turns-ratio, the converter can be targeted to operate right on top of the resonant frequency with optimal efficiency at normal operation condition, i.e. 400V input. During holdup time, input voltage drops, and LLC resonant converter reduces its switching frequency and increase voltage gain to maintain regulated output voltage. Although LLC converter operates far away from the resonant point during the holdup time which means the circuit is less efficient, it only lasts for 20ms and will not cause extra thermal problem. Because LLC converter can operate at resonant frequency during normal operation condition, the circuit is operated at the most efficient point and its efficiency could be much higher in comparison with AHB or other PWM topologies. As shown in Fig. 19, with 200kHz switching, LLC could achieve 2 to 3% efficiency improvement over that of AHB. Moreover, LLC resonant is operated with ZVS turn-on and relatively small turn-off current. These properties make switching losses at the primary side switches very small. Besides, the secondary side diodes are also operated with ZCS thus reduces the diode reverse recovery loss. The much reduced switching losses enable LLC resonant converter to operate at much higher switching frequencies while maintaining high efficiency. A proto-type 1MHz LLC was developed with 94.5% efficiency at 1kW output. The
efficiency of LLC resonant converter for different switching frequency is shown in Fig. 21. As shown in Fig. 22(b), 1MHz LLC achieves 76W/in³ power density [20, 22].

![Fig. 21: Efficiencies for LLC converter with different switching frequency](image1)

**C. High density front-end AC/DC via IPEMs**

Although higher density is achieved at higher frequency, some fundamental limitations prevent further improvement in power density. For example, the parasitic inductance in the switch commutation loop hampers the switching speed and causes more switching losses. Large voltage stresses appear on switching devices due to large parasitic inductance, which compromises reliability. The parasitic junction capacitances between high voltage transition points to the earth ground increases the common mode noise. Moreover, the parasitic components brought by the interconnection of the electrical layout played a negative role in the system electromagnetic interference noise (EMI) if it is not treated carefully.

The front-end AC/DC converters are essentially custom designed and manufactured using discrete parts, which has high labor content and high cost. To address the aforementioned performance issues and cost, the integrated power electronics module (IPEM) concept was proposed by Center of Power Electronics Systems (CPES). The IPEM concept is to explore the integration of discrete power devices to the extend that it is technologically practical and economically feasible. To this end, the active power semiconductor devices, with its associated drivers, protection circuits, sensors and controller are integrated together in the form of modular building block here referred to as active IPEM. Similarly, the passive power components such as inductors, capacitors and power transformers are integrated together into a Passive IPEM. One apparent benefit of integration is the size reduction. The integration of the switching devices together with their associated gate driver circuit, invariably will reduce parasitics associated with interconnects, thus resulting in smaller switching losses and voltage stresses. By integrating inductors, capacitors, together with power transformer, passive component size can be greatly reduced. Moreover, due to the integration, circuit component number can be greatly reduced. The assembly of such modules could be automated thus reduce labor content. Furthermore, by perfecting the process of integration, IPEMs can become standard building blocks to facilitate system integration. Therefore, the reliability, product cycle time and cost can be significantly reduced [23, 24].

To demonstrate the benefits of the IPEM concept under the system topology, two 1kW front-end AC/DC converters were built using exactly the same topologies, one using discrete devices and the other one using IPEMs. As shown in Fig. 1 and 23, the system is constructed by the two stages: PFC stage and DC/DC stage. For the PFC stage, a 400kHz single switch PFC using CoolMOS and SiC diode were chosen to reduce the boost inductor and EMI filter. The Asymmetrical Half Bridge operating at 200kHz was used for the DC/DC stage. The converters are designed for the universal input line 90V～264V, and the power rating is de-rated to 600W when operated below 150V input. Two converters are shown in Fig. 23.

![Fig. 22: Comparison among different DC/DC converter designs:](image2)

(a) 200 kHz AHB, 12W/in³ (b) 1MHz LLC, 76W/in³

By replacing the discrete active and passive devices into the IPEMs, the number of components of the systems can be reduced from several hundreds part to about 20-30 parts. Not only the system power density has been improved, the system electrical performance has been improved as well. The system efficiency increases more than 2% at the high line voltage range, and more than 3% at 90V. Since the conduction losses are roughly the same for the same operation condition, the major improvement lies on the switching loss reduction by minimizing the circuit parasitics.

At the same time, due to the smaller parasitic inductance on critical path of the converter, less voltage stress is achieved. For the discrete PFC switch, when switch turn off occurs at 7Amp, the device voltage overshoot is 123V. But when the discrete components are replaced with an active IPEM, the voltage over-shoot is reduced to 72V even at 10Amp.
IV. HIGH FREQUENCY HIGH CURRENT DENSITY BOARDMOUNTED ISOLATED DC/DC CONVERTERS

With rapidly growing computer and telecommunication applications, the point-of-load (POL) DC/DC module is becoming smaller and smaller, from non-isolated POL to isolated 1/4 brick to 1/8 brick and even to 1/16 brick, and in the mean time, with continuous increasing in current demand and decreasing in output voltage. High power density and high efficiency are demanded by the customers Design engineers, now a day are facing challenges in all fronts, including higher operating frequencies with reduced switching losses, conduction losses, body diode losses and even the gate driver losses; innovative packaging and thermal management; EMI and EMC containment and reduction.

This section will introduce two examples of circuit means of achieving higher operating frequencies and in the same time, higher efficiencies. These goals are realized by simultaneously reducing the primary side switching losses and conduction losses as well as the secondary side synchronous rectifier body diode conduction losses, reverse recovery losses, drive losses, and conduction losses.

A. Single Stage isolated DC/DC:

A.1 State-of-the-art:

Fig. 24(a) shows a typical PWM hard-switching 48V input DC/DC topology. To get faster dynamic performance and higher power density, higher switching frequency is desired. However, as shown in Fig. 24(c), efficiency will suffer a lot at higher switching frequency mainly due to the switching loss, driving loss and SR body diode conduction loss. By far, the soft switching technique is a well-known approach to reduce the switching loss effectively. Therefore, Fig. 24(b) shows the state-of-the-art 48V DC/DC for server processor (power pod), running at 300 KHz by employing phase-shift full bridge ZVS topology. Its efficiency can be seen in Figure 30(b).

A.2 Self-Driven ZVS Full-Bridge DC/DC and Magnetic Integration:

The self-driven technique has been widely used in the industry practice due to their simplicity and low cost. However, for bridge-type symmetrical converters, implementation of self-driven capability is difficult because of the inherent dead time period. One possible solution is the level-shifted self-driven concept [25]. However, the proposed approach has several drawbacks: (a) Ringing occurs at the gate signal because the signal is coming from the main power transformer and severe ringing is coupled from the power stage, (b) there is extra body diode conduction loss, and (c) there is large amount of conduction loss due to the low driving voltage during dead time. These issues prevent the level-shifted self-driven concept from being used in high frequency applications.

In order to overcome these issues, a self-driven ZVS full bridge (FB) was proposed [26, 27]. The power stage is shown in Fig. 25. By simply rearranging the control strategy, it becomes very suitable for self-driven capability as well as achieving ZVS. It was further demonstrated that the self-driven scheme can save driving loss and body diode conduction loss and is very suitable for high-frequency applications where high power density is required.

In the conventional synchronous rectifier, the dead time is necessary, accompanying with the body diode conduction loss and reverse recovery loss due to the current through the body diode during the dead time. There are some precise timing control driving ICs to reduce the body diode conduction loss. However, they cannot effectively solve the body diode reverse recovery problem. And also, they are expensive and noise sensitive.

A 1MHz prototype picture shown in Fig. 26(a) was built to verify this self-driven concept. Fig. 26(b) shows the efficiency comparison. Including the driver loss, the proposed self-driven ZVS full-bridge can achieve 81.7% efficiency.

There is an efficiency improvement of 4.7% as compared with the conventional phase-shifted full-bridge with an external driver.
However, this topology requires a total of 3 discrete transformers, one main power transformer and two synchronous rectifier gate drive transformers, thus increasing the number of passive components. Further work has been done to integrate all of the three magnetic components and two output inductors into a single core as shown in Fig. 27 [28]. This fully integrated magnetic has been adopted in a 1.2V/70A 1/8 brick prototype with 87% overall efficiency at 600kHz switching frequency. Comparing to the state-of-the-art 1/8 brick product, it can deliver 40% more output current while having 2% higher efficiency.

![Fig. 27: 600 kHz 1.2V/70A 1/8 brick hardware and measured efficiency](image)

Generally, the gate driving loss can be reduced by the combination of the ZVS technique and Self-driven technique. As an example, the proposed self-driven ZVS full-bridge has the following advantages: (a) soft switching for primary switches; (b) clean gate signal and no level-shifting during dead time; (c) reduced gate driving loss; and (d) reduced body diode conduction loss. The experimental results verify that this topology is very promising in high-frequency applications. Furthermore, the proposed self-driven method can be applied to any bridge and non-bridge topologies employing complementary control.

A.3. Current Tripler Concept and Magnetic Integration

For low-voltage and high-current applications, the secondary-side device switching and conduction losses have a major impact on system efficiency. To reduce the conduction loss in the secondary side, one solution is to reduce the on resistances of the synchronous rectifiers and the transformer winding resistance. This can be realized by paralleling more synchronous rectifier switches (SRs) and enlarging the window area of the transformer. The drawbacks of this solution are the higher cost, larger gate driver loss and larger footprint.

Other than reducing the Rds (on) of the synchronous rectifier, proper secondary-side topologies should be selected to reduce the RMS current through the SRs. There are three major secondary-side topologies: forward rectifier, center tapped rectifier and current-doubler rectifier. Among these three topologies, the current-doubler rectifier is the most suitable for high-current, low-voltage applications. Because of its simpler transformer structure and halved inductor currents and transformer secondary currents, the current-doubler topology offers lower conduction losses than the conventional center tapped topology [29].

The reason for the lower RMS current of the current-doubler rectifier is that during the freewheeling period (when there is no input-output energy transfer), both SR switches can conduct simultaneously to share the load current. As a result, the total rectifier conduction loss during the freewheeling period is reduced. To further reducing the conduction losses for higher current applications, often times, current-doubler with more semiconductor devices in parallel and distributed magnetics are used to reduce the transformer winding losses. However, those solutions have their limitations:

- a) Increased cost,
- b) Larger footprint and lower power density,
- c) More devices mean greater driver loss.

Recently, a novel current-Tripler topology was proposed, as shown in Fig. 28. The proposed topology can easily achieve ZVS for all MOSFETs, therefore switching loss is significantly reduced [30]. Through magnetic integration shown in Fig. 29, a three phase high frequency transformer can be used to greatly simplify the circuit.

Compared with the conventional current doubler, the proposed current Tripler can reduce the SR conduction loss and transformer winding loss by 20% and 12.5% respectively.

A 300kHz prototype was developed to demonstrate the concept. Comparing to the typical industry design with the same spec and switching frequency, proposed current-Tripler DC/DC converter can achieve 45% footprint reduction and 4% higher efficiency, as shown in Fig. 30.

![Fig. 28: Proposed Zero-Voltage-Switch current-Tripler DC/DC converter](image)

![Fig. 29: Implementation by three discrete cores](image)

![Fig. 30: (a) 300 kHz hardware of the proposed ZVS current tripler, (b) Efficiency comparison with state-of-the-art](image)

B. Two-Stage isolated DC/DC

The 48V input DC/DC for high-end server and telecom applications requires higher voltage devices on the primary side and a transformer for isolation. To get fast dynamic response and regulation performance, the PWM type power conversion is preferred, whereas the efficiency and switching frequency is limited by the presence of the leakage inductances of the transformer. In order to achieve acceptable efficiency, lower switching frequencies,
around 200–300 KHz, are normally adopted. Thus the size of the transformer and its passive components are bulky and the transient responses are slow. Excessive output capacitors are necessary to satisfy the dynamic transient requirement. In general, the isolated 48V DC/DC is normally customized design with higher cost, while its footprint and power density are significantly lower than that of the non-isolated POL converters.

To leverage the 48V isolated DC/DC with standard high frequency non-isolated POL converter techniques, a superior two-stage approach was proposed [31], as shown in Fig. 31. The first stage utilizes a simple inductorless “DC/DC transformer operating at 1MHz switching frequency by adopting the resonant switching to minimize switching losses. The second stage employs the multiphase buck capable of operating at multi-Mega Hertz, taking advantage of the already established infrastructure for low-voltage POL converters. Fig. 32 shows the two-stage prototype for the 48V power pod used in the server. Due to the MHz switching frequency in the second stage, the passive components can be greatly reduced. Table I lists the comparison between the CPES two-stage prototype and the industry single stage practice in Fig. 24(b). Based on the reduction of passive components, the power density of the power pod can be increased to around 150%. It is also apparent that since the output capacitors are significantly reduced, the two-stage approach is less costly than the single-stage approach. This architecture has been quickly adopted by the industry and used in the current products.

C. Intermediate Bus Architecture (IBA) and Bus Converter

With the proliferation of low-voltage, high-current microprocessors/DSPs and high-voltage analog devices on a single circuit board, the number of different voltages encountered has mushroomed. All these voltages share a common ground so that it is unnecessary to use an isolated transformer for each of these loads, respectively.

Therefore, the two-stage concept aforementioned was extended to the sub-system level, as shown in Fig. 33, in which an isolated bus converter steps down the 48V to an intermediate bus voltage to feed all the non-isolated point-of-load converters (POL) in the same board. This concept has been adopted by industry and is becoming a mainstream for high-end server and telecommunication applications, because it is more cost-effective, more flexible in terms of system structure. To minimize the size and cost of these bus converters, CPES proposed inductorless bus converter family with ZVZCS switching behavior through the resonant between the transformer leakage inductor and output capacitor [32]. These proposed topologies can double the power capability compared with state-of-the-art products. As an example, Fig. 34(a) shows the full-bridge version of the proposed inductorless bus converter family. Fig. 34(b) and (c) shows the 800 kHz 500W bus converter prototype with 96% efficiency at full load.

Table 1: The Comparison between Single-stage and two-stage

<table>
<thead>
<tr>
<th>Switching frequency</th>
<th>Transformer</th>
<th>Inductor</th>
<th>Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Industry Practice</td>
<td>Philips EI32</td>
<td>2 Philips EI22</td>
<td>15*1mF Tantalum</td>
</tr>
<tr>
<td></td>
<td>(customized)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPES</td>
<td>Philips EI22</td>
<td>4 Vishay IHLP-5050FD</td>
<td>4*270uF ESRE</td>
</tr>
<tr>
<td>Prototype 1st stage: 300kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2nd stage: 1MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Volume Reduction</td>
<td>54%</td>
<td>90%</td>
<td>75%</td>
</tr>
</tbody>
</table>

Fig. 31: Proposed two-stage solution

Fig. 32: 130W two-stage power pod prototype for server

Fig. 33: Two-stage architecture—IBA

Fig. 34: Proposed inductor-less resonant FB DC/DC transformer
V. HIGH FREQUENCY HIGH CURRENT DENSITY NON-ISOLATED POINT-OF-LOAD (POL) CONVERTERS -- VRS

In 1997, CPES proposed a multi-phase buck converter, as shown in Fig. 35, for the INTEL Pentium processor. This concept was quickly adopted by the industry. The VR is designed to operate at around 300kHz and the control bandwidth is around 50kHz. It is well known that the switching frequency can be increased to reduce the output capacitance. However, the efficiency of today’s single stage suffers at higher switching frequencies. As shown in Fig. 36, the major loss factors are the switching losses and the body diode losses.

![Fig. 35: State-of-the-art VR solution: Multi-phase Buck](image)

![Fig. 36: Issues of single stage 12V VR at higher switching frequency, (a) Efficiencies, (b) Loss breakdown comparison](image)

A. 1MHz ZVS Self-Driven Single-stage VRs

From the loss breakdown in Fig. 36, the major factors affecting circuit efficiency at 1MHz are switching loss, body diode losses and gate driving loss.

![Fig. 37: Proposed ZVS self-driven full bridge Buck](image)

To minimize the aforementioned high frequency losses, a novel self-driven dc/dc converter for non-isolated 12-V VR was proposed, as shown in Fig. 37 [33]. ZVS was realized for all the MOSFETs. By adding a transformer, the proposed topology extends its duty cycle so that both the switching loss and body diode reverse recovery loss are further reduced. This innovative self-driven concept eliminates the need for synchronous rectifier drivers which saves cost and driver loss. In addition, self-driven scheme reduces the body diode conduction losses. Furthermore, the magnetic integration has been realized to merge the output inductor into the transformer to further reduced the size. All of these benefits have been demonstrated in a 1MHz 100A 1U 12V VRM prototype shown in Fig. 38(a). Compared to the conventional Buck design, the proposed topology can elevate the efficiency by 6% at 1MHz switching frequency with the same active component setup, as shown in Fig. 38(b).

![Fig. 38: Demonstration of the proposed DC/DC in 1U 100A 12V VRM (a) Hardware, (b) Efficiency comparison](image)

Thought the proposed self-driven topology is compelling, the duty cycle loss induced by the transformer leakage inductor is one inherent limitation for higher than 1 MHz operation. Theoretical analysis reveals that the gain of this topology is diminishing with switching frequency increasing beyond 1MHz.

![Fig. 39: The structure of the two-stage approach in [34]](image)

Thereby, a two-stage approach shown in Fig. 39 is proposed in [34]. The first stage can be designed at relatively low switching frequency to step down the input voltage from 12V to around 5V. With the lower input voltage, the switching losses and reverse recovery losses of the second stage, which are proportional to the input voltage, are dramatically reduced. Therefore, it was demonstrated that the second stage switching frequency can be pushed to 2MHz to achieve 350kHz bandwidth at 83% efficiency [34, 35]. The prototype in Fig. 40 clearly shows that the two-stage approach can eliminate the output electrolytic capacitor entirely together with a 2% efficiency improvement over the single stage solution. This is achieved with a switching frequency is 4 times higher than the single stage counterpart.

![Fig. 40: Demonstration of the two-stage 12V VR (a) Hardware, (b) efficiency comparison](image)
The conventional Buck converter was employed for the first stage initially, as shown in Fig. 39. It was designed to run at low switching frequency, e.g. 200-300 kHz, to attain high efficiency. However, this low switching frequency makes the first stage relatively large in size. Subsequently, a magneticless DC/DC converter was developed by adopting the switching capacitor technology [36]. Because no magnetic component is required, it can substantially boost the power density of the first stage up to 1kW/inch³. The proposed first stage with fixed 2:1 conversion ratio is essentially serves as a voltage divider. It can achieve 98% efficiency with 12V or even higher input voltage. Fig. 41 shows the comparison between the buck and voltage divider designs for the first stage.

Other than high power density, the proposed voltage divider can achieve ultra-high efficiency in the whole load range with capability to handle over load conditions. By adapting the switching frequency to the load, 98~99% efficiency in whole load range has been demonstrated in a 70W prototype design as shown in Fig. 42. Even with 100% overload, the circuit can maintain 95.5% efficiency.

VI. CONCLUSION

This paper provides an overview of some of the important design challenges and opportunities for power supplies, specifically using the example of a generic distributed power system for computer server, telecom and network applications. First, the effects of mutual and self-parasitics of the filter capacitors and inductors on the performance of EMI filter are presented. Techniques for cancellation of both mutual parasitics and self-parasitics are introduced. Specifically, mutual coupling between inductors and capacitors as well as coupling between two capacitors can be minimized.

Among the self-parasitics, the ESL of capacitors and the winding capacitance of the filter inductors are identified most detrimental to both DM and CM noises. The unwanted effects of self-parasitic can be neutralized by circuit means. The proposed technologies are proven by theory and verified by experiments. It is demonstrated that, EMI filter’s HF performance can be greatly improved by applying proposed methods in practice.

To achieve higher power density of front-end converter, it is essential to using high switching frequency techniques to reduce passive component size. In the PFC stage, it is found that the impact of switching frequency to EMI filter size reduction is realized when the switching frequency is pushed beyond 400 kHz. The switching frequency between 150kHz to 400kHz should be avoid since the EMI filter size could be even larger than that at 70kHz due to the EMI regulation that specifies noise level from 150 kHz to 30MHz.

Besides the reduction on EMI filter and PFC inductor, it is
essential to reduce the size of bulk capacitor for hold up time requirement. It is found that the LLC resonant converter offer special advantage for this application. It can work with wide input range without sacrificing the conversion efficiency at the normal operation condition. Furthermore, smaller switching loss allows LLC converter to operate at considerably higher switching frequency while maintaining high efficiency. A prototype LLC converter operated at 1 MHz was demonstrated with 76W/in³ power density.

System power density was further improved by means of integration using IPEM concept. Modular and integrated approach makes the system layout easy and manufacturing process more automated. Furthermore, it was shown that circuit interconnect parasitics were significantly reduced, thus further improving converter efficiency and reducing components stresses.

Products in the area of isolated and non-isolated point-of-load converters are fiercely competitive. The major driving forces are cost, efficiency and power density. Design challenges for high-frequency, high-density POLs involve innovative circuit means of reducing the primary side switching losses and conduction losses as well as the secondary side synchronous rectifier body diode conduction losses, reverse recovery losses, drive losses, and conduction losses. Packaging and thermal management are equally important. Some of the important recent developments are presented. A novel zero-voltage switching (ZVS) current-Tripler converter was presented which offers great advantages compared with the popular current double configuration especially for low voltage and high current applications. A novel self-driven ZVS full bridge topology was introduced with significant saving of driver losses, switching losses, and body diode losses for isolated and non-isolated DC/DC converters. One of the potential applications is for powering the next generation of microprocessors. Prototype hardware is demonstrated operating at 1MHz 12V with an efficiency 6% above the comparable multi-phase Buck topology used in today’s VRM design. Other than the topological innovations, CPES also proposed two-stage power architectures to further improve the system performance for isolated and non-isolated applications. Prototypes were developed to demonstrate significant improvements in efficiency, power density as well as potential cost saving compared to the state-of-the-art.

REFERENCES


Modelling and Teaching of Magnetic Circuits

Yim-Shu Lee\(^1\) and Martin H.L. Chow\(^2\)

Abstract – In the analysis of magnetic circuits, reluctances are commonly modeled as resistances and magnetomotive forces modeled as electromotive forces. In this way the magnetic flux and flux density can be determined easily. However, a close examination should reveal that it is fundamentally wrong to use a resistance, which is a lossy component, to model reluctance, which is a lossless component. This confusion may result in serious problems in the analysis and computer simulation of mixed electric and magnetic circuits. The gyrator approach of modeling can resolve the problem. However, due to the unwillingness of electrical engineers to accept the term gyrator, it has never been widely used. In this paper we propose to revitalize the gyrator model and to further develop it into a z-parameter model. Since z-parameters are well-defined parameters of the 2-port networks, engineers/students in the electrical engineering discipline should find the z-parameter model much easier to understand and to manipulate. In addition, we also propose some strategies to introduce the z-parameter model of magnetic circuits into the curriculum of electrical engineering courses.

Keywords - Power converter, resonant converter, motor drives, vector control

I. INTRODUCTION

In the analysis of magnetic circuits, often reluctances are modeled as resistances and the magnetomotive forces modeled as electromotive forces. While this approach of modeling has been well accepted and widely used by practicing engineers, the concept of modeling reluctance, which is a reactive component, by resistance, which is a lossy component, is fundamentally wrong. This problem becomes very serious when computer simulations are involved. Consider the example of a theoretically lossless inductor. If the reluctance of the magnetic core is modeled as a resistance in a computer program, unexpected (false) loss will appear in simulations involving energy and power.

In 1948, Tellegen proposed the concept of gyrator [1] as a circuit element. This concept was applied to the modeling of magnetic components to solve the problem mentioned above by Buntenbach [2], [3], [4], Hamill [5], [6] and Eaton [7], [8]. However, due to the unwillingness of electrical engineers to accept the term gyrator; this approach of modeling has never been widely used.

The objective of this paper is to revitalize the gyrator concept of modeling magnetic circuits and to further develop it into a form that is readily acceptable to electrical engineers and students, and appropriately simulated by computers. More exactly, we propose to use a z-parameter two-port network to model the behavior of the interface between an electric circuit and a magnetic circuit [11]. It is assumed that the topic of z parameters is well covered in electrical engineering courses.

It is found that the z-parameter model is particularly useful for the simulation and analysis of integrated magnetics, which are now popularly used in modern power electronics, e.g., polyphase voltage regulator modules for high-speed CPUs. In Section II of this paper, the logic and methodology of using a z-parameter two-port network to model the interface between an electric circuit and a magnetic circuit will be described. In Section III, some examples of the application of the z-parameter model will be given. In Section IV, the duality relationship between the z-parameter model and the equivalent-circuit model of magnetic components will be examined. In Section V, some suggestions on the teaching of magnetic circuits to electrical engineering students will be given.

II. USE OF Z-PARAMETER TWO-PORT NETWORK TO MODEL THE INTERFACE BETWEEN AN ELECTRIC CIRCUIT AND A MAGNETIC CIRCUIT

To start with, let us consider the electrical parameters of a simple capacitor and the magnetic parameters of a simple inductor, as shown in Fig. 1.

For the capacitor shown in Fig. 1(a), we have

\[ EA = \frac{Q}{\varepsilon_0 \varepsilon_r} \]  

where \( E \) is the electric field strength between the parallel metal plates of the capacitor, \( A \) is the area of the metal plates, \( Q \) is the charge on the capacitor, \( \varepsilon_0 \) is the absolute permittivity of space, and \( \varepsilon_r \) is the relative permittivity of the dielectric material between the metal plates of the capacitor. For the inductor shown in Fig. 1(b), we have

\[ HA = \frac{\phi}{\mu_0 \mu_r} \]  

where \( H \) is the magnetic field strength in the magnetic core, \( A \) is the cross sectional area of the magnetic core, \( \phi \) is the total magnetic flux, \( \mu_0 \) is the absolute permeability of space, and \( \mu_r \) is the relative permeability of the core material.
Comparing (1) and (2), it appears natural that for simulation purposes the magnetic field strength $H$ could be modeled as the electric field strength $E$ and the magnetic flux $\Phi$ could be modeled as the electric charge $Q$. Based on this assumption, we can find the duality relationship between electric and magnetic parameters as shown in Table 1.

### Table 1: The duality relationship between electrical and magnetic parameters

<table>
<thead>
<tr>
<th>Magnetic Parameters</th>
<th>Electrical Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetic field strength $H$</td>
<td>Electric field strength $E$</td>
</tr>
<tr>
<td>Magnetomotive force $\text{mmf}$</td>
<td>Charge $Q$</td>
</tr>
<tr>
<td>The rate of change of magnetic flux $\frac{d\Phi}{dt}$</td>
<td>The rate of change of charge $\frac{dQ}{dt}$ or current $i$</td>
</tr>
</tbody>
</table>

Now let us consider the electric/magnetic interface shown in Fig. 2(a). Assume that a two-port network with $z$-parameters, as shown in Fig. 2(b), is used to model the interface. Port 1 is to model the electric part of the interface and Port 2 is to model the magnetic part. The current $i_2$ in Port 2 is to model the $\frac{d\Phi}{dt}$ of the magnetic core.

\[ i_2 = \frac{d\Phi}{dt} \]  

(3)

The negative sign in (3) is due to the opposite directions of $\frac{d\Phi}{dt}$ and $i_2$ as defined in Fig. 2. The dependent voltage source $Z_{12}i_2$ is used to model the back $\text{emf}$.

\[ Z_{12}i_2 = \frac{d\Phi}{dt} \]  

(4)

Comparing (4) with (3), it is found that

\[ Z_{12} = -N[\text{Ohms}] \]  

(5)

Note that numerically $Z_{12}$ is equal to $N$. But the unit of $Z_{12}$ is Ohms.

The parameter $Z_{11}$ can now be determined by assuming $\frac{d\Phi}{dt} = 0$, or $i_2 = 0$. Under this condition, we have from Fig. 2(b)

\[ Z_{11} = 0 \]

\[ Z_{11} = V_1 = R \]  

(6)

where $R$ is actually the series resistance of the winding. The dependent voltage source $Z_{21}i_1$ is used to model the $\text{mmf}$. Hence

\[ Z_{21}i_1 = Ni \]  

(7)

Therefore we can find $Z_{21}$ from (7)

\[ Z_{21} = N[\text{Ohms}] \]  

(8)

In order to determine $Z_{22}$, we assume that a current $i_1$ is forced into Port 1, and Port 2 is terminated by a magnetic short circuit (magnetic material with zero reluctance) as shown in Fig. 3(a). The $\frac{d\Phi}{dt}$ in the magnetic circuit can then be found as

\[ \frac{d\Phi}{dt} = \frac{\text{d}(\text{mmf})}{dt} \frac{1}{S} \]  

where $S$ is the reluctance of the magnetic core. If the magnetic core has a magnetic path length of $l$, the reluctance of the magnetic core $S = \frac{l}{\mu_A l}$. The behavior of Port 2 can be modelled by the electric circuit shown in Fig. 3(b) where

\[ i = \frac{dC}{dt} \]  

(10)

A term-by-term comparison between (9) and (10) shows the following duality relationship:

\[ i = \frac{d\Phi}{dt} \]  

(11)
Based on (5), (6), (8) and the Port 2 model shown in Fig. 3(b), we can derive a complete z-parameter two-port network model of the interface as shown in Fig. 4.

Using the interface model shown in Fig. 4, the z-parameter models of magnetic components can be derived easily. Fig. 5 shows an example of an inductor, where $R$ is the resistance of the windings, $S$ is the reluctance of the magnetic core, and $C$ is a capacitance modelling the behavior of the magnetic core. Fig. 6 shows an example of a transformer, where $R_p$ and $R_s$ are the primary and secondary winding resistances respectively. It should be noted that the z-parameter model closely resembles the physical structure of the magnetic circuit. This makes the modelling of complex integrated magnetics much easier.

### III. Examples of Application of Z-Parameter Model in Integrated Magnetics

In modern power electronics, integrated magnetics could provide a means to achieve demanding requirements in various applications, e.g., polyphase power converters for high-speed CPUs. The proposed z-parameter model is particularly useful for the analysis of integrated magnetics. Three examples of integrated magnetics and their z-parameter models will be studied in this section.

#### A. Integrated Inductor/Inductor

Fig. 7(a) shows a possible winding arrangement of an integrated magnetics consisting of two inductors. Inductor $a$, formed by windings $N_{a1}$ and $N_{a2}$, is wound on the outer limbs of the magnetic core. Inductor $b$, formed by winding $N_b$, is wound on the center limb of the magnetic core. By modelling each electric/magnetic interface as a z-parameter two-port network, a z-parameter model of the integrated magnetics can be found, as shown in Fig. 7(b). Note that for the sake of simplicity, the winding resistances of the inductor windings are assumed to be negligible so that the $Z_{11}$ in the z-parameter model can be neglected. Starting from here, the same assumption will be made in the rest of this paper.

A simple analysis on the circuit shown in Fig. 7(b) will show that if $C_1 N_{a1} = C_2 N_{a2}$, the capacitances $C_1$, $C_2$, and voltage sources, $N_{a1} i_a$, $N_{a2} i_a$, will form a balanced bridge. We shall then have $i_1 = i_2$. Under this condition $i_3$ will be unaffected by $i_a$. What this means physically is that the current in Inductor $a$ will produce zero magnetic flux in the center limb of the magnetic core. Thus the operation of Inductor $b$ will not be affected by the current in Inductor $a$. Under the same condition of $C_1 N_{a1} = C_2 N_{a2}$, the current in Inductor $b$ will produce equal but opposite voltages on the two windings of Inductor $a$. This results in a zero net voltage across Inductor $a$, meaning that the current in Inductor $b$ will also not interfere the operation of Inductor $a$.

#### B. Integrated Inductor/Transformer

A simple analysis on the circuit shown in Fig. 7(b) will show that if $C_1 N_{a1} = C_2 N_{a2}$, the capacitances $C_1$, $C_2$, and voltage sources, $N_{a1} i_a$, $N_{a2} i_a$, will form a balanced bridge. We shall then have $i_1 = i_2$. Under this condition $i_3$ will be unaffected by $i_a$. What this means physically is that the current in Inductor $a$ will produce zero magnetic flux in the center limb of the magnetic core. Thus the operation of Inductor $b$ will not be affected by the current in Inductor $a$. Under the same condition of $C_1 N_{a1} = C_2 N_{a2}$, the current in Inductor $b$ will produce equal but opposite voltages on the two windings of Inductor $a$. This results in a zero net voltage across Inductor $a$, meaning that the current in Inductor $b$ will also not interfere the operation of Inductor $a$. 
By adding a secondary winding $N_{bs}$ to the center limb of the integrated inductor/transformer given in Fig. 7(a), an integrated inductor/transformer is formed, as shown in Fig. 8(a). Note that the inductor winding $N_{b}$ in Fig. 7(a) now becomes the primary winding $N_{bp}$ in Fig. 8(a). Here $N_{bp}$ and $N_{bs}$ are the two windings of the transformer, and $N_{a1}$ and $N_{a2}$ together form the winding of the inductor.

It can be proved that, if $C_1N_{a1} = C_2N_{a2}$, the operations of the inductor and the transformer will be independent of each other.

C. Integrated Transformer/Transformer

By adding secondary windings $N_{a1}$ and $N_{a2}$ to the outer limbs of the integrated inductor/transformer shown in Fig. 8(a), an integrated transformer/transformer is formed, as Fig. 9(a). The corresponding z-parameter model of the integrated transformer/transformer is shown in Fig. 9(b). It can be proved that, if $C_1N_{a1} = C_2N_{a2}$ and $C_1N_{a1} = C_2N_{a2}$, the operations of the two transformers will be independent of each other.

IV. CONVERSION OF Z-PARAMETER MODEL TO EQUIVALENT-CIRCUIT MODEL

The z-parameter models of magnetic components developed in Section III are very useful for computer simulation and design purposes. However, electronic engineers often find difficulties in understanding the physical meanings of these z-parameter models. It will therefore be helpful if these z-parameter models can also be converted into their equivalent-circuit models.

Based on the example shown in Fig. 10(a), we propose the following steps to derive the equivalent-circuit model of an integrated magnetics:

1) By replacing each electric/magnetic interface of the integrated magnetics with an appropriate z-parameter two-port network, develop a z-parameter model of the integrated magnetics first. When this step of operation is performed on the integrated magnetics given in Fig. 10(a), a z-parameter model can be found as shown in Fig. 10(b). Note that, in Fig. 10(b), $C_{11}$ and $C_{12}$ are added to model the leakage magnetic paths of the magnetic core.

2) Take away the parts of the z-parameter model that represent the windings of the integrated magnetics. This results in a model that contains only the magnetic components. The resultant model is referred to as the magnetic model. When this step of operation is performed on the z-parameter model shown in Fig. 10(b), we get the magnetic model as shown in Fig. 10(c).

3) Assign a name to each loop in the magnetic model. In this example, the names assigned are A, B, C, D, and E, as shown in Fig. 10(c).

4) Assuming that each loop is converter into a node, carry out a duality circuit transformation on the magnetic model shown in Fig. 10(c). After the transformation, we get the duality circuit shown in Fig. 10(d). Note that loops A, B, C, D, and E in Fig. 10(c) now become nodes A, B, C, D, and E in Fig. 10(d).

5) Replace each of the current sources in the duality circuit shown in Fig. 10(d) by an ideal $N:1$ transformer, where $N$ is the number of turns of the winding concerned. When this step of operation is performed on the magnetic model given in Fig. 10(d), we get the resultant equivalent-circuit model as shown in Fig. 10(e). It is interesting to note that the leakage magnetic paths $L_{11}$ and $L_{12}$ in Fig. 10(b) have now become leakage inductances $L_{11}$ and $L_{12}$ in Fig. 10(e).

It should be understood that, as far as the external behavior is concerned, the z-parameter model shown in Fig. 10(b) and the equivalent-circuit model shown in Fig. 10(e) are identical. Both models can be used for circuit analysis and computer simulations.

Sometimes it may be convenient for one of the windings to be referred to as the primary winding. If this is the case, the ideal transformer of the primary winding may be replaced by a pair of wires connecting the output to the
input (effectively an ideal 1:1 transformer without galvanic isolation). All inductances should then be scaled by the factor $N_p^2$, where $N_p$ is the number of turns of the primary winding. Also the transformer ratios should be scaled to $N_s/N_p$, where $N_s$ is the number of turns of the secondary winding concerned. When this conversion is performed on the equivalent-circuit model given in Fig. 10(e), assuming $N_p$ to be the primary winding, we get an alternate form of the equivalent-circuit model of the integrated magnetics, as shown in Fig. 11. Note that in Fig. 11, $L_{m1} = N_p^2 L_1$, $L_{m2} = N_p^2 L_2$, $L_{m3} = N_p^2 L_3$, $L_{K1} = N_p^2 L_{K1}$ and $L_{K2} = N_p^2 L_{K2}$.

Fig. 10. (a) Winding arrangement of an integrated magnetics. (b) Z-parameter model. (c) Magnetic model. (d) Duality circuit. (e) Equivalent-circuit model of (b).

V. TEACHING OF MAGNETIC CIRCUITS TECHNICAL INFORMATION

The z-parameter/gyrator model of magnetic circuits has been extensively used in our research works on integrated magnetics [9], [10], [11], [12], [13], [14]. It has been proved to be an extremely useful tool. However, a lot of efforts are required in order to promote the use of the z-parameter/gyrator model, because engineers/students have not been exposed to it when they study magnetic circuits. It appears that, in order to fundamentally solve the problem, we have to reconsider the way the topic of magnetic circuits is taught in universities.

In the teaching of magnetic circuits, traditionally reluctance is modelled as resistance and mmf is modelled as emf. In this way, the flux and flux density of a magnetic circuit can be easily calculated. This approach of teaching is helpful to enable students to “visualize” how magnetic flux “flows” in a magnetic circuit. It is also our believe that such an intuitive understanding is necessary when students encounter magnetic circuits the first time. However, students should be warned that there are actually deficiencies in modelling reluctance (which is a lossless component) as resistance (which is a lossy component). Keeping this in mind, students would be better prepared to accept the z-parameter model to be introduced later.

As far as timing is concerned, the z-parameter model should be introduced in the curriculum whenever there is a need for mixed simulation of electric and magnetic circuits. In this way students should readily appreciate the real reason for introducing the z-parameter model. Example simulations involving magnetic components used in modern power electronics circuits, taking into account various leakage magnetic paths, could be used to convince students of the power of z-parameter models. The conversion of z-parameter model to equivalent-circuit model, as described in Section IV, should be useful to help students develop the equivalent circuits of complex magnetic components and to visualize the effects of leakage magnetic paths.
Based on the gyrator model, the z-parameter model of magnetic circuits has been developed. The advantages of the z-parameter model include

1) true modelling of the behavior of mixed electric and magnetic circuits;
2) easy acceptance by engineers and students in the electrical engineering discipline; and
3) close resemblance to the physical structure of magnetic components, making the modelling of complex integrated magnetics and leakage inductances much easier.

Some suggestions on how the z-parameter model should be introduced into the curriculum of electrical engineering courses are given. Hopefully the introduction of the z-parameter model will solve a long-standing problem in the modelling, analysis, and simulation of magnetic circuits.

This section describes the contribution of the paper so that even if readers have not read the body of your paper, they still understand the main idea of the paper. You should not insert any discussion statements in this section because they can be fitted in the previous sections. Even if the author only designed and tested a system, he can also state the achievement in this section. The following statement is an example: The theory has been implemented in an electronic circuit. The circuit has been prototyped and tested. The experimental results agreed very well with the theoretical prediction and verified the theory proposed.

REFERENCES

Abstract – Electric automobiles are clean, efficient, and powerful but are limited in range. Hybrid designs seek to enhance range through the use of liquid fuel. The energy, force, and power needs of a typical car are reviewed. The relationship to fuel cells as energy sources is discussed. Opportunities in the electrical arena, the mechanical arena, and the fuel cell arena are presented. Two commercial hybrid vehicle examples are presented. The convergence of developments in these areas will dominate hybrid designs as commercial production continues to ramp up.

I. INTRODUCTION

This paper is based on [1], in which the sequence of developments in hybrid electric vehicles is described. Added to the discussion of [1] is an overview of key challenges that need to be addressed as modern electric and hybrid vehicles continue to develop. Much present work seeks to develop fuel cells for primary automotive energy, and this recent work motivates a discussion of electrical, mechanical, and fuel cell challenges that will influence electric and hybrid vehicle design through about 2015.

Electric automobiles led the development of other vehicles, appearing by the 1990s and peaking in production after 1910 [2]. The vehicles were clean, easy to use, and required much less maintenance than the gasoline and steam vehicles of the day. Hybrid electric vehicles also appeared very early. Ferdinand Porsche’s early design [3], which can be observed at [4], dates from 1900. It used an engine-generator set, and had electric motors in the wheels for traction. No gear shifting was needed. Both electric and hybrid architectures became less popular as the technologies of fuel-driven engines evolved. Many authorities argue that low fuel cost and the rapid acceptance of the mass-produced Ford Model T led to their decline and virtual disappearance in the 1920s [5].

Hybrid vehicle technology held its ground in larger applications, and remains a significant industrial transportation system today. The diesel-electric locomotive appeared in the 1920s. It uses a large diesel engine to drive an electric generator. Power from the generator is controlled and delivered to electric motors that provide motive force. Many ships, submarines, and large off-road trucks use the same architecture.

Diesel-electric hybrids exhibit the key advantages of a hybrid configuration:

- On-board energy is stored as liquid fuel, with energy per unit mass far greater than batteries, flywheels, or other storage approaches.
- Mechanical energy is converted directly to electric form with no adjustable gearboxes, drive shafts, linkages, or other large mechanical connections.
- The engine can operate near its most efficient conditions since it is decoupled from user needs.
- Energy conversion in electric machines is efficient, with excellent power-to-weight ratio and flexible control.

Thus diesel-electric hybrids remain the transportation system of choice at levels of about 500kW and higher.

II. ENERGY, POWER AND FORCE NEEDS

Energy, power and force requirements dominate many design choices in electric and hybrid vehicles. In an electric car, for example, range is governed by stored energy. Key figures of merit for energy storage include energy per unit mass and power per unit mass. Energy per unit volume can also be important, as in vehicles that use on-board hydrogen fuel. Table I provides a summary based on energy for a few major storage technologies.

<table>
<thead>
<tr>
<th>Storage technology</th>
<th>Mass density</th>
<th>Volume density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lead-acid batteries</td>
<td>100kJ/kg</td>
<td></td>
</tr>
<tr>
<td>Compressed air, 10 MPa</td>
<td>80kJ/kg</td>
<td></td>
</tr>
<tr>
<td>Electrolytic capacitors</td>
<td>0.2kJ/kg</td>
<td></td>
</tr>
<tr>
<td>Double-layer capacitors</td>
<td>20kJ/kg</td>
<td></td>
</tr>
<tr>
<td>Lithium-ion batteries</td>
<td>600kJ/kg</td>
<td></td>
</tr>
<tr>
<td>Gasoline</td>
<td>43000kJ/kg</td>
<td>29000kJ/L</td>
</tr>
<tr>
<td>Hydrogen(liquid)</td>
<td>120000kJ/kg</td>
<td>8000kJ/L</td>
</tr>
</tbody>
</table>

The values in Table I show why batteries have long been the storage approaches for electric cars: even conventional lead-acid cells store much more energy per unit mass than mechanical and electrical alternatives. Even taking into account the limited thermal efficiency of fuel processes, gasoline stores about 100 times as much useful energy per unit mass as lead-acid batteries, and about 20 times as much as energy-dense lithium-ion cells. Hydrogen stores more energy per unit mass than any other fuel, but its low mass density limits its value as a transportation energy storage method.

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Grainger Center for Electric Machinery and Electromechanics
Department of Electrical and Computer Engineering
University of Illinois, Urbana, Illinois USA, machines@ece.uiuc.edu
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In terms of power, the process of refueling delivers energy at extraordinary rates. For example, if a fuel tank with capacity of 60L is filled in five minutes, the effective energy transfer rate is 6MW. With batteries, rates are limited, and mass power density is an important figure of merit. Conventional batteries are hard pressed to deliver more than 500W/kg, and even the best designs are unlikely to deliver more than 1000W/kg. Power density is often a key limiting factor in hybrid vehicle design. A hybrid design rated for 100kW of peak power would require at least 200kg of batteries just to support this energy rate.

Force requirements for automobiles can be computed from well-known relationships [6]. Table 2 lists several computed results, based on methods in [6], for a conventional car and estimated for the General Motors EV1 electric commuter vehicle. The results show a wide gulf between continuous power requirements under benign conditions and peak power requirements for aggressive acceleration.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Need, 1800kg car</th>
<th>Need, EV1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Move on 25% grade 100km/h cruise, level 11kW road</td>
<td>4600N thrust 3800N</td>
<td>8kW</td>
</tr>
<tr>
<td>Maintain 100 km/h, 36kW 5% grade</td>
<td>29kW</td>
<td></td>
</tr>
<tr>
<td>Peak acceleration, 0-95 km/h, (time) 80kW (12s)</td>
<td>102 kW (11s)</td>
<td></td>
</tr>
</tbody>
</table>

The pinnacle of electric vehicle redevelopment has been the General Motors EV1, a two-seat electric sports car with exceptional performance. A view is provided in Fig. 1 [7]. Although this vehicle generated wide interest and consumer demand, it was never seriously marketed by General Motors. The vehicles were recalled when difficulties appeared with the battery chargers, and apparently nearly all have since been destroyed by the manufacturer.

The EV1 showed the promise of modern electric vehicle designs:

- A small induction motor was able to deliver 102 kW in a tight traction package, and set a new standard for traction power-to-weight ratio.
- Supported smooth operation and high torque. A modified EV1 set the land speed record for electric vehicles.
- A paddle-style contactless charging system showed new ways to manage electrical safety.
- Energy recovery during braking was smooth and efficient.
- Consumers who tested the car were invariably impressed by the performance, quietness, and smooth operation.

The drawback was the heavy battery pack. Even with almost 600kg of batteries, the typical range was less than 150km. Although this range is adequate for many commuters, it was thought to be too low for mass markets.

Improvements in lithium-ion batteries are encouraging further consideration of all-electric cars [8]. Even the best batteries, however, are unlikely to store more than 300 W-hr/kg (about 1000kJ/kg). In principle, lithium batteries support most commuting needs. If rapid recharge becomes feasible, long trips might be within reach of the technology, but for the foreseeable future, energy storage remains the limiting factor for electric cars.

Since the force and power requirements in Table II are not especially difficult for electric vehicles, hybrid vehicles seek to apply electric drives but store energy as a liquid fuel. Good hybrid vehicle designs today can achieve approximately double the fuel economy of equivalent conventional cars. Perhaps more significant is the impact on tailpipe emissions. A hybrid design has at least five characteristics that reduce emissions:

1. The engine can be smaller since the electric motor can assist during peak requirements.
2. The engine can shut off when the car stops.
3. The engine can be controlled to operate only near an optimum emissions condition.
4. Stored battery energy can be used to prepare the emission system for cold starts.
5. Braking energy can be recovered and stored.

In addition, efficient engines not well-suited to direct use can be applied. The Toyota Prius, for instance, uses an Atkinson Cycle engine that is slightly more efficient than a conventional Otto Cycle engine. Some test vehicles have used even more efficient Brayton Cycle engines.

The combined effect of these characteristics yields a large impact on emissions. The Toyota Prius achieved “Super Ultra Low Emission Vehicle” (SULEV) status when it entered North American markets in 2000. The SULEV requirements result in about 90% reduction in hydrocarbon emissions, and substantial reductions in oxides of nitrogen and even carbon dioxide.

III ELECTRICAL AND MECHANICAL OPPORTUNITIES

It is well known that median daily automobile usage is less than 50 km. Given the inherent flexibility, high efficiency, and other advantages of electric drives, there is incentive to use all-electric vehicles to satisfy most daily driving needs. Since 50 km usually represents a round-trip distance, a car with a range of just 40 km – well within the typical range of the EV1 – could cover far more than half of actual driving. From a marketing perspective, such a vehicle, with less than 10% of the range of a typical car, would be too risky. The possibilities motivate the concept...
of a “plug-in hybrid”, a vehicle with electric range of 20-50 km and a hybrid system to deliver long range when the need arises. Such a vehicle would offload a large percentage of transportation energy to the electricity grid, with associated benefits.

Plug-in hybrids are associated with many opportunities for engineering advances in both electrical and mechanical arenas. On the electrical side, these vehicles would stimulate price-based utility metering to control electrical demand. The right process could improve load factor substantially on the grid. Other opportunities include intelligent battery chargers that could provide the longest possible battery life, intelligent grid interfaces that could allow battery energy to support a utility under emergency conditions, and system-level controls to minimize overall energy consumption. Challenges in power electronics in particular offer nearly unlimited opportunity in this context.

On the mechanical side, the flexibility, fast dynamics, and high-fidelity torque control capabilities of electric drives open many new possibilities. An early prototype [9] used fast motor control to eliminate the clutch in a manual transmission. Such a process provides an opportunity for intelligent gearboxes that enhance drive train efficiency and performance. For example, the capabilities of an electric drive are greatly extended if a three-speed gearbox is provided. Another emerging development is the integrated starter-alternator [10], in which all or part of the electric drive in a hybrid is closely coupled to the engine. Still others include opportunities when two separate drive motors are used, opportunities to incorporate flywheels, and even ways to use electric machines to counteract torque pulses from the engine [11].

Regardless of whether a vehicle is electric or hybrid, an important combined electrical and mechanical opportunity lies in increased use of electromechanical devices as part of the overall system. Electric power steering [12], water pumps, air conditioning compressors, and other major accessories enhance system efficiency while improving performance. Looking further into the future [13-16], electromechanical devices such as valve actuators will enhance the performance of engines themselves.

IV. FUEL CELL OPPORTUNITIES

Fuel cells act like “flow-through” batteries, providing an electrochemical potential when fuel (generally hydrogen) is present. Fuel cell vehicles are sometimes discussed as a long-term electric vehicle technology that overcomes the limitations of batteries. In the automotive size range, fuel cells are expected to be about 50% efficient in converting from fuel to electrical output [17]. This contrasts with the typical 20% efficiency or less in a modern car. Hybrids can improve the conventional situation by making more effective use of the engine, since a high-quality diesel engine with electric generator load can exceed 40% efficiency. But fuel cells remain of special interest because they offer the potential of carbon-free transportation processes.

Although fuel cells resemble batteries in many ways, they have distinctive characteristics unlike those of typical secondary (rechargeable) batteries. A simulated voltage-current characteristics for a proton-exchange-membrane (PEM) fuel cell is shown in Fig. 2. It illustrates two of the differences. First, the voltage shows wide variation over the operating range. A power converter designed for a fuel cell must cope with a 2:1 voltage range or more. Second, the curve depends on fuel flow. To use fuel effectively and achieve high efficiency, fuel delivery must be adjusted based on the electrical load.

The latter characteristic gives rise to a third major difference: practical fuel cells have slow response times, often on the order of seconds or minutes, in response to electrical load changes. In a vehicle, this means that batteries or other fast storage devices must be present to handle transients. A fuel cell vehicle thus becomes a type of hybrid car, in which a fuel cell takes the place of the engine but the rest of the system is unchanged.

The development of fuel cells continues. Many of the challenges are in materials engineering. PEM fuel cells, for example, rely on their membrane as the primary chemical exchange mechanism. Today’s membranes can be compromised by impurities such as CO and hydrocarbons, and purity of the hydrogen fuel becomes a major limitation. Membranes that can function over the full life of a car remain a challenge.

Power electronics is a central issue for fuel cells. A converter such as the one in Fig. 3 is needed for fuel cell conversion. Like any switching converter, this circuit operates at relatively high frequency to reduce the size of the magnetic. Techniques to interface fuel cells with the batteries or capacitors needed to operate the complete system are the subject of active research at many places.

V. COMMERCIAL HYBRIDS

An integrated starter-alternator (ISA) of sufficient size allows the engine to be stopped and started conveniently during stopped traffic. If the ISA is large enough to permit energy recovery during braking, the combined
system is termed a mild hybrid [18]. The Honda Insight, the first modern hybrid car on the North American market, is considered a mild hybrid by many experts. The car, shown in Fig. 4, uses an ISA architecture to maximize fuel economy. It has a lightweight two-seat chassis.

A more sophisticated parallel hybrid system can be found in the Toyota Prius (Fig. 5) and the more recent Ford Escape hybrids [19]. In this system, the engine and primary electric machine are connected through a sun-planet gear set. This provides a degree of independence between the two energy sources.

The diesel-electric drive train is an example of a series hybrid vehicle architecture. In a system of this type, the multiple energy resources are brought together in electrical form. This has the advantage of decoupling the engine from vehicle performance, since the engine drives a generator rather than an axle. The Toyota and Ford drive trains achieve a degree of operation in this regard by providing a second electric machine to serve as a generator. Series designs offer energy source flexibility. Fuel cell vehicles, for example, are series hybrids. Turbine-generator series hybrids have also been constructed.

VI. CONCLUSION

Electric vehicles were common a century ago, an hybrid designs also appeared in the early 1900s. Thanks to recent innovations in power electronics and electric drives, electric and hybrid cars are reappearing. These vehicles offer significant technical challenges in electrical, mechanical, and materials engineering topics. The anticipated introduction of fuel cell cars offers opportunities for a range of technology advances. Today’s hybrid cars use self-contained ISA and parallel architectures. Plug-in hybrids that support short-range driving from electrical energy are expected in the next few years.

REFERENCES

Novel ZVS Three-Phase PFC Converters and Zero-Voltage-Switching Space Vector Modulation (ZVS-SVM) Control

Dehong Xu¹ and Bo Feng²

Abstract – In three-phase PFC converter, there exist severe switch anti-parallel diode reverse recovery problems. The effective measures of Compound Active-clamping and Minimal Voltage Active-clamping techniques in single phase PFC are extended to three-phase PFC. A family of Active-clamping ZVS soft switching PFC converter is derived. They can effectively suppress the diode reverse recovery and realize ZVS for all the switches. In order to reduce the number of switching for the auxiliary switch, a ZVS space vector modulation (ZVS-SVM) is proposed. The switching frequency of the main switch and the auxiliary switch is fixed. In the proposed circuit only one auxiliary switch is needed, which can realize ZVS for all the switches. At the same time the input current waveform is improved. One DSP controlled 4kW ZVS Compound Active-clamping PFC converter prototype is implemented.

Keywords – Three-phase PDC, zero-voltage-switching, space vector modulation

I. INTRODUCTION

Six-switch three-phase boost rectifier is one of the preferred topologies for implementing the active input current shaping in three-phase AC-DC converter. It has several advantages such as lower current stress, high efficiency, and small input EMI filter. However, the anti-parallel diodes of all the switches in the rectifier experience reverse recovery problem which will cause severe switching loss, high di/dt and EMI problems. The anti-parallel diode reverse recovery loss is one of the main losses in the six-switch boost rectifier [1].

For passing years, many works about soft switching for three-phase rectifier or inverter have been undertaken to solve the diode reverse recovery problem. The DC rail ZVT boost rectifier proposed in [2] adopts a DC rail diode and a ZVT branch to suppress the diode reverse recovery and to realize the ZVS of the main switches. However the auxiliary switch is hard switching. The auxiliary resonant commutated pole (ARCP) converter put the soft-switching circuit at the ac side to reduce the auxiliary circuit conduction loss and facilitate bi-directional power flow. However it needs six extra auxiliary switches to realize the soft switching [3]. The resonant dc link (RDCL) proposed in [4][5] has the simplified topology. However the switches in RDCL converter suffer from high voltage stress (about 2.5 times the output voltage). The active clamped RDCL in [6] has a low voltage stress (about 1.3 ~ 1.4 times the output voltage). Instead of using PWM control, RDCL and ACRDCL converters have to use discrete pulse modulation (DPM), which normally causes undesirable sub-harmonics. DPM requires the dc-link resonating frequency to be several times higher than the switching frequency of the PWM converter for the same current spectral performance [1][6].

In this paper, the concept of Compound Active-clamping and Minimal-voltage Active-clamping [9][10] in single phase PFC is extended to three-phase PFC. A family of Active-clamping ZVS three-phase PFC is proposed. To suppress the diode reverse recovery of the three-phase switch, a novel zero voltage switching space vector modulation (ZVS-SVM) for the Active-clamping ZVS three-phase PFC is proposed. The switching frequency of both the main switches and the auxiliary switch is fixed. The switching frequency of the auxiliary switch is equal to that of the main switches. The diode reverse recovery of the switch anti-parallel diode is suppressed and all the switches can be turned on under zero voltage condition. The voltage stress on the switches is much lower than that on the RDCL and the ACRDCL converters.

A 4kW DSP (TMS320F2407A) controlled Compound Active-clamping ZVS Three-Phase PFC is built to verify the theory.

II. NOVEL ZVS THREE-PHASE PFC CONVERTER FAMILY

In single phase PFC converter, there also exists severe diode reverse recovery problem. In the passing years, there are many significant works to solve the diode reverse recovery problem [7]-[10]. Among them, the Compound Active-clamping (CAC) and Minimum-voltage Active-clamping (MVAC) techniques can effectively suppress the diode reverse recovery and create ZVS for both the main switch and the auxiliary switch. Fig.1 and Fig.2. show the CAC and MVAC PFC converters separately. The key ideas of these two Active-clamping soft-switching techniques are as follows:

1. An inductor is placed in series with the diode and the main switch. The inductor can suppress the diode reverse recovery and reduce the diode reverse recovery related loss.
2. A clamping branch composed of one clamping capacitor and one auxiliary switch is placed in parallel with the inductor, thus it can clamp the voltage stress of the inductor when the main switch turns off. The auxiliary circuit can also help to realize ZVS for the two switches.
In three-phase PFC, the diode reverse recovery problem in every phase is similar to that in single-phase PFC. Thus we extend the concept of Active-clamping techniques to three-phase PFC, and can get Compound Active-clamping three-phase PFC converters that are shown in Fig. 3 and Fig. 4.

The ZVS PDC converters in Fig. 5 and Fig. 6 use only one auxiliary switch, one resonant inductor and one clamping capacitor. Since in most time of a switching cycle, the auxiliary switch is conducting, there is generally enough energy circulating in the auxiliary branch. When the auxiliary switch is turned off, the current in the resonant inductor will discharge the parallel capacitors of the main switches, then the main switches can be turned on under zero voltage condition. When the main switches are turned on, the resonant inductor can suppress the reverse recovery current of the anti-parallel diode of the opposite switch in the same pole.

Although the topology is the same as that of ACRDCL converter, the control pattern is quite different. To suppress the diode reverse recovery for the switches in three phase. Special control methods should be taken. In this paper, a novel Zero-Voltage-Switching Space Vector Modulation (ZVS-SVM) is proposed. Under the ZVS-
SVM control, all the diode reverse recovery of the switch anti-parallel diodes are suppressed and all the switches can be turned on under zero voltage condition. The switching frequency of both the main switches and the auxiliary switch are fixed. The switching frequency of the auxiliary switch is equal to that of the main switches.

Among the three-phase PFC converters, the VIENNA rectifier employs only three active switches and can achieve good current quality. However there also exists severe diode reverse recovery problem that limit the switching frequency of the VIENNA rectifier. In this paper, the concepts of Compound Active-clamping and Minimal-voltage Active-clamping are extended into the VIENNA rectifier and two kinds of ZVS VIENNA rectifies are got. Fig. 7 shows the CAC ZVS VIENNA rectifier and Fig. 8 shows the MVAC VIENNA rectifier.

III. ZERO VOLTAGE SWITCHING SPACE VECTOR MODULATION (ZVS-SVM)

In space vector modulation scheme, the phase voltage waveform and voltage space vector definition are shown in Fig. 9. V0 to V7 are the eight different switching states in the converter operation. In ZVS SVM, the whole utility cycle is divided into 12 sectors.

In three-phase PFC, since there are three legs in the main bridge, the auxiliary switch must be activated three times per switching cycle if the switches in the three legs are modulated asynchronously. Actually in one sector the switch states of the phase with the highest current is fixed, only other two phases need to be considered about the diode reverse recovery suppressing and ZVS condition. If the switches in the other two phases are so controlled that the turn on time of the other two phase switches is synchronized, the diode reverse recoveries of them can be coped with at the same time. Thus the auxiliary switch need only to operate once in one switching cycle to resonant the DC bus to zero and create ZVS condition for the two phase switches and suppress the diode recoveries of both phases. Thus the auxiliary switch can work at the same frequency with the main switches.

Since the operation of the converter is symmetrical in every 30°, to understand the operation of the circuit, we assume that the converter is operating in sector 2 as an instance where input current Ia>0, Ic<0 and Ib<0. There are three switch states in one switching cycle, as shown in Fig. 10. The three switch states are state 100, state 110 and state 110. The equivalent circuits of these three states are shown in Fig. 11. In this sector, phase A has the highest input voltage and the highest input current. Switch S1 is always on while switch S4 is always off in sector 2. The switches in the other two phases are controlled in the PWM manner. According to the proposed ZVS-SVM scheme, the switch S3 and S5 are to be turned on simultaneously when switching state 100 changes to state 111.

In state 100, although the driving singles of S1, S6 and S2 are effective, it is the anti-parallel diodes of S1, S6 and S2 being conducting. If the rectifier state is changing from 100 to 111, switch S3 and S5 will starts to conduct while the anti-parallel diodes of S6 and S2 will turn off. During the commutation from the lower-leg diodes to the upper-leg diodes to the upper-leg switches there exist diode reverse recovery problems. In state 100, switch S7 is conducting and the current in the resonant inductor Lr is increasing. The energy stored in the resonant inductor can help to realize ZVS for both switch S3 and S5 in the transition from state 100 to 111.

In state 111, the energy in the input inductor is increasing while the current in the resonant inductor Lr is charging the clamping capacitor Cc. Later the current in Lr changes its direction.

In he state transition from 111 to 110, switch S5 is turned off, the current in input inductor Lc will charge S5’s paralleled capacitor and discharge S2’s paralleled capacitor. Thus S5 is ZVS turned off. Once the voltage on S5 decrease to zero, S2’s anti-parallel diode starts to conduct. Therefore the current naturally transfers from S5 to S2’s anti-parallel diode.

In the state transition from 110 to 100, S3 is turned off, the current in input inductor Lb will charge S3’s paralleled capacitor and discharge S6’s paralleled capacitor. Thus S3 is ZVS turned off. Once the voltage on S3 decrease to zero, S6’s anti-parallel diode starts to conduct. Therefore the current naturally transfers from S5 to S2’s anti-parallel diode.
Thus with the ZVS-SVM control the ZVS Active-clamping three-phase PFC can realize ZVS for all the switches and suppress all the diode reverse recovery. The switching frequency of the auxiliary switch is equal to that of the main switch.

The following assumptions are made to simplify the analysis of the proposed CAC PFC converter:

- The capacitances C1 to C6 paralleled with main switches S1 to S6 respectively include parasitic capacitance and external capacitance. The capacitance C7 paralleled with the auxiliary switch S7 also includes parasitic capacitance and external capacitance.
- The input filter inductors L1, L2, L3 are so large that their currents can be considered as constant current source in one switching cycle.
- The output filter capacitor Co is represented by a constant voltage source.
- The value Cc is large enough so that the voltage can be seen as a constant.
- The resonant frequency of Cc and Lr is much lower than the operation frequency of the converter.

The steady-stage and key waveforms of the CAC ZVS three-phase PFC are shown in Fig. 12 and Fig. 13 respectively. The switching cycle can be divided into 8 stages.

Stage 1 (t0-t1): In this stage, S1, S2, S6 and the auxiliary switch S7 are on. The energy in input inductor is sending to the output. The current in resonant inductor Lr increases at the rate of
\[
\frac{di_c}{dt} = \frac{V_{cc}}{L_r}
\]  
(1)

**Stage 2 (t1-t2):** In t1, S7 is turned off, the resonant inductor Lr will discharge the main switch S3, S5, S4’s paralleling capacitors C3, C4, C5. At time t2, the voltages on these capacitors decrease to zero and the anti-parallel diode of these main switches start to conduct. Then S3 and S5 can be turn on with zero voltage switching. At time t2 the voltage on S7 reaches \( V_o + V_{cc} \).

**Stage 3 (t2-t3):** From this stage, the anti-parallel diode of S6 and S2 experience diode reverse recovery. Due to the existence of the resonant inductor Lr, the diode reverse recovery is suppressed. At time t3, the current of the anti-paralleled diodes of both switch S6 and S2 drop to zero.

**Stage 4 (t3-t4):** At t3, the voltage on S6 and S2 start to rise. Lr, C2, C6 and C7 start to resonance. The voltage on S7 starts to decrease. At t4, the voltage on S7 decrease to zero, and the anti-parallel diode of S7 start to conduct. S7 can be ZVS turn on.

**Stage 5 (t4-t5):** At t4, the diode reverse recovery process completes. The circuit enters the state 111. The main switch S1, S3, S5 and the auxiliary switch S7 are on. The resonant inductor is charging the clamping capacitor Cc.

**Stage 6 (t5-t6):** At t5, the main switch S5 is turned off. Since the existence of C5 and C2, it is ZVS turn off. The input inductor Lc will charge C5 and discharge C2.

**Stage 7 (t6-t7):** At t6, the voltage on S2 decrease to zero, the anti-parallel diode starts to conduct. S2 can be ZVS turn on. The circuit enters state 110. The lasting time is decided by the SVM control.

**Stage 8 (t7-t8):** At t7, the main switch S3 is turned off, since the existence of C3 and C6, it is ZVS turn off. The input inductor Lb will charge C3 and discharge C6. At t8, the voltage on S6 decrease to zero, the anti-parallel diode starts to conduct. S6 can be ZVS turn on. The circuit enters state 100. After t8, the next switching cycle starts again.

![Fig. 12: operation stages of CAC ZVS PFC](image1)

![Fig. 13: Steady-state waveforms of the proposed converter](image2)

**V. THEORETICAL ANALYSIS OF CAC ZVS THREE-PHASE PFC CONVERTER**

In every switching cycle there are three switching states, if we still take sector 2 as an example, the three states are 100-111-110. The duration of the three states can be
expressed as T1, T0, and T2, where T is the operation period.

\[ T_1 = \sqrt{3} \frac{U_{dc}}{E_{dc}} T \sin\left(\frac{\pi}{3} - \theta_r\right) \]  
\[ T_2 = \sqrt{3} \frac{U_{dc}}{E_{dc}} T \sin \theta_r \]  
\[ T_0 = T - T_1 - T_2 \]

(2)
(3)
(4)

A. Voltage stress on the switches

The maximum voltage stress on the switches is

\[ V_{max} = V_a + V_{cc} \]

\[ L_r \left( I_a T_1 + I_a T_2 + V_e \sqrt{\frac{3C + C_2}{L_r}} \right) \]

\[ = V_a + \frac{I}{T} \]  

(5)

In sector 2, the voltage stresses on the switches vs. the output voltage are shown in Fig.. The switch voltage stresses are only a little higher than the output voltage.

B. Soft switching condition

The auxiliary switch is always zero-voltage turn-on condition. However the main switches satisfy zero-voltage turn-on condition when there is enough energy stored in resonant inductor to discharge the paralleling capacitor of the main switches. The zero-voltage switching condition for the main switch is:

\[ 2I_a \frac{I_1}{T} + 2I_a \frac{I_2}{T} - I_a \frac{K \cdot V_{CE(on)}}{L_r} \cdot T > 0 \]  

\[ 0 < k < 1 \]

(6)

Where Vce(on) is the conduction voltage drop of the auxiliary switch. It is easy to achieve soft switching in the ZVS-SVM scheme.

VI. EXPERIMENTAL RESULTS

A 4 kW prototype of the ZVS-SVM controlled CAC PFC converter, as shown in Fig.5 (a), is built to verify the theory, which is controlled by DSP (TMS320F2407A). The parameters of the circuit are: phase voltage Vin=220Vac, output voltage Vo=620Vdc, L=12mH, Lr=80μH, Cc=45μF. The parallel capacitors of the switches are C1=C2=...=C7=2nF. The operation frequency f=12.8kHz. The main switches, S1~S6: IRGPH50K. The auxiliary switch S7: CT60AM-20F.

Fig. shows the input voltage and the input current. The harmonic spectrum of the input current is shown in Fig..

The measured Power factor is 0.998 and the THD is 3.295%.

The CE voltage and the driving signal of the main switch and the auxiliary switch are shown in Fig. 17 and Fig. 18 respectively. As can be seen that the CE voltage drop to zero before the driving signal turn high. Thus both the main switch and auxiliary switch is ZVS turn on.

The clamping voltage on the clamping capacitor is less than 40V, as shown in Fig.. Thus the voltage stress of the switches in the proposed rectifier is only about 660V (Vo+Vcc). So the voltage stress is lower.
The efficiency of the ZVS PFC rectifier is shown in Fig. 20. The efficiency of a hard switching counterpart is also shown in Fig. 20.

VII. CONCLUSION

A family of Active-Clamping ZVS Three-Phase PFC is proposed. A specially designed ZVS-SVM for the soft switching PFC converter is proposed too. It can suppress all the diode reverse recovery, meanwhile creating soft-switching condition for both the main switches and the auxiliary switch. The switching frequency is fixed, and the auxiliary switch works at the same frequency with other switches, thus the rectifier can work at higher frequency.

The voltage stress in the Active-clamping ZVS Three-Phase PFC is lower. It is suitable for high-density rectifier application.

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Application of Active Disturbance Rejection Controller in PWM Voltage Source Rectifier

Xiao-zhong Liao 1,2, Li-wei Shao 1,2, Yan-lei Xiao 1

Abstract – The DC output voltage will deviate as disturbances in the PWM voltage source rectifier based on voltage oriented direct power control. A new strategy was proposed in this paper to solve this problem. The voltage controller is active disturbance rejection controller (ADRC). The load disturbance and other disturbances are contributed to the total disturbances, and then the total disturbances is estimated and compensated by extended state observer (ESO). Simulation results show that this new method has high power factor, low harmonic, fine dynamic performance. Further more it has better robust property to load disturbance.

Keywords - PWM rectifier; active disturbance rejection controller; voltage oriented direct power control

I. INTRODUCTION

Three phase PWM voltage source rectifier is widely used in reactive compensation, active filter, superconducting energy storage, high voltage direct current transmission and renewable energy, since it has some good properties such as sinusoidal AC line current, bidirectional power flow function and unity power factor control [1]. In most voltage source rectifier (VSR) control strategies, the direct power control based on the voltage oriented (VO-DPC) is a more interesting solution for industrial application because of its high power factor and low THD [2]. And the scheme of the system and the algorithm are simple [3]. However, when the load is changed or has a disturbance, the output DC voltage will deviate. Traditional PI controller can’t achieve a good performance on the above conditions.

Active disturbance rejection controller (ADRC) is a nonlinear controller. It has got many good performances in many fields. ADRC can estimate and compensate the total system disturbances in real time, combining with special scheme of nonlinear feedback to achieve good character. And the algorithm of ADRC is simple and easy to implement with digital control.

This paper proposes a new control method that ADRC is used in the PWM rectifier based on VO-DPC. In this novel control scheme, the ADRC is used to control the voltage loop. The extended state observer (ESO) is used to estimate the total disturbances including the change of the load. The principle is that ESO can estimate accurately and compensate the change of the load. Simulation results show that this new method has not only the better dynamic and static performance than fuzzy PID control, but also restrain the output voltage fluctuation caused by the change of the load available.

II. DIRECT POWER CONTROL BASED ON THE VOLTAGE ORIENTED IN PWM RECTIFIER

Fig. 1 shows the block diagram of the direct power control based on the voltage oriented (VO-DPC). The whole system consists of active power control portion and reactive power control portion. When the voltage vector is oriented to the d-axis in rotating d-q coordinates, the relations of output DC voltage \( V_{dc} \) and current \( i_d \) are linear. So the output DC voltage can be controlled by controlling the current. The instantaneous active power and reactive power can also be calculated from the voltage and the current on d-axis and q-axis. The converter switching states are appropriately selected by a switching table based on the instantaneous errors between the reference values and estimated values of active and reactive power. In order to get the unity power factor, the reactive current is usually set to zero.

Fig. 1: Block diagram of VO-DPC

VO-DPC has no coordinate transformation. The estimated values of the instantaneous power include not only fundamental component but also harmonic component, leading to the high power factor. The errors are determined by the width of the hysteresis loop controller. The scheme of the system is simple. The disadvantages of VO-DPC are high sampling frequency and variable switching frequency which leads to the random AC current and makes it is hard to design the input filter. Also when the load \( R_L \) on DC side is changed, the output DC voltage \( V_{dc} \) will fluctuate.
III. ACTIVE DISTURBANCE REJECTION CONTROLLER

ADRC mainly includes tracking-differentiator (TD), extended state observer (ESO) and nonlinear combination (NLC). It is widely used because of its simple control algorithm, easily be achieved, high precision, rapidly and good disturbance rejection [5].

Many real objects can be expressed as follows

\[
\begin{align*}
\dot{x}^{(n)} &= f(x, \dot{x}, \ldots, x^{(n-1)}, w(t), t) + bu \\
\dot{y} &= x(t)
\end{align*}
\]  

(1)

where \(w(t)\) is the total disturbances of the system which include the outer disturbances of the system and the inner disturbances caused by the model changed. \(x\) is the state value. \(y\) is the output value. \(u\) is the control value and \(b\) is the coefficient value. The main principle of the ADRC is to utilize ESO to observe and compensate the total disturbances, thus makes the system to be integral and serial system.

\[
\begin{align*}
\dot{x}^{(n)} &= b u_o \\
\dot{y} &= x(t)
\end{align*}
\]  

(2)

Through the feedback of the state errors, the control goal is obtained. Here, it is not important whether \(f(x, \dot{x}, \ldots, x^{(n-1)}, w(t), t)\) is known or unknown, linear or nonlinear, as long as it is limitary.

IV. THE ADRC DESIGN IN PWM RECTIFIER

A. Mathematical model of the PWM rectifier

The mathematical model of VSR in rotating d-q coordinates is

\[
\begin{align*}
\frac{dv_c}{dt} &= -\frac{3}{2} (i_q + j_s) - i_d \\
\frac{di_d}{dt} &= -\omega L_s + R_i = e_y - v_d S_d \\
\frac{di_q}{dt} &= \omega L_i + R_i = e_y - v_q S_q
\end{align*}
\]  

(3)

where \(v_d\) is the output DC voltage, \(i_d\) and \(i_q\) are the AC current on d-axis and q-axis. \(i_s\) is the load current. \(C\) is the DC-link capacitor. \(L\) is the filter inductance of reactor. \(R\) is the resistance of reactor. \(\omega\) is the voltage frequency. \(S_d\) and \(S_q\) are the on/off values in rotating d-q coordinates.

If ADRC be used in PWM rectifier, the controlled model needs to be transformed as (1). When the wastage of three phase PWM rectifier is ignored, the AC-link active power \(p_a\) is equal to the DC-link power \(p_d\), that is

\[
p_a = p_d
\]  

(4)

Taking equation (4) into d-q synchronous mode, the power equations are

\[
\begin{align*}
p_a &= \frac{3}{2} e_q j_s + \frac{3}{2} e_s i_d \\
p_a &= v_d i_d = v_a C \frac{dv_a}{dt} + \frac{v_a^2}{R_i}
\end{align*}
\]  

(5)  

(6)

Equation (7) is derived from (4)-(6) is given by

\[
\frac{dv_a}{dt} = -\frac{2}{R_i C} v_a^2 + \frac{3}{C} e_q j_s + \frac{3}{C} e_s i_d
\]  

(7)

Letting \(u = v_a^2\) then the equation (7) can be expressed as

\[
\frac{du}{dt} = -\frac{2}{R_i C} u + \frac{3}{C} e_q j_s + \frac{3}{C} e_s i_d
\]  

(8)

In the VO-DPC, the voltage is oriented on the d-axis and the voltage on the q-axis is equal to zero.

\[
\begin{align*}
e_y &= \sqrt{3} e_a \\
e_y &= 0
\end{align*}
\]  

(9)

where, \(e_a\) is a phase effect value of the AC-link voltage. Equation (8) can be expressed as

\[
\frac{du}{dt} = -\frac{2}{R_i C} u + \frac{3\sqrt{3}}{C} e_q j_s
\]  

(10)

Using

\[
\begin{align*}
a(t) &= -\frac{2}{R_i C} u \\
b &= \frac{3\sqrt{3}}{C} e_a
\end{align*}
\]  

(11)  

(12)

Then from equation (10), that becomes

\[
\frac{du}{dt} = a(t) + bi_d
\]  

(13)

From equation (13), it is known that the output DC voltage and the current on d-axis are satisfied with equation (1). So the first order ADRC can be utilized in the voltage loop. The equation (11) shows that total disturbances of the system \(a(t)\) include \(R_i\). ESO can estimate and compensate \(a(t)\) in time. If \(R_i\) is changed in the application, the effect of DC voltage fluctuation can be restrained.

B. Design of voltage ADRC in VO-DPC

Design of the ADRC usually uses nonlinear function to get the better result. It will increases the complex of the computation and nonlinear ADRC is difficult to implement. The linear function ADRC, linear ADRC, is used instead of nonlinear function sometimes. The performance of the linear ADRC is appropriately as same as the nonlinear ADRC. But it is much simple in computation and easy to be implemented. The linear ADRC is used in the scheme.
1) Design of tracking-differentiator (TD)

Design linear TD for the reference output DC voltage \( V_{d_c} \) is

\[
\begin{align*}
\cdot \quad v_{d_{c1}} &= v_{d_{c2}} \\
\cdot \quad v_{d_{c2}} &= -1.73 r v_{d_{c2}} - r^2 (v_{d_{c1}} - v_{d_{c}})
\end{align*}
\]  

Where, \( v_{d_{c1}} \) is tracking signal of \( v_{d_{c}} \). \( r \) is an adjustable parameter.

2) Design of extended state observer (ESO)

Design of the second order liner ESO for the actual output DC voltage in PWM rectifier can be written as the equation (15). ESO can get the estimation of the DC voltage states and the total disturbances of the system.

\[
\begin{align*}
\dot{e} &= z_1 - v_{d_{c}} \\
\dot{z}_1 &= z_2 - \beta_{z1} e + b i_d \\
\dot{z}_2 &= -\beta_{z2} e
\end{align*}
\]  

Where, \( v_{d_{c}} \) is DC-link voltage. \( Z_1 \) is the state estimation of the voltage \( v_{d_{c}} \). \( Z_2 \) is the estimation of the total disturbances \( a(t) \). \( \beta_{z1} \) and \( \beta_{z2} \) are two adjustable parameters.

If \( a(t) \) is not estimated by ESO exactly, there has steady state error in the system, even to be unsteady. So tuning the parameters of the ESO is very important. \( Z_2 \) shows the estimation of the total disturbances \( a(t) \). It affects the dynamic performance and accuracy. The value of \( Z_2 \) has a significant influence to the output of the system. There are disturbances in the output voltage of the PWM rectifier, so \( Z_1 \) plays a important role in estimating the state accurately for the real voltage.

3) Design of the linear combination

Then control law is given

\[
\begin{align*}
\dot{I}_{d_0} &= k (v_{d_{c1}} - z_1) \\
\dot{I}_{d} &= i_{d_0} - z_2 / b
\end{align*}
\]  

Where \( k \) is an adjustable coefficient, \( i_{d_0} \) is the d-axis current.

Fig. 2 shows the block diagram of ADRC.

V. SIMULATION RESULTS

The PWM rectifier with the whole control scheme has been simulated. The main electrical parameters of the power circuit are given as tab 1.

<table>
<thead>
<tr>
<th>AC-link voltage</th>
<th>Frequency</th>
<th>Inductance</th>
<th>Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>380V</td>
<td>50Hz</td>
<td>15mH</td>
<td>0.1Ω</td>
</tr>
<tr>
<td>DC-link Load</td>
<td>Reference</td>
<td>capacitor</td>
<td>voltage</td>
</tr>
<tr>
<td>660μF</td>
<td>100Ω</td>
<td>600V</td>
<td></td>
</tr>
</tbody>
</table>

Fig.3 shows the waveform of the output DC voltage. The output DC voltage is rapidly rising without overshoot and the static error is small.

Fig.4 shows the waveform of the AC-link voltage and current. The phase current vector is aligned with the phase voltage vector, so it achieves the unity power factor. And the harmonic spectrum of the line current is 2.73%.

The new strategy with ADRC is compared with the fuzzy PID controller. Fig.5 shows the waveform of the output DC voltage when the reference voltage is changed. The reference voltage is changed to 625V at the time 0.2s. From Fig.5, it is known the system with ADRC is more rapidly achieve to the steady than fuzzy PID.
Fig. 6 shows the waveform of the output voltage when load resistance is changed from 50Ω to 100Ω at the time 0.5s. Comparing with the fuzzy PID, the new method has smaller voltage-fall and rapidly renew-time.

Fig. 5 Control results when reference voltage changed

VI. CONCLUSION

The present ADRC voltage control scheme is proposed in PWM rectifier based on VO-DPC. ESO is used to observe the total disturbances. Then controlled and compensated them with ADRC, the effect caused by load change can be restrained available. Simulation results show that this new method can control the output voltage rapidly without overshoot. It achieves the unity power factor, furthermore, the effect caused by load change is restrained.

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BIOGRAPHY

Liao Xiaozhong was born in Guangdong, China, in 1962. She received her BSc and PhD degrees respectively from the Tianjin University in electrical and automation engineering and the Beijing Institute of Technology in control engineering. She is currently a professor in Beijing Institute of Technology. Her research interests are the electric drive system and energy converter control.
Control on Green Energy Source and Ecologic Environment

Jie Wu¹, Si-zhe Chen² and Jun-hua Yang³

Abstract – The development and utilization of control strategies are closely linked with progress and requirement of society. All sorts of renewable green energy sources and ecologic environment construction become more and more paid attention to, as fossil energy resources become shortage day by day as well as environmental pollutions. This paper researches and analyzes energy sources status and sustainable development problem. Some key control projects and strategies were raised through studying wind energy conversion system and solar PV system. As an example, a hybrid generation station was constructed for environmental protection, energy conservation and harmonious ecologic environment. CAN bus technology was applied to monitor and control the wind-solar PV hybrid electric station and greenhouse as well as energy management.

Keywords - Green energy source, ecologic environment, hybrid electric station

I. ENERGY SOURCES STATUS AND SUSTAINABLE DEVELOPMENT

Energy source is the basic element of human existence and is also the main material foundation for the development of the national economy. Energy security is fundamental to the economic security of our country.

With international industrialization, global energy consumption is expected to be a 3% growth rate in future. The depletion of conventional energy resources is the dilemma we are facing. On the mid-1970's, global energy resources faced crisis and oil prices dramatic rise. It stimulated those big countries with great energy consumption to put the research and development of alternative energy sources on an important position. A new round of global energy crisis is a profound impact on the economic, political and military relations among all countries. It is an example that USA army attacked Iraq, the major oil producing country in the Middle East, in 2003.

The rapid development of economy and the low efficiency of energy utilization made the energy status of China more severe. The growth rate of GDP was 9.1% in 2003, but 30% of energy and raw material of the world were consumed and our GDP is just 4% of the global production. The ecological environment will not endure if we only seek for the economic growth speed.

From the view of energy development strategy, human must seek the road to sustainable development of energy. With economic development and the improvement of living standard, there has been increasing emphasis on the improvements in the living conditions of human, and their awareness of environmental protection. Human urgently need some new energy sources which are clean, non-polluting and renewable. Developing and using renewable energy becomes a strategic choice. In fact, compared to coal, oil and other fossil fuel energy, some other energy such as water power, solar energy and wind power have much larger energy reserves. Theoretically, the solar energy that the entire earth absorbs in ten days exactly equals to all the world's energy reserves of fossil fuels [1]. The maximum utilization of the Earth's wind power is estimated to \(1.3 \times 1011\) kW. It is obviously much larger than the water power with \(2.9 \times 109\) kW. Statistics show that the useable wind energy can be four times larger than the total energy consumption in 1998 [2]. Meteorologists estimated that about 1% of the solar energy received by earth was converted to wind energy. According to relevant statistics of the 1980s, only 1% of wind energy (0.01% of solar energy) was able to meet the energy need of the globe [1,3]. It can be predicted that the energy structure of the 21st century will undergo fundamental change. The traditional energy with fossil fuels as the main energy will be replaced by solar energy, wind energy, biomass energy, nuclear fusion and other new energy. Currently, about 85% of 12 trillion watts of energy consumption come from fossil fuels. To slow global warming, in the middle of this century, global primary energy will reach the aim without carbon dioxide emission. And then alternative energy outputs are three times of the current global energy consumption. Recently, many countries are setting down their energy plan. The European Union has announced that regenerative energy utilization will account for 50% of the whole electrical power production until 2050.

After 1992, the Chinese government presented environment and development strategy, asking for developing and spreading clean energy such as solar energy, wind energy, geothermal energy, tidal energy, biomass and other clean energy according to local conditions. Chinese government formulated the wind power, solar energy development projects and programs, named ‘wind project’ and ‘bright project’ [4]. However, the development of renewable energy in China is very slow because of the insufficient fund investment. The production capacity of solar photovoltaic technology was just 4.5MW and the equipment capacity of wind power only was 567MW in China at the end of 2003 [5,6]. It is far behind developed countries. For instance, wind energy conversion equipment capacity was 14609MW in Germany. Therefore, the Commission of National Development and Reform proposed that by 2020, wind power capacity should reach to 30000MW, about 2% of the total installed capacity of power generation.

Digital ref: A170101006
1,2,3Electric Power College, South China University of Technology, Guangzhou 510641, China
The paper is first received in April 2007 and is an invited paper to the Journal
This century will be an era that renewable energy and new energy replace conventional energy to play the leading role. The International Energy Agency forecasts that the proportion of new and renewable sources of energy will be developed to constitute more than 50% of the world’s energy by 2060. Last four years, the global wind power generation has grown at an average annual rate of 65%, and the growth of solar energy is more than 30%, which even exceeded the development of the information technology industries.

II. WIND ENERGY CONVERSION SYSTEM AND CONTROL METHOD

In the numerous renewable energy and new energy technology development, wind power generation is the most mature, most large scale commercial development conditions and development prospects, the most competitive, the greatest potential. However, because of the intermittent and randomness of wind power, the quality of power was impacted greatly by the changes of wind speed and wind direction. The difficulty of the development of wind energy causes a number of particular problems to wind power technology and management systems, and makes wind power become a uncontrollable source. In fact, the power of wind energy conversion systems, if without control, does not have much commercial value. If it was directly put into the electric network, it will become pollution. In most cases, it can only contribute in harmonic, and it will affect the stability of the local power grid operation. In recent years, because of the rapid development and extensive application of technical control, power electronic technology and new materials technology, it creates favorable conditions for the use of wind power. In order to make wind power a high efficient, high quality and controllable energy, there are many control projects and control program of wind power, such as variable-pitch control (capturing maximum power), variable-speed constant-frequency control, yaw control, brake control and so on. However, two core issues needed to be solved are: the biggest wind energy power coefficient, variable-speed constant-frequency control, yaw control, brake control and so on. On the other hand, the control methods from the most simple PID to more complex modern control methods, such as intelligent control, optimal control, adaptive control, variable structure control, robust control, differential geometry and so on[2,8]. Figure 1 is based on the CAN bus control system block diagram of the wind farm.

A. Control of maximum power point tracking

According to the Betz theory of aerodynamics’ the output power of wind wheel is

\[ P_m = \frac{1}{2} \rho \pi C_p R^2 V^3 \]  

where, \(\rho\) is air density (kg/m\(^3\)), \(R\) is radius of wind wheel (m), \(V\) is wind speed (m/s) and \(C_p\) is wind energy power available coefficient.

We can know from this formula that: 1. If the wind speed is a constant, then \(P_m\) is in proportion to \(R^2\) (R is the radius of wind-wheel,) that is to say, for getting higher output power, the wind-wheel need the largest radius as possible, or say the largest area the wheel blade can get. But big size wind-wheel will make the increase of the cost and the difficulty of install of the wheel. 2. If the radius of wind-wheel \(R\) is a constant, \(P\) is in direct proportion to \(V^3\), so the wind generators should be installed in the areas with high wind speed, which relates to the environment. In the same position, the higher altitude, the higher wind speed will be, hence the tower-shelf should have a comparative altitude. 3. The wheel power is independent of the numbers of wheel lamina, but is in direct proportion to the air density. 4. The biggish wind energy power available coefficient \(C_p\), can improve the wheel power.

The available wind energy power coefficient \(C_p\), is not constant, its maximum is 0.593 theoretically. This value is also be defined by Betz-limit, it changes with the wind speed, the generator’s revolution and the blade parameters (the pitch angle for example), in generally,

\[ C_p = C_{p\text{m}} (\lambda = \frac{\omega R}{v}, \beta, \lambda) \]  

where, \(C_{p\text{m}}\) is wind energy power available coefficient, \(\omega\) is the Wind rotation angular velocity.

Figure 2 plots the relation curve between the wind energy utilization factor and \(\lambda\) . Usually, the wind energy utilization factor \(C_{p\text{m}}\)=0.2~0.5 in the horizontal axis, and in the vertical axis \(C_p\)=0.3~0.4.

![Fig. 1: Monitoring and control of wind turbine](image1)

![Fig. 2: Power coefficient](image2)
The overall design and operation strategy of the wind generator should ensure the safe of operation, in the meanwhile, to make \( C_p \) keep within the maximum during the operation area, to maximize the output power. We can know from formula (1) that, the output power of the wind generators is a cube function of the wind speed, that is to say, the bigger the wind speed, the higher the output power, but there are two limitations in the actual system: firstly, the maximum limitation of the electrical installations and electrical components, secondly, there is a rotate speed limit of the turbine components, especially the wind wheel. Thus, there are three typical run states: low wind speed phase operates in shift state, to maintain \( C_p \) be a constant value (to the extent possible, the best is to achieve the Betz limit), we can control the rotate speed of the generator according to the changes of the wind speed, to make \( \lambda \) unchanged until the rotate speed get to the limit. When rotate speed get to the limit, the wind speed increased further, control the operation at constant rotate speed until get to the maximum output power. At this point, \( C_p \) is not necessarily the maximum. When excess the rating speed, the output power gets to the limitation regulates the generators in constant output power. Figure 3 plots these three typical operating conditions. Figure 4 plots the control curve of maximum wind energy capturing.

B. Control of variable speed constant frequency generation

As we all know, the random wind, gust, and the uncertainty caused the frequency and voltage of the electric power from the wind power unit, this electric energy is lack of use except for the electric installations which have low-rise need for electric energy like heaters, we need to control and set the quality of the electric energy, the methods in common used are: constant speed constant frequency, variable speed constant frequency, variable frequency control. The VSCF control method can not only control the quality of the electric energy, and also can capture the wind energy furthest, the active and reactive power can be independently adjusted by decoupling control, and restrain harmonic, reduce the cost. The VSCF control projects we often use are: Asynchronous generator system, the exchange-fed generator excitation system, BDFM generator system, permanent magnet generator system. Because the electronic equipment of the double-fed electrical generator play the pole only in the control loop, equipment capacity generally should not exceed 30% of the power output of wind energy conversion system. The cost of equipment can be significantly reduced. Thus BDFM is a kind of wind energy conversion methods which have good prospect. BDFM, got rid of the slide loop and brush which can be easily attrited, improved the reliability of wind energy conversion system.

VSCF control can convert wind energy to alternating current which has constant frequency and constant voltage power. The wind turbine generator can be freely integrated into electric network.

The increasing depletion of fossil fuels, made the world's growing emphasis on the development and utilization of renewable energy. Various wind turbines emerge. Two major trends in the development of wind power generation systems: on the one hand, the development of greater capacity single large wind turbine generators, other developing distributed small and micro wind power generation system. Large-scale wind power equipment can reduce the cost of wind power generation, distributed small wind power generation system, which is designed to solve distributed remote areas scattered local power supply, can save the planning and construction of the supply networks which are hardly cost-effective.
III. CONTROL OF SOLAR PV STATION

A. Solar PV generations
The solar photovoltaic power generation is an important way for use of solar energy, and our country is focus on developing this green energy. Practically in China's western region, with a scattered population, and economic backwardness, many households without power and the use of solar energy has unique conditions. Along with the implementation of the western development policy and the "bright project", the implementation of solar photovoltaic technology has been rapidly developed. China's strong demand for photovoltaic products, PV batteries increased by 30% in average on sales. Until 2000, the retain of PV products got to 15MW, which are mainly used in telecommunications, railways, television, meteorology and navigation, cathodic protection, etc. Housing-use PV systems and independent photovoltaic power plant operators have made great progress. According to the solar energy resources developing plan made by the Development and Reform Commission, Ministry of Science and Technology, the development plan "Bright Project" plans to reach a total installed capacity of 300 MW photovoltaic power system in 2005, World Bank GEF project started in 2001, plans for the installation of 10 MW of photovoltaic power systems in rural areas in five years.

Solar energy generates electricity, including solar photovoltaic generators and large thermal electrical plants. Photovoltaic power generation has a conversion efficiency of about 10%~20%. It includes crystalline model and non-crystalline model. Crystalline model can be divided into single-crystal model and multi-crystalline model. About solar energy thermal electrical plants, trough solar power’s conversion efficiency can get to 15%, Spain will build the largest trough thermal electrical plants of Europe. Furthermore, there also have other forms, as for Tower power etc.

B. Control of solar PV station
(1) Sun tracking control, realize the maximum capture of solar energy’ power input.
(2) Maximum power output control of solar energy’ battery array (MPPT), we often uses the optimization algorithm.
(3) Solar inverter parallel and parallel control.
(4) Wind-solar PV system
This wind, solar control is the basic bottom module control, to constitute an optimal operation of wind-solar hybrid power systems. An upper energy management system is needed, and equipped with batteries. Figure 6 is a typical hybrid power system maps.

Fig. 6 Hybrid electric station

IV. CONTROL ON ECOLOGIC ENVIRONMENT

Research result indicates that 34% of the environment pollution is relate to construction industry, and 50% of the energy is used in the constructing and using of construction. Researching continuable ecotypic industry, including ecotypic house and greenhouse, is one of life aims of human being.

A. Control on ecologic environment
Using ecological principles, ecological balance and sustainable development and integrated follow optimal efficiency, controlled substances in the construction of energy conversion cycle of the system in an orderly manner, properly regulated to a small residential ecosystem, to get a highly efficient, low-consumption, low waste, alternative residential intelligent ecological environment, as illustrated in figure 7.

Specific measures:
1) Control of water recycling, rainwater collection system.
2) Develop the renewable energy: solar energy integration with the unified structures (building integration: BIPV), wind energy, natural temperature.
3) Use new power-saving, environmentally materials and indoor air quality monitoring.
4) Take full advantage of the characteristics of the climate and environment, farthest use the natural daylight and ventilation to reduce energy consumption.
5) Green and Waste disposal.

Fig. 7 A typical ecologic residence

B. Computer control system of greenhouse
Complete environmental control system of greenhouse including sensors, controllers and implementing agencies, generally using distributed computer control. The main functions of the control system are:

Throughout the vegetal process of crops, record the condition of indoor ecologial environment and control, to provide a basis for optimization Model of ecological environment.

1. According to the optimization model of ecological environment, make optimal control strategy.
2. According to the optimal control strategy, control heating, irrigation or ventilation.

2. According to the optimal control strategy, control heating, irrigation or ventilation.

\[ T^* = f(T_a, T_{p}, q_{s}, T_{e}) + g(T_a, u, Q, e, T_{e}) \]  

where, \( f \) is the part of certain parameters; \( g \) is the nonlinear part of time-varying parameters; \( T_a \) is the greenhouse air temperature; \( T_{p} \) is the heater temperature; \( q_{s} \) is the solar thermal radiation energy; \( T_{e} \) is the outdoor temperature; \( Q \) is the solar illumination angle; \( u \) is the outside wind.

C. Modelling and control of greenhouse

Greenhouse is one of the important signs of modern agriculture, modeling and control of the greenhouse environment began in the 1960s. The expression of greenhouse model is:

\[ T^* = f(T_a, T_{p}, q_{s}, T_{e}) + g(T_a, u, Q, e, T_{e}) \]  

C.1. Modelling methods of greenhouse

1. Based on the thermal energy balance modeling, mechanism analysis and system identification will be integrated to model.
2. Based on the expert system modeling and absorb the experience of agricultural experts.
3. Based on the fuzzy neural network modeling, genetic algorithm was used to train the network parameters.

C.2. Adaptive control system of greenhouse

Because of the outside environment factors such as radiation, or outdoor temperature, humidity, wind speed and so on. The greenhouse environment model parameters change. Conventional computer control cannot guarantee the control quality, more advanced control strategies are needed, such as the adaptive control. Fig. 9 is a typical adaptive control heating system of greenhouse.

D Control system of hybrid electric station and ecologic environment based on CAN bus

The technology of CAN bus is the amalgamation and integration of computer technology, network and communication technology and control technology. Using CAN bus for wind-solar energy hybrid electric station, greenhouse to monitor and energy manage, can make a environmentally, power-saving and harmonious ecological environment. As an example, the research center of renewable energy source of SCUT lays a 10kW solar battery array, there sets of dynamo (of a 1 kW horizontal axis, a 2kW vertical axis and a 2 kW horizontal axis) and the storage battery array on the roof, which together form a 15kW hybrid electric system. It also builds a 60m² greenhouse. The whole system use CAN bus technology, look at the Fig.10.
V. CONCLUSION

As conventional energy being exhausted, it is urgent to research, develop and utilize the green regenerative energy sources, which is represented by the wind energy and the solar energy. For example, in European Union with 15 member countries, its total target in 2010 is to make the utilization of green energy reach 22% among the total power production.

Based on the ecological theory, and following the principles of ecological balance, the sustainable development and the optimization of the system efficiency, the objective of the control is to make the substance energy sources be transformed orderly and circularly in the building system, also to construct the house to be a small ecological system, thus we can get an intellectualized and ecological resident environment with high efficiency, low-consumption, low-scrap and light pollution. This is just the requirement of the present time.

The new research subjects are coming forth endlessly with the development of green energy source and ecological environmental control.

REFERENCES


BIOGRAPHY

Jie Wu was born in Harbin in 1937. He received the B. Sc. Degree from Harbin Institute of Technology. He is a Professor in South China University of Technology, a Director in New Energy Research Center and editor in chief of an important journal named Control Theory & Application. He has published over 200 technical papers and book chapters. His research interest includes new energy, power electronics and control.
Dynamic Phasor Modelling of TCR based FACTS Devices for High Speed Power System Fast Transients Simulation

Zhijun E¹, K. W. Chan² and D. Z. Fang³

Abstract – This paper firstly proposes a generic dynamic phasor model of thyristor controlled reactor (TCR) at the device level. The modelling approach is based on the time-varying Fourier coefficient series of the power system variables. By truncating the less important higher order terms and keeping the significant ones, this dynamic phasor TCR model can realistically simulate the nonlinear characteristics of TCR with fast speed and high accuracy. The operation of anti-parallel-connected thyristor pair is simulated by a switching function. Based on this TCR dynamic phasor model, fast and efficient SVC and TCSC dynamic phasor models could then be implemented. While a simple power system was used for the device level evaluation, the 39-bus New England power system was built to fully verify the accuracy and efficiency of the propose dynamic phasor models by benchmarking with a commercial software named DCG-EMTP. The availability of fast and efficient dynamic phasor models for FACTS devices has provided a powerful basis for high speed power system fast transients simulation of large scale interconnected power systems.

Keywords - Dynamic phasors, thyristor-controlled reactor, thyristor-controlled series capacitor, static VAR compensator

I. INTRODUCTION

With the rapid development of power electronics technologies, more and more Flexible AC Transmission System (FACTS) devices have been widely adopted and applied in modern power systems for enhancing the controllability and power transfer capability of the AC system; and as a result, they play an important role in the power system operation and control. The static VAR compensators (SVCs) constitute the first generation of FACTS controller. It is shunt-connected static generator or absorber of reactive power in which the output is varied to maintain or control specific parameters of power system. Thyristor-controlled series capacitor (TCSC), on the other hand, is a series-controlled capacitive reactance that can provide continuous control of power on the AC line over a wide range. By now, SVC and TCSC are the most common FACTS devices used to improve the power system performance in steady-state and dynamic stability, voltage profile, and reactive power flow. For the stability assessment of large-scale power systems, it is necessary to model those FACTS device accurately and efficiently.

Because of the nonlinear switching behaviour of thyristor controlled reactor (TCR), accurate modelling of SVC or TCSC is non-trivial. The quasi-static approximation model commonly used in electromechanical transients (transient stability) simulation is not adequate to catch the dynamic behaviour of the switching. Even though in electromagnetic transient simulation, the full device level time-domain model can provide detailed response of the devices, the computation burden of such model is very demanding and hence is impractical for daily usage in large-scale power system simulations.

Dynamic phasor (DP) is developed from time-domain descriptions using the generalized averaging procedure [1-7], and can be used to establish nonlinear time-invariant and large-signal models of nonlinear devices. By now, HVDC system [8-9] and FACTS devices [10] such as SVC [11], TCSC [12-13], STATCOM [14] and UPFC [15-17] have been investigated and modelled using the dynamic phasor approach. However, the model of SVC in [11] and TCSC in [12] takes only the fundamental phasor into consideration for sub-synchronous resonance (SSR) study. In addition, simplified assumptions were taken in [13] to deduce the TCSC dynamic phasor model without the inclusion of the important self-governed control circuit.

In this paper, a generic dynamic phasor model of TCR is firstly proposed and evaluated. This model includes a switching function to simulate the operation of thyristor pair. By truncating the less important higher order frequency components and keeps only the lower order significant ones, the model of SVC and TCSC, which can accurately catch the dynamic behaviour of SVC and TCSC with fast simulation speed, are then implemented. Finally, the system level dynamic simulation of the 39-bus New England power system is implemented using the proposed dynamic phasor models. Balanced and unbalanced case studies on this 39-bus system show the validity of the proposed dynamic phasor models. The dynamic phasor models proposed in this paper can either be used in dynamic phasor (DP) simulation of modern power systems or incorporated in the traditional transient stability (TS) simulation to form a TS-DP hybrid simulation for transient stability study of large power system with accurate modelling of FACTS devices.

The rest of this paper is organized as follows. In Section II, the basic concept of dynamic phasor modelling approach is introduced. Section III presents the dynamic phasor models of TCR. Section IV provides the evaluation results of the proposed SVC and TCSC model on a simple power system. Section V shows the system level dynamic phasor simulation and Section VI concludes the paper.

II. BASIC CONCEPT OF DYNAMIC PHASORS

The approach of dynamic phasors is firstly known as the method of state-space averaging and is based on the time-varying Fourier coefficients. Generally, a complex time
domain waveform \( x(\tau) \) can be represented on the interval \( \tau \in (t-T,t] \) using a Fourier series of the form:

\[
x(\tau) = \text{Re}\{ \sum_{k=0}^{\infty} X_k(t)e^{jk\omega_s \tau} \}
\]

(1)

where \( \omega_s = 2\pi / T \) and \( X_k(t) \) are the complex time-varying Fourier coefficients called as dynamic phasors. The \( k \)th dynamic phasor at time \( t \) is determined by the following expression:

\[
X_k(t) = \frac{c}{T} \int_{t-T}^{t} x(\tau)e^{-jk\omega_s \tau} d\tau = (x^*)_k(t)
\]

(2)

where \( c = 1 \) if \( k = 0 \) and \( c = 2 \) if \( k > 0 \). The dynamic phasor method is based on the idea of frequency decomposition and focuses on the dynamics of the significant Fourier coefficient. The following are the two key and useful properties of the phasors:

1. **k-phasor differential characteristic:**

   For the \( k \)th Fourier coefficient, the differential with time satisfies the following formula:

   \[
   \frac{dX_k}{dt}(t) = \frac{d}{dt}(x^*)_k(t) - jk\omega_s X_k(t)
   \]

   (3)

2. **Product of dynamic phasors:**

   The \( k \)th phasor of a product of two time-domain waveform \( x(\tau) \) and \( y(\tau) \) can be obtained by the following operation:

   \[
   \langle xy \rangle_k = \sum_{i=0}^{k-1} \langle x \rangle_{i+k}, \langle y \rangle
   \]

   (4)

Also, the time domain waveform \( x(\tau) \) can be transformed back from its dynamic phasors by the following equation:

\[
x(\tau) = \text{Re}(X_k(t)e^{jk\omega_s \tau})
\]

\[
= X_k(t)e^{-jk\omega_s \tau} + X_{k-1}(t)e^{-j(1-k)\omega_s \tau} + \cdots
\]

\[
+ X_{k-1}(t)e^{j(1-k)\omega_s \tau} + X_k(t)e^{jk\omega_s \tau}
\]

(5)

Moreover, since \( x(\tau) \) is real, \( X_k = X_k^* \) where the operator \( * \) means the conjugate of a complex number.

### III. DYNAMIC PHASOR MODEL OF TCR

TCR is one of the most important building blocks of thyristor-based SVC and TCSC. Although it can be used alone, it is more often employed in conjunction with fixed or thyristor-switched capacitors to provide rapid and continuous control of reactive power over the entire selected lagging-to-leading range. As an example, the three-phase SVC shown in Fig. 1 consists of three delta-connected three-phase TCRs, shunt capacitors and filter circuits of odd harmonics.

![Fig. 1: Three-phase SVC circuit](image)

**A. Dynamic phasor model of TCR**

Fig. 2 depicts a single phase TCR. If the two thyristor valves are fired symmetrically in the positive and negative half-cycles of supply voltage, and thus only odd-order harmonics would be produced. Harmonics analysis shows that seventh and higher order harmonics has less effect on TCR dynamic characteristics [18]. As a result, in this paper only the fundamental, third and fifth harmonics would be considered in the dynamic phasor model of TCR.

![Fig. 2: Single phase circuit of TCR](image)

**From the single phase TCR circuit as shown in Fig. 2, its time-domain model can be obtained as:**

\[
\begin{align*}
C\frac{dI}{dt} &= i_i - i_s \\
L\frac{di}{dt} &= sv
\end{align*}
\]

(6)

where \( v = u_i - u_s \) and \( s \) is the switching function. When one thyristor is full conducting, \( s = 1 \); and when both thyristors are shut, \( s = 0 \). With \( < x >_i \) rewritten as \( X_i \), the dynamic phasor model of TCR can be obtained by the differential characteristic as the following formula:

\[
\begin{align*}
C\frac{dv_i}{dt} &= -jk\omega_s CV_i + I_v - I_s \\
L\frac{di}{dt} &= -jk\omega_s LI_i + <sv>_i
\end{align*}
\]

(7)

where \( <sv>_i = \sum_{i=5,3,1,3,5} S_i V_i \)

(8)

Dynamic phasors are complex quantities. Each equation in (7) consists of two parts: the real and imaginary parts; and as a result, the dynamic model of single phase TCR would have more equations than the corresponding time domain model. Nevertheless, it could catch the dynamic behaviour of TCR with relatively larger integration step time. The complete TCR dynamic phasor model is as follow:

\[
\begin{align*}
C\frac{dv_i^R}{dt} - k\omega_s CV_i^R &= I_v^R - I_s^R \\
C\frac{dv_i^I}{dt} + k\omega_s CV_i^I &= I_v^I - I_s^I
\end{align*}
\]


As an illustration for (9), the fundamental phasor model is presented as follow:

\[
<sv> = S_2 V_2 + S_3 V_3 + S_4 V_2 + S_5 V_2 + S_6 V_3 = S_1 V_1 + S_2 V_2 + S_3 V_3 + S_4 V_4 + S_5 V_5 + S_6 V_6
\]

\[
C \frac{dV_r}{dt} - \omega_C V_1 = I_r - I_1
\]

\[
C \frac{dV_i}{dt} + \omega_C V_1 = I_r - I_1
\]

\[
L \frac{dI_r}{dt} - \omega_c I_1 = S_1 V_2 + (S_2 V_2 + S_3 V_3 + S_4 V_4 + S_5 V_5)
\]

\[
L \frac{dI_i}{dt} + \omega_c I_1 = S_1 V_2 + (S_2 V_2 + S_3 V_3 + S_4 V_4 + S_5 V_5)
\]

(10)

where the superscript \( R \) and \( I \) denote the real and imaginary parts of the defined quantities.

**B. Dynamic phasor model of switching function**

The nonlinear operation of a TCR is simulated by a switching function. The dynamic model of the switching function [13] is a key element of dynamic phasor model of a TCR and can be described as follow:

\[
S_0 = \frac{1}{T} \int_{-\tau}^{\tau} s(\tau) \cdot d\tau = \frac{\tau - \alpha}{\pi}
\]

\[
S_m = \frac{1}{T} \int_{-\tau}^{\tau} s(\tau) \cdot e^{-im\tau} \cdot d\tau = \frac{j}{m\pi} \left[ e^{im\alpha} - e^{-im\alpha} \right]
\]

\[
= \frac{j}{m\pi} \left[ \sin m(\alpha - \sigma) - \sin m\alpha \right] + \frac{j}{m\pi} \left[ \cos m(\alpha + \sigma) - \cos m\alpha \right] \quad (m \neq 0)
\]

(11)

where, \( m \) is the sub-script of the \( m \)th phasor of switching function, \( \alpha \) is the firing angle and \( \sigma \) is conduction angle of TCR which depend on the closed-loop control of the SVC or TCSC. For each simulation time step, \( \alpha \) and \( \tau \) are calculated from control loop.

Because of the angle difference between phases, the switch function models for phase B and C are different from phase A and can be expressed as:

\[
\begin{align*}
S_{\alpha,B} &= e^{i(\alpha-2\pi/3)} S_{\alpha,A} \\
S_{\alpha,C} &= e^{i(2\pi/3)} S_{\alpha,A}
\end{align*}
\]

(12)

**C. Dynamic phasor model of controller circuit**

A practical model of the control system for the SVC and TCSC is essential for the proper representation of the system dynamic. A general SVC control system consists of a measurement system, a voltage regulator, a gate-pulse generator, a synchronizing system, and a supplementary control as shown in Fig. 3. The time-domain model of the controller circuit is shown in Fig. 4. In the dynamic model of SVC, the same voltage control unit is used. But the gate-pulse generator and synchronizing system is not included because only firing angle \( \alpha \) and conduction angle \( \tau \) are necessary for the dynamic phasor modelling work. The main difference is the calculation of \( V_{aux} \) is derived from the dynamic phasors of voltage instead of the instantaneous value. The same approach can also be applied in the modelling of the TCSC control system.

**D. Dynamic phasor model of filter circuit**

The filter circuit is also necessary for proper modelling of SVC or TCSC. In short, it is an RLC circuit which consists of one RL circuit and one capacitor circuit shown as Fig. 5. The dynamic phasor model of RL circuit and capacitor circuit is deduced as follows [19]:
1. DP model of RL circuit

For RL circuit, time-domain model is:

\[ v(t) = L \frac{di(t)}{dt} + Ri(t) \]  \hspace{1cm} (13)

and the dynamic phasors are obtained by

\[ L \frac{di_k}{dt} = V_k - jk\omega L I_k - RI_k, \quad k = 1, 3, 5 \]  \hspace{1cm} (14)

Then the complete dynamic phasor model becomes

\begin{align*}
L \frac{dI_k^R}{dt} &= (V_k^R - RI_k^R) + k\omega L I_k^I, \quad k = 1, 3, 5 \\
L \frac{dI_k^I}{dt} &= (V_k^I - RI_k^I) - k\omega L I_k^R
\end{align*} \hspace{1cm} (15)

2. DP model of capacitor circuit

For capacitor circuit, we have the time-domain model:

\[ i(t) = C \frac{dv(t)}{dt} \]  \hspace{1cm} (16)

and the dynamic phasors are obtained by

\[ C \frac{dV_k}{dt} = I_k - jk\omega CV_k, \quad k = 1, 3, 5 \]  \hspace{1cm} (17)

Then the complete dynamic phasor model becomes

\begin{align*}
C \frac{dV_k^R}{dt} &= I_k^R + k\omega CV_k^I, \quad k = 1, 3, 5 \\
C \frac{dV_k^I}{dt} &= I_k^I - k\omega CV_k^R
\end{align*} \hspace{1cm} (18)

IV. EVALUATION OF TCR MODEL

The TCR dynamic phasor model presented in this paper is evaluated via the modelling of the SVC and TCSC. For the evaluation of the dynamic phasor model, full DCG EMTP simulations for the entire test systems are carried out to produce the benchmark results for each case.

A. SVC DP model evaluation

In SVC, three single phase TCRs is connected in delta to prevent the triple harmonics from percolating into the transmission lines. As a result, in the SVC DP model, the third harmonics is not taken into consideration, and the term of third harmonics in the equations of other harmonics is also eliminated.

![Fig.6: The test system including SVC](image)

A simple test system shown in Fig. 6 is created to evaluate the performance of the dynamic phasor SVC model. The SVC circuit is powered by a constant current source. The impedance of the current source is 159.39+j48.86Ω. The capacity of the SVC is ±100MVar. The reference voltage of the test system is 230kV.

The evaluation includes four phases to cover all the SVC operating regions ranged from full conduction to close as detailed in Table 1. In total, the simulation lasts for two seconds. The emphasis of the comparison is placed on the waveforms of SVC bus voltage. The results of comparison are shown in Figs. 7-9.

<table>
<thead>
<tr>
<th>Phase</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>T (s)</td>
<td>0.5</td>
<td>1.0</td>
<td>1.5</td>
<td>2.0</td>
</tr>
<tr>
<td>M (A)</td>
<td>950</td>
<td>780</td>
<td>763</td>
<td>700</td>
</tr>
<tr>
<td>(\alpha) (°)</td>
<td>90</td>
<td>112</td>
<td>140</td>
<td>180</td>
</tr>
<tr>
<td>Region</td>
<td>Full</td>
<td>inducting</td>
<td>inductive</td>
<td>capacitive</td>
</tr>
</tbody>
</table>

Fig. 7 shows the phase A dynamic phasor voltage of the SVC bus with the instantaneous results obtained from the DCG-EMTP superimposed. It is clearly shown that the dynamic phasor voltage closely traces the envelop of the instantaneous voltage over the whole simulation period. This shows that the model including fundamental and fifth phasors is accurate enough to catch the dynamic response of SVC with faster simulation speed as shown in Table 2.

![Fig.7: SVC bus dynamic phasor voltage](image)

![Fig.8: Instantaneous SVC bus voltage – DCG EMTP](image)

![Fig.9: Instantaneous SVC bus voltage – dynamic phasor](image)
Fig. 8 and 9 show the comparison of instantaneous voltages between DCG EMTP and dynamic phasors. The instantaneous voltages of dynamic phasors are reversely transformed using equation (5). It is obviously that the dynamic phasor model has practically the same results as DCG EMTP software.

2. Efficiency evaluation

Various dynamic phasor models of SVC with different combinations of harmonics terms have also been built using the same modelling method. The run times for dynamic phasor simulations with different dynamic phasor models incorporated into the test system in Fig.5 are listed in Table 2. In Table 2, DP1 denotes the model only including fundamental phasor, DP1,5 denotes the model including fundamental and fifth phasors, and DP1,5,7 denotes the model including fundamental, fifth and seventh phasors. Comparing with full time-domain model, DP1 is fastest but least accurate model. DP1,5,7 is most accurate but most time demanding among the three dynamic phasor models. Overall, DP1,5 is the best compromise in term of accuracy and simulation efficiency.

<table>
<thead>
<tr>
<th>Model type</th>
<th>DP1</th>
<th>DP1,5</th>
<th>DP1,5,7</th>
<th>EMTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time consumed(s)</td>
<td>17</td>
<td>24</td>
<td>36</td>
<td>28</td>
</tr>
</tbody>
</table>

B. TCSC DP model evaluation

Different from the SVC DP model, TCSC DP model cannot ignore the effect of triplen harmonics because of the TCRs connection. So the third harmonics phasors have to be taken into consideration in TCSC dynamic phasor model. A simple test system similar to the previous one is used in the evaluation of TCSC DP model. The constant current source with same impedance is used as the power source in the TCSC circuit. The RMS of the current source is 1kA. The parameters of limped line are R=5.87Ω, L=134.20mH. The parameters of the TCSC are L=6.85mH, C=175μF. The evaluation includes three phases which lasts for 1.5 seconds in total. The simulation starts with firing angle \( \alpha = 60^\circ \) at \( t=0 \), then \( \alpha = 75^\circ \) at \( t=0.5s \), and the simulation end with \( \alpha = 85^\circ \) at \( t=1.5s \). The emphasis of the comparison is placed on the waveforms of capacitor voltage. The results of comparison are shown in Fig.10-12.

Fig. 10: The test system including TCSC

1. Accuracy evaluation

Fig. 11 shows the comparison of phase A capacitor voltage from the dynamic phasor simulation with the counterpart from the DCG EMTP instantaneous voltage. The comparison shows that the dynamic phasors can also trace the envelop of the instantaneous voltage over the whole three simulation phases. Fig. 12 and 13 show the comparison of instantaneous capacitor voltages waveform between DCG EMTP and dynamic phasors. It is clearly show that the dynamic phasor model, which includes the first and third phasors, has good accuracy and is able to capture the TCSC dynamic behaviour in transients with faster simulation speed as shown in Table 3.

![Fig. 11: Capacitor dynamic phasor voltage](image)

![Fig. 12: Instantaneous capacitor voltage – DCG EMTP](image)

![Fig. 13: Instantaneous capacitor voltage – dynamic phasor](image)

2. Efficiency evaluation

Several dynamic phasor models of TCSC with different harmonics considered are also implemented. Table 3 lists the simulation run times for the simple test system with different types of dynamic phasor models incorporated. In Table 3, DP1 denotes the model only including fundamental phasor, DP1,3 denotes the model including fundamental and third phasors, and DP1,3,5 denotes the model including fundamental, third and fifth phasors. Comparing with the dynamic phasor models of SVC, the dynamic phasor models of TCSC have the similar conclusion that DP1,3 is the best compromise in term of accuracy and simulation efficiency.

<table>
<thead>
<tr>
<th>Model type</th>
<th>DP1</th>
<th>DP1,3</th>
<th>DP1,3,5</th>
<th>EMTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time consumed(s)</td>
<td>18</td>
<td>25</td>
<td>38</td>
<td>32</td>
</tr>
</tbody>
</table>
V. Dynamic Phasor Simulation at System Level

Apart from evaluating the performance of the dynamic phasors at the device level modeling, the overall system dynamic performance is also considered. For the system level assessment, the 39-bus New England test system shown in Fig.14 is adopted. Again, the results obtained from the DP simulation are compared against with the benchmark results generated from the DCG EMTP.

In the EMTP simulation, generators and transmission lines are represented by two-axis generator models and distribution parameter line models, respectively. All loads are modeled as constant impedance. In the DP simulation, the dynamic phasor models of generators are derived from voltage flux-linkage equations directly and transmission lines are derived from distributed parameters model using the averaging approach. The step time of EMTP model is 50\(\mu\)s whereas the one for DP is 0.2ms. Two cases are performed and simulation comparison between DP and EMTP model is presented in the following sections.

A. Balanced fault case

In case 1, three phase to ground fault happens on bus 28 at 0.04s. The voltage of bus 26 is the focus of comparison. The results show in Fig.15.

From Fig.15-16, the waveforms of bus voltage using different models are generally matched each other while the ones from the DP simulation is relatively smoother with less high frequency transients. This is as expected since the time step adopted by the DP simulation is relatively larger and hence the simulation resolution (bandwidth) is lower while the simulation speed is higher. As indicated from Fig.15-16, DP simulation is indeed able to capture the dynamic characteristic of the system during the fault on and post-fault stage for both symmetry and asymmetry fault conditions.

Fig. 14: The 39-bus test system

In the EMTP simulation, generators and transmission lines are represented by two-axis generator models and distribution parameter line models, respectively. All loads are modeled as constant impedance. In the DP simulation, the dynamic phasor models of generators are derived from voltage flux-linkage equations directly and transmission lines are derived from distributed parameters model using the averaging approach. The step time of EMTP model is 50\(\mu\)s whereas the one for DP is 0.2ms. Two cases are performed and simulation comparison between DP and EMTP model is presented in the following sections.

B. Unbalanced fault case

In case 2, phase A to ground fault happens on bus 28 at 0.05s and then cleared at 0.07s. The voltage of bus 28 is the focus of comparison. The results show as Fig.16.

VI. Conclusion

A practical dynamic phasor model of TCR is proposed in this paper. The dynamic phasor modelling approach is developed from the time-domain descriptions using time-varying Fourier coefficients. This new model is then used in development of the SVC and TCSC dynamic phasor model which includes the effects of dominant harmonics and hence is more accurate than the conventional transient stability counterpart models. Without the simplifications as taken in transient stability simulation, dynamic phasor simulation is capable of catching the fast dynamics characteristics as the EMTP simulation while its simulation speed is much faster than the EMTP. The
newly developed models have been fully evaluated on a simple test power system with constant current source and the 39-bus New England test system for device and system level assessment, respectively. By benchmarking with the DCG EMTP software, it is clearly shown that the dynamic phasor models are accurate and efficient, and could be practically applied to large scale power system for accurate system dynamic modelling with extensive use of fast acting power electronics devices such as SVC, TCSC and HVDC, etc.

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BIOGRAPHIES

Zhijun E obtained Bachelor degree and master degree from Tianjin University, respectively in 2000 and 2005, and now is still studying at the Tianjin University for PhD degree. His research interests are in the areas of power system stability simulation and hybrid simulation, real-time power system simulation.

K. W. Chan received his B.Sc Hons. and Ph.D degrees in Electronic and Electrical Engineering from the University of Bath, UK. He is currently an assistant professor in the Department of Electrical Engineering, the Hong Kong Polytechnic University. His research interests are in the areas of power system stability and security assessment, real-time power system simulation, distributed and parallel processing.

D. Z. Fang received the M. Eng. Degree from Tianjin University, China in 1981 and Ph.D. degrees from The Hong Kong Polytechnic University in 1995. He joined the faculty of Tianjin University, China in 1981 and has been Professor there since 1999. His research interests are in power system analysis, transient stability control and optimization.
A Six-level SPWM Inverter for an Open-end Winding Induction Motor

K.Chandra Sekhar\textsuperscript{1} and G.Tulasi Ram Das\textsuperscript{2}

Abstract – A six-level inverter system for an open-end winding induction motor drive is presented in this paper. Multilevel inversion is achieved by feeding an open-end winding induction motor with a 3-level inverter from one end and a 2-level inverter from the other end of the motor. The 3-level inverter used in the proposed drive, is realized by cascading two 2-level inverters. The combined inverter system with open-end winding induction motor produces voltage space phasor levels identical to a conventional 6-level inverter. In the multilevel carrier based sinusoidal pulse width modulation (spwm), used for the proposed drive, a progressive discrete DC bias depending upon the speed range is given to the reference wave so that the drive can operate in the k-level modes (k = 2, 3, ... 6) depending on the speed range. The inverter with the higher DC-link voltage is switching less frequently, compared to the inverter with the lower DC-link voltage.

Keywords - Multilevel inverter, open-end winding induction motor, multilevel carrier based sinusoidal pulse width modulation

I. INTRODUCTION

Multilevel inverters have found increased relevance in the area of high power high voltage applications in the recent years since they were proposed in 1981[1][2][3]. The Multilevel inverters investigated for large induction motor drives fall under four general categories: the neutral-point clamped inverters, flying capacitor multilevel inverters, cascaded H-bridge inverters and open-end winding induction motor fed by dual inverters.

The neutral point clamped inverters experience neutral point fluctuations, as the DC-link capacitors have to carry the load current [4][5]. Flying capacitor topology is another scheme proposed for the multilevel inverters [6]. This structure does not require the neutral clamping diodes but needs as many capacitors as floating DC voltage sources. Higher number of levels is obtainable with series connected hybrid topology are more complex [7][8].

Dual inverter fed open-end winding induction motor drives also results in multilevel inverter structure [9][10]. A Dual inverter scheme with asymmetrical DC link voltages for the open-end winding induction motor is capable of producing a 4-level PWM waveform with reduced switching ripple for the motor phase voltage [11].

A multilevel system that is capable of realizing a PWM waveform ranging from 2-level to 5-level is described in [12]. In the topology described in [12], an asymmetrical 3-level inverter and a 2-level inverter feed an induction motor with open-end windings. The waveforms in [12] were obtained by switching the appropriate space vector combination using the look-up table. It is a formidable and cumbersome proposition to switch appropriate space vector combinations using look-up table approach. The three-level inverter in [13] is constituted by the cascade connection of two 2-level inverters with equal DC-link voltage.

In the present work, an inverter system to produce a multilevel PWM waveform ranging from 2-level to 6-level for the motor phase voltage for an open-end winding induction motor drive is proposed. In the proposed scheme, an open-end winding induction motor is fed with a symmetrical three-level inverter from one end and a two-level inverter from the other end. In the present work, symmetrical three-level inversion is obtained by connecting two 2-level inverters with equal DC-link voltage in cascade. The inverter scheme proposed in this paper produces voltage space phasor levels equivalent to a conventional 6-level inverter. This six-level inverter does not experience neutral point fluctuations and uses a lesser number of DC sources compared to the series H-bridge topology. A multilevel carrier based PWM is implemented for the drive where a progressive discrete DC bias is given to the reference wave depending upon the speed range. This results in a reduction of the switching ripple in the motor phase voltage waveform. This multilevel carrier based PWM eliminates the use of look-up approach to switch the appropriate space vector combination as in [12].

II. PROPOSED POWER CIRCUIT CONFIGURATION

The proposed power circuit topology to realize a multilevel phase voltage is shown in Fig.1. In this circuit configuration, an open-end winding induction motor is fed from a 3-level inverter (two 2-level inverters are connected in cascade-inverter-1 & inverter-2 of Fig.1) from one end and a two-level inverter (inverter-3 of Fig.1) from the other end of the motor. The DC-link voltages of inverter-1, inverter-2 and inverter-3 are (2/6)V_{dc}, (2/6)V_{dc} and (1/6)V_{dc} respectively, where V_{dc} is the DC-link voltage of an equivalent conventional single 2-level inverter drive. For inverter-2, let V_{A2n}, V_{B2n} and V_{C2n} represent the pole voltages of A, B and C phases respectively, referred to the point ‘O’ (Fig.1). The pole voltage, of any phase for inverter-2 for example V_{A2n} (Fig.1) attains a voltage of (2/6) V_{dc} if the following conditions are satisfied:

\begin{align*}
\frac{2}{6} V_{dc} & = \frac{2}{6} V_{A2n} + \frac{2}{6} V_{B2n} + \frac{2}{6} V_{C2n} \\
& \leq \frac{V_{dc}}{2} \\
\end{align*}

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\text{1Dept. of Electrical \\ & Electronics Engineering, R.V.R \\ & J.C College of \\ & Engineering, Chowdavaram, Guntur, -520 019(India).}

\text{2Dept. of Electrical Engineering, J.N.T.U \\ & College of Engineering, \\ & Kakapally, Hyderabad-500 072 (India).}

\text{email: cskoritala@hotmail.com , das_tulasiram@yahoo.co.in}

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The top switch of that leg in inverter-2, in this case $S_{21}$, is turned on (Fig.1).

The bottom switch of the corresponding leg in Inverter-1, in this case $S_{14}$, is turned on (Fig.1).

Similarly the pole voltage of any phase in inverter-2, for example $V_{A_2o}$, attains a voltage of $(4/6) V_{dc}$ if the following conditions are satisfied:

- The top switch of that leg in inverter-2, in this case $S_{21}$, is turned on (Fig.1).
- The top switch of the corresponding leg in inverter-1, in this case $S_{11}$, is turned on (Fig.1).

Thus, the DC-input points of individual phases of inverter-2 may be connected to a DC-link voltage of either $(4/6) V_{dc}$ or $(2/6) V_{dc}$ by turning on the top switch or the bottom switch of the corresponding phase leg in inverter-1. Additionally, the pole voltage of a given phase in inverter-2 attains a voltage of zero, if the bottom switch of the corresponding leg in inverter-2 is turned on. Thus, the pole voltage of a given phase for inverter-2 is capable of assuming one of the three possible values $0$, $(2/6) V_{dc}$ and $(4/6) V_{dc}$, which is the characteristic of a three level inverter. This configuration of 3-level inverter eliminates the neutral point fluctuations associated with the conventional neutral clamped 3-level inverter [1] as the capacitors $C_1$ and $C_2$ do not carry the load current but only the ripple currents. Also, the fast recovery neutral clamping diodes are eliminated in this topology of 3-level inverter. This 3-level inverter can be synthesized by reconnecting two existing 2-level inverters as a retrofit. The pole voltages of 2-level inverter ‘inverter-3’ ($V_{A_3O}$, $V_{B_3O}$, $V_{C_3O}$) assume one of the two values $0$ or $(1/6) V_{dc}$ depending on whether the top switch or the bottom switch of a given phase leg is turned on. When these inverters drive the induction motor from both sides each phase of the induction motor can attain six different levels. To find the equivalent levels when Three level inverter and two level inverter are switched independently, the points O and O’ are assumed to be connected. The different levels, generated for phase-A when Three level inverter and two level inverters are switched with different pole voltage levels are shown in Table-1.

It can be verified that all the other phases also can realize these six levels. It can be seen that the first two levels – $(1/6) V_{dc}$ and $0$ (L1, L2) are obtained when Three level inverter is clamped to zero while two level inverter is switched to $(1/6) V_{dc}$ and $0$. For the third and fourth levels (L3, L4) Three level inverter is clamped to its second level $(2/6) V_{dc}$ while two level inverter is switched to $(1/6) V_{dc}$ and $0$. For the fifth and sixth levels (L5, L6) Three level inverter can be clamped to third level $(4/6) V_{dc}$ while two level inverter is switched to $(1/6) V_{dc}$ and $0$. Hence the Three level inverter is switched less frequently as the inverter operates in all these levels.

It may be noted that when the bottom switch in a leg of the bottom inverters (inverter-2 or inverter-3) is ON, taking the machine winding end to O or O’, the top switch of top inverter in the same leg could be ON or OFF. But if the top switch of the top inverter (inverter-1) is also made ON, the top switch of the bottom inverter would have to block twice DC link voltage [i.e.$(4/6) V_{dc}$]. So whenever the bottom switch in any leg of the bottom inverter is ON, the top switch in the same leg of the top inverter is kept OFF. The condition to be forced on the top switches of the inverters to realize these 6-levels in the A-phase is shown in the Table-2. The state of the bottom switch is complementary to the condition of the top switch in the same leg. The bottom switches of the bottom inverter of
Three level inverter (inverter-2) have to be rated for \((4/6)V_{dc}\), as they will have to block \((4/6)V_{dc}\) when the top switches of inverter-1 and inverter-2 are switched on. The bottom switches of the bottom of two level inverter (inverter-3), have to be rated for \((1/6)V_{dc}\), as they will have to block \((1/6)V_{dc}\).

This six-level topology does not need the clamping diodes as in the case of neutral-point clamped inverters. The DC-link capacitors do not carry the load current and hence the neutral-point fluctuations are absent. When compared with the series-connected H-bridge, it uses the less number of switching devices and DC-sources. The five-level inverter configuration has further been improvised to yield a six-level operation would results in a better waveform with lower THD.

### Table 1: The levels realized in the A-phase winding when Three level inverter and Two level inverter are switched independently

<table>
<thead>
<tr>
<th>Pole-voltage of Three level inverter ((V_{A20}))</th>
<th>Pole-voltage of Two level Inverter ((V_{A20}, V_{A30}))</th>
<th>Motor phase voltage (V_{A2A3}=V_{A20} - V_{A30})</th>
<th>Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>((1/6)V_{dc})</td>
<td>(-(1/6)V_{dc})</td>
<td>L1</td>
</tr>
<tr>
<td>0</td>
<td>((1/6)V_{dc})</td>
<td>((1/6)V_{dc})</td>
<td>L2</td>
</tr>
<tr>
<td>((2/6)V_{dc})</td>
<td>((1/6)V_{dc})</td>
<td>((2/6)V_{dc})</td>
<td>L3</td>
</tr>
<tr>
<td>((2/6)V_{dc})</td>
<td>((2/6)V_{dc})</td>
<td>((3/6)V_{dc})</td>
<td>L4</td>
</tr>
<tr>
<td>((4/6)V_{dc})</td>
<td>((1/6)V_{dc})</td>
<td>((4/6)V_{dc})</td>
<td>L5</td>
</tr>
<tr>
<td>((4/6)V_{dc})</td>
<td>0</td>
<td>(0)</td>
<td>L6</td>
</tr>
</tbody>
</table>

### Table 2: The status of the switches in the inverters for each of six levels

<table>
<thead>
<tr>
<th>Level in A-phase</th>
<th>Status of the top switches of the 2-level Inverters (The bottom switches condition is complementary)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>(-V_{dc})</td>
</tr>
<tr>
<td>L2</td>
<td>0</td>
</tr>
<tr>
<td>L3</td>
<td>((1/6)V_{dc})</td>
</tr>
<tr>
<td>L4</td>
<td>((2/6)V_{dc})</td>
</tr>
<tr>
<td>L5</td>
<td>((3/6)V_{dc})</td>
</tr>
<tr>
<td>L6</td>
<td>((4/6)V_{dc})</td>
</tr>
</tbody>
</table>

### III. VOLTAGE SPACE PHASORS OF PROPOSED SCHEME

The combined effect of three voltages in the three 120 degree separated phase winding of the induction motor at any instant, could be represented by an equivalent vector in space. This space vector \(V_s\), for the dual inverter scheme is given by

\[
V_s = V_{A2A3} + V_{B2B3} e^{j(2\pi/3)} + V_{C2C3} e^{j(4\pi/3)}.
\]

Substituting expressions for the phase voltages in the above equation gives

\[
V_s = (V_{A20} - V_{A30}) e^{j(2\pi/3)} + (V_{B20} - V_{B30}) e^{j(4\pi/3)} + (V_{C20} - V_{C30}) e^{j(0)}.
\]

This equivalent vector can be determined by resolving the phase voltages along two mutually perpendicular axes, \(\alpha-\beta\) axes of which \(\alpha\) is along the A-phase(Fig.2). The space vector is then given by

\[
V_s = V_s(\alpha) + jV_s(\beta) = \begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix}.
\]

Where \(V_s(\alpha)\) is the sum of all components of \(V_{A2A3}, V_{B2B3}\) and \(V_{C2C3}\) along the \(\alpha\) axis and \(V_s(\beta)\) is the sum of the components \(V_{A2A3}, V_{B2B3}\) and \(V_{C2C3}\) along the \(\beta\) axis. The voltage components \(V_s(\alpha)\) and \(V_s(\beta)\) can be thus obtained by the following transformation

\[
V_s = \begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ \sqrt{3}/2 & -\sqrt{3}/2 & 0 \end{bmatrix} \begin{bmatrix} V_{A20} - V_{A30} \\ V_{B20} - V_{B30} \\ V_{C20} - V_{C30} \end{bmatrix}
\]

Substituting expressions for the phase voltages in the above equation gives

\[
V_s = \begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ \sqrt{3}/2 & -\sqrt{3}/2 & 0 \end{bmatrix} \begin{bmatrix} V_{A20} - V_{A30} \\ V_{B20} - V_{B30} \\ V_{C20} - V_{C30} \end{bmatrix}.
\]

The inverters can take different levels of pole voltages independently in the three phases depending upon the condition of the inverter switches and for each of the different combination of their pole voltages, \(V_{A20}, V_{B20}\) and \(V_{C20}\) for the Three level inverter and \(V_{A30}, V_{B30}\) and \(V_{C30}\) for the two level inverter. The equivalent voltage space phasor \(V_s\) can be determined using equations (3) and (7). All the space phasors can be determined for all the possible combinations of the pole voltages of the two inverters. They will occupy different locations as shown in Fig.3, where the location marked ‘1’ is the location of the zero amplitude space vector. When compared with five-level inverter the space phasor locations are enhanced to 91 from 61 and the sectors are enhanced to 150 from 91 in the space vector point of view. The maximum amplitude of the space phasor generated can be verified to be \(V_{dc}\).
A. Effect of Common-Mode Voltage in Space Phasor Locations

In the above analysis for deriving the different levels and the space phasor locations, the points O and O’ were assumed to be connected. When these points are not connected (as in the proposed drive Fig.1), the actual phase voltages are

\[ V_{A2A3} = V_{A2O} - V_{A3O'} - V_{O'O} \]  
\[ V_{B2B3} = V_{B2O} - V_{B3O'} - V_{O'O} \]  
\[ V_{C2C3} = V_{C2O} - V_{C3O'} - V_{O'O} \]  

\[ V_{O'O} \] corresponds to the common-mode voltage present in this balanced three-phase system and is given by

\[ V_{O'O} = \frac{1}{3} (V_{A2O} + V_{B2O} + V_{C2O}) - \frac{1}{3} (V_{A3O'} + V_{B3O'} + V_{C3O'}) \]  

Substituting these expressions for the phase voltages in (1)

\[ V_s = (V_{A2O} - V_{A3O'} - V_{O'O}) + (V_{B2O} - V_{B3O'} - V_{O'O}) e^{j(2\pi/3)} + (V_{C2O} - V_{C3O'} - V_{O'O}) e^{j(4\pi/3)} \]

\[ = (V_{A2O} - V_{A3O'}) + (V_{B2O} - V_{B3O'}) e^{j(2\pi/3)} + (V_{C2O} - V_{C3O'}) e^{j(4\pi/3)} - (V_{O'O} + V_{O'O} e^{j(2\pi/3)} + V_{O'O} e^{j(4\pi/3)})\]

In this equation

\[ (V_{O'O} + V_{O'O} e^{j(2\pi/3)} + V_{O'O} e^{j(4\pi/3)}) = 0 \]

and the equation then reduces to

\[ V_s = (V_{A2O} - V_{A3O'}) + (V_{B2O} - V_{B3O'}) e^{j(2\pi/3)} + (V_{C2O} - V_{C3O'}) e^{j(4\pi/3)} \]

This equation is the same as that derived earlier (2), assuming that points O and O’ were connected. Hence the above analysis shows that the common-mode present between points O and O’ does not change the space phasor locations. This common-mode voltage will result only in the multiplicity of space phasors in different locations, and the system with isolated O and O’ points generates the same voltage-space phasors.

IV. MODULATION SCHEME FOR THE PROPOSED INVERTER

Multilevel carrier based SPWM is used for the proposed inverter scheme. The multilevel carrier based PWM for an N-level inverter uses a set of N-1 adjacent level shifted triangular carrier waves with the amplitude and frequency [14]. If reference wave has peak amplitude \( V_m \) and frequency \( f_m \), the modulation index is defined with reference to a triangular wave of peak-to-peak amplitude of \( V_C(N-1) \) as

\[ M_a = \frac{2V_m}{V_C(N-1)} \]  

For the 6-level inverter drive structure, 5 triangular waves C1 to C5, with peak-to-peak amplitude of \( V_C \) are used, as shown in Fig.4a. The peak-to-peak amplitude of each carrier is \( V_C = (1/6)V_{max} \) where \( V_{max} \) is the maximum value possible for the modulating signal. These five carriers divide the entire range of modulating signal to six regions R1 to R6, R1 being the region below the lowest carrier C1 and R6 the region above the highest carrier C5. The regions between these two carriers are referred as R2 to R5. When the modulating signal is in a particular region a corresponding voltage level is applied across the motor phase winding as assigned below:

\[ R1 = > (1/6)V_{dc}; R2 = > 0; R3 = > (1/6)V_{dc}; \]
\[ R4 = > (2/6)V_{dc}; R5 = > (3/6)V_{dc}; R6 = > (4/6)V_{dc}; \]

Three 120 degree phase shifted sinusoids with 20% third harmonics content are used as the reference waves for the proposed carrier based SPWM. The addition of third harmonic content increases the maximum fundamental voltage amplitude that can be generated using the SPWM scheme [15].

These reference waves are continuously compared with
the carrier set to determine the region (R1, R2...R6) in which the instantaneous value of the reference wave exists. This comparison is performed simultaneously for all the three phases. Control signals for the two inverters then can be generated such that the appropriate devices are switched to realize the particular level in a particular phase depending upon the region. It may be noted that the proposed inverter can realize the even numbered levels also, and can start with the 2-level operation and progressively move to the 3-level, 4-level, 5-level and to the 6-level operation as the modulation index increases.

For low modulation index such that \( V_m \leq V_c / 2 \) where \( V_m \) is the peak value of the modulating signal, in conventional SPWM the reference waves are placed at the center of the carrier set (Fig. 4a). This will result in a 4-level operation as the modulating signal at different instants could be in one of the four regions R2, R3, R4 or R5. To realize the four levels associated with these regions (13), both inverters

Three level inverter and two level inverter would be switching (Table-2). Now if the reference wave is placed at the middle of the lowest carrier C1 as Fig. 4b, the modulating signal exists only in two regions R1 or R2 and it will result in only two levels L1 (-1/6 \( V_{dc} \)) and L2 (0). In this case the switching losses are only due to two level inverter.

When the modulating index increases such that \( V_c / 2 \leq V_m \leq V_c \), an additional DC bias of \( V_c / 2 \) is given to the reference wave such that it is at the middle of the two lower carriers C1 and C2 and results in 3-level operation (Fig. 4c). A similar progressive DC shift in steps \( V_c / 2 \) of is gives such that the inverter progressively moves through the 3-level, 4-level, 5-level and to 6-level operation (Fig. 4d, Fig. 4e & Fig. 4f).

When the V/f control is used, these 5 ranges of voltage amplitudes correspond to 5 ranges in frequency. Therefore the range (denoted by \( n = 1, 2, \ldots 5 \)) in which the frequency command falls can be used to determine the DC shift to be given to the reference waves and the reference waveforms can be represented by,

\[
V_a^* = V_m \sin(\omega t) + 0.2 V_m \sin 3 \omega t + n V_c / 2, \tag{14}
\]
\[
V_b^* = V_m \sin((\omega t - 2\pi/3)) + 0.2 V_m \sin 3 \omega t + n V_c / 2, \tag{15}
\]
\[
V_c^* = V_m \sin((\omega t - 4\pi/3)) + 0.2 V_m \sin 3 \omega t + n V_c / 2. \tag{16}
\]

When this SPWM scheme is employed, Three level inverter is clamped to zero level and two level inverter is switched in two level mode to create the first two levels (L1, L2), then Three level inverter is clamped to second level (2/6)\( V_{dc} \) and two level inverter is switched in 2-level mode to create the next two levels (L3, L4) and finally Three level inverter is clamped to its third level (4/6)\( V_{dc} \) and two level inverter is switched in 2-level mode to create the last two levels (L5, L6). This results in the inverters, which has the higher DC bus voltage switching less frequently compared to two inverters.
means that the DC-bus voltage of an equivalent conventional 2-level inverter is $V_{dc}$. The speed reference is translated to the frequency and voltage commands maintaining V/f. Depending upon the range in which the frequency command falls the reference waves are generated according to Eqn. (14), (15) and (16). The three reference waves are simultaneously compared with the carrier set and the level at which the instantaneous value of the reference wave is determined.

A DC-bus voltage ($V_{dc}$) of 600 volts is assumed for simulation studies. A load torque of 10 N-m is applied at 0.5sec. Fig.6 shows the motor phase voltage in the lowest speed range and it may be noted that the inverter is operating in the 2-level mode. In this case, inverter-3, being a two level inverter is switched between $(1/6)V_{dc}$ and 0 while the three level inverter (constituted by the cascade connection of inverter-1 and inverter-2) is clamped to zero. Fig.7 shows the motor phase voltage $V_{A2A3}$, in the next speed range in 3-level operation with the three level inverter is now in the 2-level mode, switching between zero and $(2/6)V_{dc}$ while two level inverter (i.e. inverter-3) switches. Fig.8 shows the motor phase voltage in the next speed range in the 4-level operation, where three level inverter switching in the 2-level mode between zero and $(2/6)V_{dc}$ and two level inverter switched between $(1/6)V_{dc}$ and 0. Fig.9 shows the motor phase voltage for the 5-level operation, in which the three level inverter enters into the three level operation switching between 0, $(2/6)V_{dc}$ and $(4/6)V_{dc}$ while the two level inverter switched. Fig.10 shows the motor phase voltage in the 6-level operation in which the Three level inverter switching in the 3-level mode between zero and $(4/6)V_{dc}$ and the two level inverter switched in the 2-level mode.

It can be seen that the motor phase voltage during 6-level operation is very smooth and close to the sinusoid with lower THD. Fig.11a to Fig.11e show the phase voltage, transient phase current, steady state phase current, torque and speed of the motor during six-level operation. Fig.12a to Fig.12e show the normalized harmonic spectrum of the motor phase voltage at different levels of operation. Fig.13 shows the decrease of total harmonic distortion (%THD) in the motor phase voltage as the number of levels increased.
Fig. 6: Motor phase voltage and its fundamental waveform during 2-level operation

Fig. 7: Motor phase voltage and its fundamental waveform during 3-level operation

Fig. 8: Motor phase voltage and its fundamental waveform during 4-level operation

Fig. 9: Motor phase voltage and its fundamental waveform during 5-level operation

Fig. 10: Motor phase voltage and its fundamental waveform during 6-level operation

Fig. 11a: Motor phase voltage during 6-level operation (with more number of cycles)

Fig. 11b: Transient motor phase current during 6-level operation

Fig. 11c: Steady state Motor phase current during 6-level operation
Fig. 11d: Motor torque during 6-level operation

Fig. 11e: Motor speed during 6-level operation

Fig. 12 (a): Normalized harmonic spectrum for the motor phase voltage during 2-level operation

Fig. 12 (b): Normalized harmonic spectrum for the motor phase voltage during 3-level operation

Fig. 12 (c): Normalized harmonic spectrum for the motor phase voltage during 4-level operation

Fig. 12 (d): Normalized harmonic spectrum for the motor phase voltage during 5-level operation

Fig. 12 (e): Normalized harmonic spectrum for the motor phase voltage during 6-level operation

Fig. 13: Total harmonic distortion (%THD) of the motor phase voltage as the number of levels increased
VI. CONCLUSION

An open-end winding induction motor fed by a 3-level inverter from one end and a 2-level inverter from the other end of the motor results in voltage space phasor locations identical to a conventional 6-level inverter. The Three level inverter used is realized by cascading two 2-level inverters. When compared with the cascaded H-bridge topology the present scheme employs a lower number of power supplies and switching devices. The proposed inverter does not experience neutral-point fluctuations and the DC-link capacitors carry only the ripple current as isolated DC supplies are used for all the DC links. When compared with the five-level inverter the switching ripple and THD in the motor phase voltage of proposed inverter is reduced. Multilevel carrier based SPWM, where a progressive discrete DC shift is added to reference wave depending on the speed range, allowing operation in all levels (2-level to 6-level) is employed for the proposed work.

The phase current is also near to sinusoidal and contains low THD. The motor torque reached steady state and responded for a change of load at 0.5 sec. The corresponding speed response is also presented and the speed reached the steady state. The motor exhibits good dynamic response. The phase voltage of six-level operation contains lowest harmonics when compared to that of two-level to five-level operation. As the number of levels increased the %THD in the motor phase voltage decreased.

REFERENCES


BIOGRAPHIES

K.Chandra Sekhar received his B.Tech degree in Electrical & Electronics Engineering from V.R.Siddartha Engineering College, Vijayawada, India in 1991 and M.Tech with Electrical Machines & Industrial Drives from Regional Engineering College, Warangal, India in 1994. From 1994 to 1995, he was the Design & Testing Engineer in Maitreya Electricals (P) Ltd. Vijayawada. From 1995 to 2000, he worked with Koneru Lakshmaiah College of Engineering as a Lecturer, since 2000, he has been with R.V.R & J.C.College of engineering as Assistant Professor. Presently he is a part-time research student at J.N.T.U College of Engineering, Hyderabad- 500072, India, working towards his doctoral degree.

G.Tulasi Ram Das received his B.Tech degree in Electrical & Electronics Engineering from J.N.T.U college of Engineering, Hyderabad, India in 1983 and M.E with Industrial Drives & Control from O.U College of Engineering, Hyderabad, in 1986. He received the PhD, degree from the Indian Institute of Technology, Madras, India in 1996. He is having 20 years of teaching and research experience. He is currently Principal J.N.T.U College of Engineering, Hyderabad- 500 072, India. His Research interests are FACTS Devices.
Modeling and Simulation of Self-Tuning PI Control for Electrical Machines

Ziqian Liu

Abstract – This paper presents the work of modeling and simulation of a self-tuning PI control for induction motors. A mathematical model of a three-phase induction motor, together with its self-tuning PI controller will be illustrated. By using the computer simulation, it has been found that the proposed design approach is robust to the variations of induction motor parameters and it achieves the performance of global asymptotic speed tracking.

Keywords - Modeling and simulation, self-tuning PI control, indirect vector control, induction motor

I. INTRODUCTION

The conventional proportional-integral (PI) control remains the most popular design approach used in industrial applications due to its simplicity and reliability for the control of first and second order plants, and even high order plants with well-defined conditions. A well-tuned PI controller is capable in achieving an excellent performance. However, it suffers a crucial disadvantage of getting a poor performance whenever the plant is subjected to some kind of disturbance or, the plant has high order nonlinear structure. Induction motor is a prime choice of variable-speed drive in a wide range of applications due to its low cost, reliability, and ruggedness. Because of the highly coupled non-linearity and the variations of internal parameters, the tuning of PI controller becomes a challenging problem when the conventional PI design is applied to the control problem of induction motors [1], [2]. In order to deal with this problem, self-tuning PI control for induction motor drive has received considerable attention in the literature [3], [4], and [5]. In this paper, we have adopted a self-tuning PI control which has been developed in [6]. Consequently, the PI control gains in this design are automatically adjusted online. Therefore, this makes our controller being robust to the changes of induction motor parameters.

Modeling and simulation is usually used in designing a motor drive in order to avoid building a system prototype due to the high expense. If all components are correctly selected, the simulation process could demonstrate both the steady state and the dynamic performance that would have been obtained if the drive was actually needed. This practice saves time, and reduces the cost of building a prototype, and most importantly it ensures that the requirements are being achieved.

Furthermore, simulation-based design plays an important role in understanding and evaluating induction motor drives. Recently, the work of modeling and simulation by using Matlab/Simulink has been widely used in the field of industrial drives. Along this way, we developed an entire simulation program for the whole system and also created several unique modules to replace the existing ones in Matlab/Simulink. For example, in order to visualize clearly the relationship between internal parameters and system performances, all of the differential equations have been embedded into the models of electrical machines. The theoretical derivation, modeling work, and simulation results will be illustrated as follows.

II. THE PRINCIPLE OF INDUCTION MOTOR MODELING WITH INDIRECT VECTOR CURRENT CONTROL

Given several assumptions ([7] and [8]), the dynamical model of an induction motor in a fixed reference frame attached to the stator can be described as follows:

\[
\frac{d\omega}{dt} = \frac{M}{J_L} (\psi_a b - \psi_b a) - \frac{T_i}{J} \tag{1}
\]

\[
\frac{d\psi_a}{dt} = -\frac{R_a}{L_r} \psi_a - \omega \psi_b + \frac{R_a}{L_r} M a \tag{2}
\]

\[
\frac{d\psi_b}{dt} = -\frac{R_b}{L_r} \psi_b + \omega \psi_a + \frac{R_b}{L_r} M b \tag{3}
\]

\[
\frac{di_a}{dt} = \frac{M R_r}{(L_r L_s - M^2) L_r} \psi_a + \frac{M}{L_r L_s - M^2} \omega \psi_b \tag{4}
\]

\[
\frac{di_b}{dt} = \frac{M R_r}{(L_r L_s - M^2) L_r} \psi_b - \frac{M}{L_r L_s - M^2} \omega \psi_a \\
- \frac{M^2 R_r + L_r^2 R_s}{(L_r L_s - M^2) L_r} i_b + \frac{L_r}{L_r L_s - M^2} u_b \tag{5}
\]

where: rotor speed \( \omega_r \), rotor fluxes \((\psi_a, \psi_b)\), and stator currents \((i_a, i_b)\) are state variables. rotor inertia \(J\), stator and rotor inductances \((L_s, L_r)\), mutual inductance \(M\), stator and rotor resistances \((R_s, R_r)\) are system parameters.

Control inputs are stator voltages \((u_a, u_b)\).

For the purpose of current control of induction motor using the technique of rotor-flux-oriented vector control, the model of induction motor can be represented on d-q rotating axis, where the d-axis is aligned with the rotor flux at all time and the q-axis is always 90\(^\circ\) ahead of the d-axis. Therefore, we take new variables similar to [9] and [10] as follows.

\[
\begin{bmatrix}
\psi_d \\
\psi_q
\end{bmatrix} = \begin{bmatrix}
\cos \varphi & \sin \varphi \\
-\sin \varphi & \cos \varphi
\end{bmatrix} \begin{bmatrix}
\psi_a \\
\psi_b
\end{bmatrix} \tag{6}
\]
variables on left side represent the components of rotor fluxes, stator currents and stator voltage vectors, respectively, with respect to the d-q rotating axis at speed \( \omega \) and identified by the angle \( \varphi \). In the new state variables \((\omega, \psi_d, \psi_q, i_d, i_q)\) and new control inputs \((u_d, u_q)\), the motor dynamics become:

\[
\begin{align*}
\frac{d\omega}{dt} &= \frac{M}{J}\left(\psi_d i_q - \psi_q i_d\right) - \frac{T_L}{J} \\
\frac{d\psi_d}{dt} &= \frac{R_s M}{L_r} i_d - \frac{R_s}{L_r} \psi_d + \left(\omega_e - \omega\right) \psi_q \\
\frac{d\psi_q}{dt} &= \frac{R_s M}{L_r} i_q - \frac{R_s}{L_r} \psi_q - \left(\omega_e - \omega\right) \psi_d
\end{align*}
\]

(7) (8)

When the current-controlled PWM inverter is applied, the model can be reduced to a third-order system, which is widely used in the induction motor control design ([11], [12], and [13]).

\[
\begin{align*}
\frac{d\omega}{dt} &= \frac{M}{J}\left(\psi_d i_q - \psi_q i_d\right) - \frac{T_L}{J} \\
\frac{d\psi_d}{dt} &= \frac{R_s M}{L_r} i_d - \frac{R_s}{L_r} \psi_d + \left(\omega_e - \omega\right) \psi_q \\
\frac{d\psi_q}{dt} &= \frac{R_s M}{L_r} i_q - \frac{R_s}{L_r} \psi_q - \left(\omega_e - \omega\right) \psi_d
\end{align*}
\]

(9) (10) (11)

According to the rotor-flux-oriented vector control ([14] and [15]), the rotor flux is aligned with the \( d \) axis and kept at a constant so that we have the following relations in steady state:

\[
\begin{align*}
\psi_d &= \psi_q = 0 \\
\psi_r &= \text{const.}
\end{align*}
\]

(17) (18)

Applying (17) and (18) into (15) and (16), we can get the slip frequency and the flux current in steady state

\[
\begin{align*}
\omega_s &= \omega_e - \omega = \frac{R_s M}{L_r \psi_r} i_q - \frac{M}{T_p \psi_r} i_q \\
i_d &= \frac{\psi^*}{M}
\end{align*}
\]

(19) (20)

The vector control technique shown above guarantees that the transient terms vanish in short time. Therefore, the steady state equations are sufficient for the derivation of speed control design. The control objective now is to design a speed controller so that \( \omega \) tracks \( \omega^* \). As a consequence, Fig. 1, in which \( K_T = \frac{M \psi^*}{L_r} \), shows the block diagram of speed control design.

III. SELF-TUNING PI CONTROL DESIGN

Due to its simplicity and reliability, the conventional PI control remains the most popular method used in motor control. However, since the variation and the high uncertainty of induction motor internal parameters, the tuning of PI control gains becomes a challenging problem. In this study, we apply the concept that has been presented in [6] to develop a self-tuning PI control and eliminate any dependence on the control model of induction motor. First, we divide the whole system into three parts as shown in Fig. 2, which is similar to the one given in [16]. Part 1 is the proportional part with the exception of proportional gain \( K_P \). Part 2 is the integral part with the exception of integral gain \( K_I \). Part 3 is the control plant. Then we consider \( K_P \) and \( K_I \) as independent variables. Based on the principle of gradient descent optimization, we construct a cost function as

\[
E = \frac{1}{2} e^2 = \frac{1}{2} \left( \omega^* - \omega \right)^2
\]

(21)

Using the algorithm of gradient descent

\[
\dot{K} = -\eta \frac{dE}{dK}, \quad K = \{ K_P, K_I \}
\]

(22)

and following the derivative of chain rule, we can obtain the following tuning algorithm

\[
\begin{align*}
\dot{K}_P &= \eta \psi_y 1 \\
\dot{K}_I &= \eta \psi_y 2
\end{align*}
\]

(23)

where \( \eta \) is an adaptive coefficient.

IV. SIMULATION RESULTS

In order to evaluate and validate the effectiveness of our proposed control design presented in the previous sections, a simulation program has been developed by using Matlab/ Simulink. Fig. 3 shows the block diagram of the entire motor drive system. The module of the simulation program is shown in Fig. 4. Fig. 5 shows the model of induction motor. The specifications for the induction motor are [17]: motor power = 15kW (rated), load torque = 70Nm (rated), rotor flux linkage = 1.3Wb (rated), angular speed = 220 rad/s (rated), \( n = 1, J = 0.0586kgm^2, R_s = 0.18\Omega, L_s = 0.0699H, M = 0.068H, R_P = 0.15\Omega, L_r = 0.0699H \). In our simulation, we take the change of rotor resistance as \( R_s(t) = R_s^*(2 - \exp(-at)) \) in which \( a = 2 \) and give different load torques.

Let us see the dynamic behaviors of induction motor from the results of Fig. 6 when the motor runs in four quadrants. Fig. 6(a) shows that the motor runs without load. Fig. 6(b) presents that the motor runs with 100% load. In Fig. 6, one can see that the control system of induction motor achieves a good tracking performance.
Fig. 1: Speed control design for induction motor with rotor-flux-oriented vector control

Fig. 2: The design of self-tuning PI for induction motor

Fig. 3: The whole block diagram of the induction motor drive system

Fig. 4: Matlab/Simulink model of the induction motor drive system
Five Dynamical Differential Equations of Induction Motor

Fig. 5: Simulink model of an induction motor

Fig. 6: (a) Speed response in four quadrants without load.
(b) Speed response in four quadrants with 100% load
V. CONCLUSION

The work of modeling and simulation of an entire induction motor drive system controlled by a self-tuning PI controller has been presented in this paper. In addition a novel detailed Simulink model for induction motor has been illustrated, which allows us to clearly visualize the relationship between the internal parameters and the system performances. By using the computer simulation, it has been found that the proposed design approach is robust to the variations of induction motor parameters and achieves the performance of global asymptotic speed tracking.

REFERENCES


Enhanced Direct Torque Control Using a Three-Level Voltage Source Inverter

R. Zaimeddine¹, E.M. Berkouk²

Abstract – The objective of this paper is to study a new control structure for the sensorless induction machine dedicated to electrical drives by using a three-level voltage source inverter (VSI). The output voltages of the three-level VSI can be represented by four groups: the zero voltage vectors, the small voltage vectors, the middle voltage vectors and the large voltage vectors in (d, q) plane. The amplitude and the rotating velocity of the flux vector could be freely controlled while both the fast torque and the optimal switching logic are obtained. The selection is based on the value of the stator flux and the torque. Both approaches are simulated for an induction motor. The results obtained have shown a superior performance over the conventional DTC one without the need of the mechanical sensor.

Keywords - Direct torque control, field oriented control, induction motor, sensorless vector control, flux estimators, switching strategy optimisation, multi-level inverter, neural-point clamped.

I. INTRODUCTION

Vast development in capacity and switching frequency of the power semiconductor devices, together with the continuous advancement of the power electronics technology have caused many changes in the static power converter systems and industrial motor drive areas. The conventional GTO inverters have limitation in their dc-link voltage. Hence the series connections of the existing GTO thyristors have been essential in realizing high voltage and large capacity inverter configurations with the dc-link voltage [1]. The vector control of the induction motor drive has made it possible for applications that require fast torque control such as traction [2]. In a perfect field oriented control, the decoupling characteristics of the flux and torque are affected significantly by the parameter variation of the machine.

This paper studies the control scheme for the direct torque and flux control of the induction machines which are fed by a three-level inverter by using a switching table. In this method, the output voltage is selected and applied sequentially to the machine through a look–up table so that the flux is kept constant and the torque is controlled by the rotating speed of the stator flux. The direct torque control (DTC) is one of the actively researched control schemes which is based on the decoupled control of flux and torque. It provides a very quick and robust response with simple control [3],[4].

The performances permit such a system to be applicable in areas such as railway traction, ac drives.

II. THREE-LEVEL INVERTER TOPOLOGY AND THE NPC VOLTAGE SOURCE

Fig. 1 shows the schematic diagram of the neutral point clamped (NPC) three-level VSI. Each phase of this inverter consists of two clamping diodes, four GTO thyristors and four freewheeling diodes.

![Schematic diagram of a three-level GTO inverter](image)

Table 1 shows the switching states of this inverter. Since three kinds of switching states are existed in each phase, a three level inverter has 27 switching states.

<table>
<thead>
<tr>
<th>Switching states</th>
<th>S₁</th>
<th>S₂</th>
<th>S₃</th>
<th>S₄</th>
<th>Vₙ</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>Vₐ</td>
</tr>
<tr>
<td>O</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>V₉/2</td>
</tr>
<tr>
<td>N</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>0</td>
</tr>
</tbody>
</table>

A two-level inverter is only capable in producing six non-zero voltage vectors and two zero vectors [2]. Fig.2 shows the representation of the space voltage vectors of a three-level inverter for all switching states.

According to the magnitude of the voltage vectors, we divide them into four groups : the zero voltage vectors (V₀), the small voltage vectors (V₁, V₄, V₇, V₁₀, V₁₃, V₁₆), the middle voltage vectors (V₃, V₆, V₉, V₁₂, V₁₅, V₁₈), the large voltage vectors (V₂, V₅, V₈, V₁₁, V₁₄, V₁₇).

The zero voltage vector (ZVV) has three switching states, the small voltage vector (SVV) has two, and both the middle voltage vector (MVV) and the large voltage vector (LVV) have only one [1].
III. INDUCTION MACHINE

Torque control of an asynchronous motor can be achieved on the basis of its model developed in a two axes (d, q) reference frame stationary with the stator winding. In this reference frame and with the conventional notations (appendix), the electrical mode is described by the following equations:

\[
\frac{di_d}{dt} = \frac{1}{\sigma T_L s} \phi_{sd} + \frac{p \Omega}{\sigma L_s} \phi_{sq} - \frac{1}{\sigma T_r} \frac{1}{I_s} i_{sd} - p \Omega i_{sq} + \frac{1}{\sigma L_s} V_{sd} \tag{1}
\]

\[
\frac{di_q}{dt} = \frac{p \Omega}{\sigma L_s} \phi_{sd} + \frac{1}{\sigma T_r} i_{sq} - \frac{1}{\sigma T_r} \frac{1}{I_s} i_{dq} + p \Omega i_{sd} + \frac{1}{\sigma L_s} V_{sq} \tag{2}
\]

\[
\frac{d\phi_{sd}}{dt} = V_{sd} - R_s i_{sd} \tag{3}
\]

\[
\frac{d\phi_{sq}}{dt} = V_{sq} - R_s i_{sq} \tag{4}
\]

\[
\phi_{sd} = L_s i_{sd} + L_m i_{rd} \tag{5}
\]

\[
\phi_{sq} = L_s i_{sq} + L_m i_{rq} \tag{6}
\]

\[
\phi_{rd} = L_r i_{rd} + L_m i_{sd} \tag{7}
\]

\[
\phi_{rq} = L_r i_{rq} + L_m i_{sq} \tag{8}
\]

The mechanical mode associated to the rotor motion is described by:

\[
J \frac{d\Omega}{dt} = \Gamma_{em} - \Gamma_r(\Omega) \tag{9}
\]

\(\Gamma_r(\Omega)\) and \(\Gamma_{em}\) are respectively the load torque and the electromagnetic torque developed by the machine.

IV. STATOR FLUX AND TORQUE ESTIMATION

Basically, DTC schemes require the estimation of the stator flux and torque. The stator flux evaluation can be carried out by different techniques depending on whether the rotor angular speed or (position) is measured or not. For sensorless application, the “voltage model” is usually employed. The stator flux can be evaluated by integrating from the stator voltage equation.

\[
\phi_s(t) = \int (V_s - R_s I_s) dt \tag{10}
\]

This method is very simple requiring only the knowledge of the stator resistance. The effect of an error in \(R_s\) is usually negligible at high excitation frequency but it becomes more serious as the frequency approaches zero [5].

![Fig. 3: Flux deviation](image)

Fig. 3 shows the representation of the space voltage vectors for one group of the switching states. The deviation that is obtained at the end of the switching period \(T_e\) can be approached by the first order Taylor Series as below.

\[
\Delta \theta_s = T_e \frac{\cos(\theta_v - \theta_s)}{\phi_{so}} \tag{11}
\]

Considering the combination of states of switching functions \(S_u, S_v, S_w\). Fig. 3 shows the adequate voltage vector selection in which we can increase or decrease the stator flux amplitude and phase in order to obtain the required performances. The electric torque is estimated from the flux and current information as [2]:

\[
\Gamma_{em} = p \left( i_{sq} \phi_{sd} - i_{sd} \phi_{sq} \right) \tag{12}
\]

V. PRINCIPLE OF DIRECT TORQUE CONTROL

Fig. 4 shows a block diagram of the DTC scheme. The reference values of flux, \(\phi^*\), and torque, \(\Gamma^*_e\), are compared to their actual values and the resultant errors are fed into a two level comparator of flux and torque, [2]. The stator flux angle, \(\theta_s\), is calculated by:

\[
\theta_s = \arctan \frac{\phi_{sq}}{\phi_{sd}} \tag{13}
\]

This is also quantified into 6 levels depending on which sector the flux vector falls into. Different switching strategies can be employed to control the torque depending on whether the flux has to be reduced or increased. Each strategy affects the drive behavior in terms of torque and current ripple, switching frequency and two or four-
A possible to drive selection of the voltage vector step by step, makes it possible to drive \( \varphi_s \), along a prefixed track curve.

\[ \Delta \varphi_s = V_s \cdot T_e \]  

(14)

The switching configuration is made step by step, in order to maintain the stator flux and torque within limits of the two hysteresis bands. Where \( T_e \) is the period that the voltage vector is applied to the stator winding, appropriate selection of the voltage vector step by step, makes it possible to drive \( \varphi_s \) along a prefixed track curve.

![Block diagram of direct torque control](image)

Fig. 4: Block diagram of direct torque control

Assuming the stator flux vector lying in the k-th sector \((k=1,2,3,4,5,6)\) of the \((d, q)\) plane, in the case of three level inverter, to improve the dynamic performance of DTC at low speed and to allow four-quadrant operation, it is necessary to involve the voltage vectors \( V_{k-1} \) and \( V_{k+2} \) in the case of three level inverter, to improve the dynamic performance of DTC at low speed and to allow four-quadrant operation, it is necessary to involve the voltage vectors \( V_{k-1} \) and \( V_{k+2} \) in torque and flux control. In the following, \( V_{k-1} \) and \( V_{k+2} \) will be denoted “backward” voltage vectors in contrast to “forward” voltage vectors utilised to denote \( V_{k+1} \) and \( V_{k-2} \). A simple strategy which makes use of these voltage vectors is shown in table 2. The conventional DTC for an induction motor fed by three-level voltage source inverter has been studied, \[6\].

<table>
<thead>
<tr>
<th>Table 2: Selection strategy for four-quadrant operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \varphi_s )</td>
</tr>
<tr>
<td>( \varphi_s )</td>
</tr>
</tbody>
</table>

For steady operating conditions, equations (12) that describe the machine torque can be transformed to a sinus function:

\[ \Gamma_{elmo} = \Gamma_{max.o} \cdot \sin 2\gamma_o \]  

(15)

\( \Gamma_{max.o} \) and \( \gamma_o \) are equation respectively torque and the difference angle between stator and rotor flux vectors.

\[ \Gamma_{max.o} = \frac{1 - \sigma}{2 \sigma L_s} \varphi_{so}^2 \]  

(16)

Equations (15) and (16) are established with the assumption that stator flux and rotor closed values are in steady state. For the disturbed states, the stator flux angle \( \theta \), has in practice a fast dynamic mode as compared to the rotor flux angle \( \theta \). If these two assumptions are held the effect of stator vector voltage on the machine torque can be expressed by the first order Taylor expansion as shown below:

\[ \Delta \Gamma_{elm} \approx K_\varphi \Delta \varphi_s + K_\theta \Delta \theta_s \]  

(17)

The sensitivity coefficients \( K_\varphi \) and \( K_\theta \) are defined by:

\[ K_\varphi = \frac{d\Gamma_{elm}}{d\varphi_s} = \frac{2}{\varphi_{so}} \Gamma_{elmo} \]  

(18)

\[ K_\theta = \frac{d\Gamma_{elm}}{d\theta_s} = 2 \Gamma_{max.o} \cos 2\gamma_o \]

Linking equations (11), (17) and (18) leads to:

\[ \Delta \Gamma_{elm} = 2 \frac{V_s \cdot T_e}{\varphi_{so}} \Gamma_{elmo} \cos (\theta - \theta_o) \]

(19)

\[ + \frac{2V_s T_e}{\varphi_{so}} \sqrt{\Gamma_{max.o}^2 - \Gamma_{elm}^2} \cdot \sin (\theta - \theta_o) \]

This shows the feasibility torque control by a well selected vectors voltage \( V_s \) \[6\].

According to the strategy, the stator flux vector is required to rotate in both positive and negative directions. Even at a very low shaft speed, large negative values of rotor angular frequency can be achieved, which are required when the torque is to be decreased very quickly. Furthermore, the selection strategy represented in table 2 allows good flux control to be obtained even in the low speed range. However the high dynamic performance which can be obtained by utilising voltage vectors and having large components tangential to the stator vector locus, have implied a very high switching frequency.

VI. SWITCHING STRATEGY FOR CONVENTIONAL DIRECT TORQUE CONTROL

The switching strategy in the order of the sector \( \theta_s \), is illustrated by each table.

<table>
<thead>
<tr>
<th>Sector</th>
<th>( \theta_s )</th>
<th>( \varphi_{so} )</th>
<th>( \Gamma_{elmo} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>PL 5 4 8</td>
<td>PS 3 4 6</td>
<td>ZE 0 0 0</td>
</tr>
<tr>
<td></td>
<td>NS 18 0 12</td>
<td>NL 17 13 14</td>
<td></td>
</tr>
<tr>
<td>02</td>
<td>PL 8 7 11</td>
<td>PS 6 7 12</td>
<td>ZE 0 0 0</td>
</tr>
<tr>
<td></td>
<td>NS 3 0 15</td>
<td>NL 2 16 17</td>
<td></td>
</tr>
<tr>
<td>03</td>
<td>PL 11 10 14</td>
<td>PS 9 10 15</td>
<td>ZE 0 0 0</td>
</tr>
<tr>
<td></td>
<td>NS 6 0 18</td>
<td>NL 5 1 2</td>
<td></td>
</tr>
<tr>
<td>04</td>
<td>PL 14 13 17</td>
<td>PS 12 13 18</td>
<td>ZE 0 0 0</td>
</tr>
<tr>
<td></td>
<td>NS 9 0 3</td>
<td>NL 8 4 5</td>
<td></td>
</tr>
<tr>
<td>05</td>
<td>PL 17 16 2</td>
<td>PS 15 16 3</td>
<td>ZE 0 0 0</td>
</tr>
<tr>
<td></td>
<td>NS 12 0 6</td>
<td>NL 11 7 8</td>
<td></td>
</tr>
<tr>
<td>06</td>
<td>PL 2 1 5</td>
<td>PS 18 1 6</td>
<td>ZE 0 0 0</td>
</tr>
<tr>
<td></td>
<td>NS 15 0 9</td>
<td>NL 14 10 11</td>
<td></td>
</tr>
</tbody>
</table>
VII. AN ENHANCED DIRECT TORQUE CONTROL

A switching table is used to select the best output voltage depending on the position of the stator flux and the desired action on the torque and stator flux. The flux position in the (d, q) plane is quantified in twelve sectors. Alternative tables are also existed for the specific operation mode. In the case of a two-level inverter, it is possible to expand the optimal vector selection in order to include a larger number of voltage vectors produced by a three-level inverter. The appropriate vector voltage is selected in such order that reduces the number of commutation and the level of steady-state ripple.

For the flux control, let the variable $E_\theta (E_\theta = \phi_s^* - \phi_s)$ be located in one of the three regions fixed by the contraints:

$$E_\theta < E_{\theta \text{min}}, E_{\theta \text{min}} \leq E_\theta \leq E_{\theta \text{max}}, E_\theta > E_{\theta \text{max}}.$$  

The switchable flux level is then bounded by $E_{\theta \text{min}}$ and $E_{\theta \text{max}}$. The flux control is made by the two-level hysteresis comparator. Three regions for the flux location are noted, flux as in fuzzy control schemes, by $E_{\theta \text{nn}}$ (negative), $E_{\theta \text{ns}}$ (zero) and $E_{\theta \text{np}}$ (positive).

A high level performance torque control is required. To improve the torque control let of the mismacth $E_T (E_T = \Gamma_{\text{em}} - \Gamma_s)$ to belong to one of the five regions defined by the contraints:

$$E_T < E_{T \text{min}2}, E_{T \text{min}2} \leq E_T \leq E_{T \text{min}1}, E_{T \text{min}1} \leq E_T \leq E_{T \text{max}1},$$

$$E_{T \text{max}1} \leq E_T \leq E_{T \text{max}2} \text{ and } E_{T \text{max}2} < E_T.$$

The five regions defined for torque location are also noted, as in fuzzy control schemes, by $E_{T \text{nl}}$ (negative large), $E_{T \text{ns}}$ (negative small), $E_{T \text{ps}}$ (zero), $E_{T \text{ps}}$ (positive small), $E_{T \text{pl}}$ (positive large). The torque is then controlled by an hysteresis comparator built with two lower bounds and two upper known bounds [7].

VIII. SWITCHING STRATEGY FOR AN ENHANCED DIRECT TORQUE CONTROL

The switching strategy in the order of the sector $\theta$s, is illustrated by each tables. The flux and torque control by vector voltage has a desacrate behavior in nature.

The vector voltage selection can then be made with an established table of knowledge and rules that have three inputs: flux mismatch $E_\theta$, the torque mismatch and the rank $k$ of the location sectors of $\theta_s$ shown by the fig. 5. It is also based on the vector diagram shown in fig.3. Looking at the position of the flux in the sector $\theta_s$, for a small decrease in flux and torque, state 15 is selected. For a small increase in flux in torque, state 3 is selected. For a small decrease in flux and large decrease in torque, state 14 is selected. For a small decrease in torque and a constant flux, state 0 is selected. Thus the selection changes as the position of the flux vector changes.

In fact it simply verifies that the same vector could be adequate for a set of value of $\theta_s$. The number of sectors should be set as large as possible in order to have an adequate decision. For this reason, we propose a new approach for direct torque control by using a three-level inverter based on twelve regular sectors noted by $\theta_1$ to $\theta_{12}$.

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Fig. 5: Location sectors of flux approach
IX. THE SIMULATION RESULTS

The validity of the proposed DTC algorithm for the three-level voltage source inverter is proved by the simulation results using Matlab-Simulink. The parameters of the motor are given in the Appendix. The used flux and torque mismatches for the approach are expressed in percentage with respect to the flux and torque reference values.

\[ E_{\phi\max} = 3\%, \ E_{\phi\min} = -3\%, \ E_{I_{\min}1} = -0.8\%, \ E_{I_{\min}2} = -3\%, \ E_{I_{\max}1} = 0.8\%, \ E_{I_{\max}2} = 3\%. \]

The simulation results illustrate both the steady state and the transient performance of the proposed torque control scheme. However, the machine has been supposed to run at load.

\[ \Gamma_f = \left( \frac{\Gamma_{cm}}{\Omega_{ref}} - K_f \right) \Omega \] \hspace{1cm} (20)

The FFT of the current waveform of phase (a) is shown in Fig. 6. The phase currents generated by the three-level inverter have low harmonic contents with the new approach (5.95 % THD).

Fig. 7 shows the phase current and flux for the steady state operation and the transient régime at 9 N.m with 0.9 Wb. The wave form of the stator current is closed to a sinusoidal signal. The trajectory of the flux in the case of the new approach is nearly a circle and it answers more quickly, (9ms), compared to the flux response in the conventional DTC.

Fig. 8 shows the torque reverse response from +9 N.m to -9 N.m and flux for 0.9 Wb. The output torque reaches the new reference torque in about 2 ms, fast torque response is obtained.

Low torque ripple is observed in Fig. 9. One nearly has the same rate of harmonic for the two approaches.

Fig. 10 shows an overtaking of the current which is acceptable. The simple voltage response of the motor commutes to a variable frequency in the two approaches.

Fig. 11 shows the torque response for a linear change in the torque reference, a good follow-up of the trajectory is obtained with a control of the stator flux that is achieved. The stator current wave form is shown more closely to the suitable sinusoidal signal. From this analysis, high dynamic performance, good stability and precision have been achieved.

![Fig. 6: Current harmonics enhanced](image1)

![Fig. 7: Vector flux locus and current response](image2)

![Fig. 8: Torque and flux response](image3)

![Fig. 9: Torque response and flux for steady state](image4)
The direct torque control DTC was introduced to provide a fast and well dynamic torque which is considered as an alternative to the field oriented control FOC technique. Two problems usually associated with the DTC drives which are based on hysteresis comparators, are the variable switching frequency and the inaccurate stator flux estimation. These have found to have a degrading effect in the drive performance. Another issue is concerned with the stability problem of the input DC voltage of the inverter, in which it is under survey.

The effect of the proposed method has been proven by the simulations conducted. It is concluded that the proposed control produces better results for transient state operation than that of the conventional control.

In this paper, a DTC systems using three-level GTO voltage source inverter is presented. It is found suitable for the high-power and high-voltage applications. Enhancement has been made on the DTC approach by introducing the two multi-level hysteresis comparators for flux and torque control. It imposes the flux angle detection procedure by defining twelve sectors of space and establishes a larger table of knowledge rules.

From the analysis of these results establish the following remarks:

The enhanced approach has a fast torque and flux response as compared to the conventional DTC. The amplitude of the torque ripples in steady state is closed for the two approaches.

**X. CONCLUSION**

The direct torque control DTC was introduced to provide a fast and well dynamic torque which is considered as an alternative to the field oriented control FOC technique. Two problems usually associated with the DTC drives which are based on hysteresis comparators, are the variable switching frequency and the inaccurate stator flux estimation. These have found to have a degrading effect in the drive performance. Another issue is concerned with the stability problem of the input DC voltage of the inverter, in which it is under survey.

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From the analysis of these results establish the following remarks:

The enhanced approach has a fast torque and flux response as compared to the conventional DTC. The amplitude of the torque ripples in steady state is closed for the two approaches.

**LIST OF THE USED NOTATIONS**

\[ s, r : \text{indices variables}; L : \text{magnetizing Inductance}; L_m : \text{mutual inductance}; V : \text{voltage}; i : \text{current}; \varphi : \text{flux}; R : \text{resistance}; \Gamma_{em} : \text{electromagnetic torque}; J : \text{rotor inertia}; P : \text{number of pairs of poles}; \omega_s : \text{statoric pulsation}; V_d : \text{dc-link voltage}; K_f : \text{friction Coefficient}; T_e : \text{sampling time}; E : \text{error of the variables}; r_T : \text{rotor time response}; s_T : \text{stator time response} \]

\[ \omega_r : \text{electric rotor speed}; \Omega = p \omega_s; \]

\[ \sigma : \text{Leakage coefficient}, \sigma = \frac{L_2}{L_s L_r} \]

**INDUCTION MOTOR PARAMETERS**

Rated power : 1.5 kW; Rated voltage : 220 V; Rated speed : 1420 rpm; Rated frequency : 50 Hz; Rotor resistance : 3.805 \( \Omega \); Stator inductance : 0.274 H; Rated current : 3.64 A (Y) et 6.31 (L); Stator resistance : 4.85 \( \Omega \); Rotor inductance : 0.274 H; Magnetizing Inductance : 0.258 H; Number of poles : 2; Rotor inertia : 0.031 \( \text{kg.m}^2 \); Friction Coefficient : 0.008 N.m.s/rd; \( V_d = 514 \text{ V} \); \( T_e = 100 \text{ s} \).

**REFERENCES**


Unity-Power-Factor Operation of Two-Stage Electronic Ballast

V. B. Borghate¹ and H. M. Suryawanshi²

Abstract – This paper presents the zero-voltage switched power-factor-correction (PFC) circuit. The proposed PFC circuit along with the half bridge asymmetrical series connected parallel loaded resonant inverter is used in the electronic ballast. The current is injected to the dc-bus capacitor at higher frequency as compared to the switching frequency of the inverter circuit. The high frequency (HF) modulated voltage source is generated in series between the input ac source and the dc-bus capacitor by simply using coupling inductor. This helps to boost the dc-bus voltage above the peak of ac input voltage. These lead to the unity-power-factor (UPF) operation of electronic ballast. The HF operation of PFC circuit reduces the switch current, limits the THD below 4.0%, increases the efficiency and reduces the component sizes. The circuit maintains UPF and low THD even under lamp power and input voltage variations. The prototype of the electronic ballast is built-up with inverter circuit to operate at 50 kHz and PFC circuit at 150 kHz. The simulation and experimental results of proposed circuit are presented for 40W fluorescent lamp with 230 V, 50 Hz input.

Keywords - Current injection, modulated voltage source, zero voltage switching, unity power factor.

I. INTRODUCTION

With continuous growth of population in the world, the demand for the power is ever increasing. The lighting is one of the major power-consuming loads. Therefore the electronic ballast operating at high efficiency and high power factor with low total harmonic distortion (THD) has become one of the important areas for the researchers. The continuous research has evolved two-stage [1]-[3] and single-stage electronic ballasts (EB) [4]-[10] operating at high efficiency, high power factor and low THD as compared electromagnetic ballast.

In [6], the HF voltage is derived from the transformer at the output of the inverter and connected in series with the boost inductor after the input diode rectifier to operate the EB at high power-factor and low THD. This HF voltage is of constant magnitude and depends on the dc-bus voltage. The EB in [7] uses the coupling inductor with buck-boost topology and the dc-bus voltage is to be maintained at value above the twice of peak of ac input voltage. This results in high voltage stress on the switches, if EB operates at 230 V, 50 Hz supply input. The topology used for EB in [8] employs the coupling inductor with very high value of leakage and magnetizing inductances. The leakage inductances are used as the boost inductor. This results in freewheeling of flat-top current at its peak value for the longer time, which may results in saturation of magnetic component of its PFC circuit. In these topologies, the commonly shared switches carry the both PFC as well as inverter currents, which results in increase in their current stresses.

In this paper, independent HF switched PFC circuit is proposed for the EB. The PFC circuit with its magnetic components is switched independently than inverter circuit. The proposed PFC circuit serves three functions as; feedbacks the current from the output of diode-bridge rectifier to the input of the ballast circuit at HF, injects the stored energy to the dc-bus capacitor at HF and generates the HF modulated voltage at the input of diode-bridge rectifier. Therefore, it maintains unity power factor and low THD at the ac source even under wide change in input voltage condition. HF operation (150 kHz) reduces the sizes of PFC circuit components, filtering requirements, magnitude of current to be injected, and flat-top current time period as compared to other topologies. The dc-bus voltage is required to maintain just above the peak of input ac voltage for operation of PFC circuit in discontinuous conduction mode (DCM). This topology reduces the current stress, voltage stress and power loss of the switches as they handle the PFC and inverter currents separately. Therefore, the proposed circuit operates at high efficiency, unity power factor and low THD. This circuit requires two additional switches as compared to single-stage EB. It is most suitable for high power lamp applications with high reliability, since the separate switches handle the PFC circuit current. The small values of leakage inductances of the coupling inductor (of PFC circuit) are sufficient to filter out the ripples of the input current, therefore, no separate EMI filter is required.

The operation and analysis of the proposed circuit are presented in the next section. The simulation is carried out to get insight of the circuit operation. The experimental results are obtained from the laboratory prototype fabricated for 40W fluorescent lamp at 230V, 50Hz.

II. OPERATION AND ANALYSIS OF THE PROPOSED PFC CIRCUIT

The circuit diagram of the proposed EB is shown in Fig. 1. The PFC circuit consists of inductor $L_p$, capacitors $C_1$-$C_2$, MOSFETS $M_1$-$M_2$, and coupling inductor $L_c$. The $L_p$ injects the current and transfers its stored energy to the dc-bus capacitor and also re-stores energy in every half switching cycle. The $C_1$ and $C_2$ act as the filter for the...
Fig. 1. Circuit diagram of proposed electronic ballast.

Fig. 2. Equivalent diagram of proposed PFC circuit.

Fig. 3. Operating modes of PFC circuit.
current of \( L_p \). These capacitors are sufficiently large enough so that the voltage across them remains constant during the switching cycle. The \( L_p \) has two identical coils wound on the common core. These coils carry the current in opposite directions and the cause of induced emf \( (v_m) \) in the coils is differential current component. Therefore, the \( L_p \) is represented as a transformer with two ideal windings \( w_1-w_2 \) and magnetizing inductance \( L_m \) as shown in Fig. 2 of equivalent circuit diagram. The \( w_1 \) and \( w_2 \) carry the same current, whereas the \( L_m \) carries the differential current of two coils. The \( L_m \) is reflected on the side of \( L_p \), which carries the larger current. The frequency of the induced emf is double of switching frequency of the PFC circuit and its magnitude decreases with increase in instantaneous value of input ac voltage and vice-versa. This induced emf acts as a HF modulated voltage source connected in series between ac input voltage and dc-bus voltage sources and always boosts the dc-bus voltage above the peak value of ac input voltage over the input 50 Hz cycle to obtain the discontinuous conduction mode (DCM) operation. The PFC and inverter circuits are switched at frequencies \( f_p \) and \( f \), respectively.

The following assumptions are made in the analysis.

- All the semiconductor devices and magnetic components are ideal.
- The dc-link capacitor \( C_d \) is large enough to be considered as a ripple free constant voltage source of magnitude \( V_d \).
- The \( V_d \) is always greater than the peak value \( V_{ip} \) of the ac input line voltage \( v_i \).
- The input voltage \( v_i \) is constant during a switching cycle, since the switching frequency \( f_p \) of the PFC circuit is much higher than the input supply frequency \( f \).
- The MOSFETs \( M_1-M_2 \) are switched symmetrically with duty ratio \( (d = 0.5) \).
- The fluorescent lamp operating at HF (50 kHz) is considered as a resistive load \( [2] \) of value \( R_{FL} \).

For clarity, operation and analysis of PFC circuit only are given in this section, since the inverter circuit is well presented in [1]-[10]. It is explained with the help of six modes of operation shown in Fig. 3, and the simulated waveforms of Fig. 4 over one switching time period \( T_s \).

Since the switch capacitances are of small values, the transition of MOSFETs is assumed instantaneous, and therefore the corresponding modes are not included.

### A. Operating modes

From the above discussion and Fig. 2,

\[
i_{a1} = i_{a2} \quad \text{and} \quad i_{C1} = \frac{i_{Lj}}{2}, \quad i_{C2} = -\frac{i_{Lj}}{2} \tag{1}
\]

\[
v_{C1} + v_{C2} = v_i, \quad v_{C1} = v_{C2} = d \cdot v_i = 0.5v_i, \quad \text{and} \quad V_d > V_{ip} \tag{2}
\]

Before the beginning of mode 1, it is assumed that the switch \( S_2 \) is in conduction and current \( i_{Lj} \) is circulating through \( S_2 \) and \( L_m \) at its positive peak value \(+i_{Lj}\), therefore \( i_2 = +i_{Lj} \) and \( i_1 = 0 \).

**Fig. 4:** Simulated waveforms of PFC circuit.

energy stored in \( L_p \) is transferred to \( C_d \). Therefore, the inductor current \( i_{Lj} \) decreases linearly from its maximum positive value \(+i_{Lj}\) to zero at \( t_1 \) as shown in Fig. 4. The energy is also supplied to \( L_m \) from the input source during this mode.

The expression of \( v_m \) & \( v_{Lj} \) with reference to Figs. 2 and 3(a) are,

\[
v_i = 2v_m + V_d, \quad v_{Lj} = v_m - v_{C1} = v_{C2} - V_d - v_m \tag{3}
\]

Therefore, from (1) to (3)
\[ v_m = \frac{V_d - v_i}{2} \]  
\[ v_{Lj} = -\frac{V_d - (1 - 2d)v_i}{2} \]

The inductor current \( i_{Lj} \) decreases linearly as,

\[ i_{Lj}(t) = I_{Lj} + \frac{v_{Lj}}{L_j}(t - t_0) \]
\[ = I_{Lj} - \frac{V_d - (1 - 2d)v_i}{2L_j}(t - t_0) \]

As \( i_1 = i_n \) and \( i_{Lj} = i_{Lj} \), the MOSFET \( M_1 \) current is,
\[ i_{M1} = -(I_{DSS} = i_{Lj} = -i_m) \]
\[ i_1 = i_1 + i_{C1} = i_1 + (i_{Lj}/2) \]

**Mode-2** \((t_1-t_2)\), Fig. 3(b): At \( t_1 \), \( i_{Lj} \) is decreased to zero, therefore the diode \( D_1 \) turns off naturally and upper switch \( S_1 \) turns on. Thus, it achieved the zero-voltage-switching (ZVS). The energy stored in \( L_m \) is transferred to \( L_j \) through \( S_1 \); therefore the current through \( L_j \) increases linearly in opposite direction at the same rate as that of last mode and reaches to maximum negative value -\( i_{Lj} \) at \( t_2 \) as it stored energy to its full capacity. Therefore, \( i_{M1} = i_{Lj} = -i_m \) and \( i_1 = i_1 - (i_{Lj}/2) \)

**Mode-3** \((t_2-t_3)\), Fig. 3(c): At \( t_2 \), the diode \( D_2 \) turns off because the current \( i_{Lj} \) has become zero. During this mode, the current \( i_{Lj} \) is clamped at -\( i_{Lj} \) and the additional energy of \( L_m \) is returned to the input source. Therefore,
\[ i_{Lj} = -I_{Lj} = -i_m, \quad i_2 = i_m = i_{Lj} \]
\[ v_{Lj} = 0, \quad v_m = v_{C1} = d \cdot v_i \]

and the input current, \( i_1 = i_{C2} = I_{Lj}/2 \)

**Mode-4** \((t_3-t_4)\), Fig. 3(d): At \( t_3 \), the switch \( S_1 \) is turned off and the diodes \( D_2 \) and \( D_3 \) start conducting. The energy stored in \( L_m \) is transferred to \( C_{j2} \) and the energy is supplied to \( L_0 \) from the input source during this mode. The inductor current \( i_{Lj} \) increases linearly from its maximum negative value (-\( i_{Lj} \)), and becomes zero at \( t_4 \). Therefore,
\[ v_1 = 2v_m + V_d, \quad v_{Lj} = v_{C2} = v_m + V_d \]
\[ v_m = \frac{V_d - v_i}{2} \]
\[ v_{Lj} = \frac{V_d - (1 - 2d)v_i}{2} \]

The inductor current \( i_{Lj} \) increases linearly from \( -i_{Lj} \) as;
\[ i_{Lj}(t) = -I_{Lj} + \frac{V_d}{L_j}(t - t_3) \]
\[ = -I_{Lj} - \frac{V_d - (1 - 2d)v_i}{2L_j}(t - t_3) \]

As \( i_2 = i_{n2} \) and \( i_{n1} = i_{n2} \), the MOSFET \( M_2 \) and input currents are
\[ i_{M2} = -(i_{SS2} = i_m = -i_{Lj}) \]
\[ i_1 = i_2 + (i_{Lj}/2) \]

**Mode-5** \((t_4-t_5)\), Fig. 3(e): At \( t_4 \), the diode \( D_3 \) turns off, as the current through it \( (i_{Lj}) \) is reached zero. The lower switch \( S_2 \) turns on, thus achieving its ZVS. During this mode, the energy stored in \( L_m \) is transferred to \( L_j \) through \( S_2 \). Therefore, the current through \( L_j \) increases linearly at the same rate as that of last mode but in opposite direction and reaches to maximum positive value +\( i_{Lj} \) at \( t_5 \) as it has stored energy to its full capacity. During this mode,
\[ i_{M2} = i_{Lj} = i_m - i_{Lj} \]
\[ i_1 = i_2 = (i_{Lj}/2) \]

**Mode-6** \((t_5-t_6)\), Fig. 3(f): At \( t_5 \), the diode \( D_1 \) turns off as the current \( i_1 \) is reached to zero. The inductor current \( i_{Lj} \) is clamped at +\( i_{Lj} \) and the additional energy is returned to the input source during this mode. Therefore,
\[ i_2 = i_m - i_{Lj} = i_{Lj} = +i_{Lj} \]
\[ v_{Lj} = 0, \quad v_m = v_{C2} = d \cdot v_i \]

At \( t_6 \), the switch \( S_2 \) is turned off and the mode 6 ends, completing one cycle of the switching frequency \( f_p \) of PFC circuit.

**B. Analysis of the PFC circuit**

During the modes 1 and 2, the current \( i_1 \) varies linearly as,
\[ i_1(t) = 0 + \frac{I_{Lj}}{t_2 - t_0}(t - t_0) \]
The instantaneous mean value of \( i_1 \) is the sum of the average value of \( i_1 \) and \( i_{Lj}/2 \) i.e. \( i_{avg} = i_{avg} + \left(\frac{I_{Lj}}{2}\right)_{avg} \).

The average value of \( i_{Lj} \) during \( t_0 \) to \( t_2 \) is zero. Therefore,
\[ i_{avg} = \frac{I_{Lj}}{2} + 0 = \frac{I_{Lj}}{2} \]

During the modes 4 and 5, the current \( i_2 \) varies linearly as,
\[ i_2(t) = 0 + \frac{I_{Lj}}{t_5 - t_3}(t - t_3) \]
The instantaneous mean value of \( i_2 \) is sum of the average value of \( i_2 \) and \( i_{Lj}/2 \) i.e. \( i_{avg} = i_{avg} + \left(\frac{I_{Lj}}{2}\right)_{avg} \).

The average value of \( i_{Lj} \) during \( t_3 \) to \( t_5 \) is zero. Therefore,
\[ i_{avg} = \frac{I_{Lj}}{2} + 0 = \frac{I_{Lj}}{2} \]

During the modes 3 and 6, the input current is also \( I_{Lj}/2 \). That is the instantaneous value of input current is constant and equal to \( I_{Lj}/2 \), and follows the input voltage over the complete switching cycle.

In references [7] and [8], the of leakage inductances of the coupling inductor are used as boost inductor and is given by,
\[ L_b = 2L_j = 2d^2 \frac{T_s V_p^2}{4P_i} = 2d^2 \frac{V_p^2}{4f_j P_i} \]

And the maximum current through it is,
\[ I_b = \frac{T_s V_p}{4L_b} = \frac{V_p}{4L_b f_j} \]
Where $P_i$, $V_{ip}$, and $T_i (=1/f_i)$ are the input power, peak value of ac input voltage and the time period of switching cycle of the ballast circuit respectively.

In the proposed topology, the frequency of the inductor current is twice the operating frequency of the PFC circuit. Therefore, the required value of current injecting inductor and its maximum current are,

$$L_j = \frac{d^2 V_{ip}^2}{4(2f_p)P_i} = \frac{V_{ip}^2}{32f_pP_i} = \eta \frac{V_{ip}^2}{32f_pP_o} \quad (28)$$

$$I_{Lj} = \frac{V_{ip}}{8L_j f_p} \quad (29)$$

Therefore, the input current, $i_j = \frac{V_{ip}}{16L_j f_p} \sin \omega t \quad (30)$

Where, $P_o$ and $\eta$ are output power and efficiency of the ballast circuit at rated input voltage respectively.

From (26) and (28), it is evident that the required values of the $L_j$ of proposed EB is one-fourth of $L_o$ in [7,8]. Equation (29) shows that the current $i_{Lj}$ is half of the corresponding current in other single-stage topologies at the same switching frequency. Their values further reduce with increase in operating frequency of the separately switched PFC circuit.

The minimum value of $L_m$ required for maintaining the $V_{ip}$ at $V_{ip}$ is $L_j/d$, if PFC and output circuits are operated at the same frequency. In this topology, PFC circuit is operated at comparatively higher frequency. Therefore, the minimum $L_m$ is,

$$L_m \leq \frac{L_j}{d} \left( \frac{V_{ip}}{V_{ip}} \right) \left( \frac{f_i}{f_p} \right) \quad (31)$$

From above discussions and operating modes, it is evident that,

- The ZVS of MOSFETs $M_1$-$M_2$ is achieved inherently.
- The rate of current injection is twice the operating frequency of PFC circuit.
- The magnitude of induced emf $v_m$ in coupling inductor $L_c$ varies in inverse proportion of the instantaneous value of the input ac voltage.
- The frequency of $v_m$ is twice of operating frequency of the separately switched PFC circuit $f_p$.
- The both coils $w_1$-$w_2$ of $L_c$ carry the same current in opposite direction, whereas its $L_m$ carries the equal and opposite current that of inductor $L_j$. Therefore, distortions in the input current because of HF injection current $i_{Lj}$ is minimized.

The value of $i_{Lj}$ varies from $+I_{Lj}$ to $-I_{Lj}$ or vice versa in an each half switching cycle. The rate of variation of $i_{Lj}$ is double as that of the boost inductor current in single-stage ballast with unconventional PFC circuit [6] and four times as that of the ballast with the two-stage PFC circuit [2]. The input current $i_j$ remains constant and equal to $I_{Lj}/2$ and follow the input voltage during the whole switching cycle.

Therefore, this circuit operates at unity power factor with low THD.

III. DESIGN EXAMPLE

The Laboratory prototype of the proposed electronic ballast is built to drive the 40W fluorescent lamp at 230 V, 50 Hz input source with following circuit parameters and components.

A. PFC circuit

$$f_p = 150 \text{ kHz}, \quad d = 0.5, \quad \eta = 0.94 \text{ (assumed)}, \quad L_j = 0.5 \text{ mH}, \quad L_m = 0.425 \text{ mH}, \quad L_{L1} = L_{L2} = 5 \mu \text{H}, \quad C_1 \text{ and } C_2 = 0.1 \mu \text{F (polypropylene)}.$$

B. Resonant circuit

The resonant circuit parameters are finalized by adopting the method described in [7], as given below.

The ratio of dc-bus voltage to lamp voltage, $(V_{dc}/V_{FL}) = 2$, $Q = 0.9$, $(f_i/f_p) = 1.12$, $f_i = 45 \text{ kHz}$, $f_p = 50 \text{ kHz}$, $L_r = 1.3 \text{ mH}, \quad C_r = 10 \text{nF (Polypropylene)}, \quad C_b = 0.47 \mu \text{F (Polypropylene)}$

MOSFETs $M_1$-$M_2$: IRFPC 30 and Diodes: $D_1$-$D_4$: UF408.
IV. SIMULATION AND EXPERIMENTAL RESULTS

The simulation and experimental results are obtained for the circuit shown in Fig. 1. From Fig. 5(a), it is evident that the magnitude of the induced HF voltage \(v_{m} \) in the coupling inductor \(L_c \) varies inversely with the instantaneous value of the input ac voltage. The voltage \(v' \) available at the input terminals of the diode-bridge rectifier shown in Fig. 5(b) is modulated at frequency of \(v_m \). Its magnitude is constant over the input cycle, and equal to sum of instantaneous input ac voltage \(v_i \) and twice the induced voltage, which keeps the diodes in conduction at the valley of ac input line voltage. The frequency of the \(v_m \) and \(v' \) is twice the operating frequency of the PFC circuit, that is 300 kHz. The inverter output circuit is operating in lagging mode, since the inverter switches are operated above the resonant frequency (45 kHz). Therefore, the inverter switches \(M_3 \) and \(M_4 \) operate with ZVS [1][10]. Fig. 6 indicates the ZVS operation of the active power switches of PFC circuit. The lamp voltage and current waveforms \(V_{FL} \) and \(i_{FL} \) shown in Fig. 7(b) are sinusoidal in nature. The current shape is sinusoidal and circular because of operation of inverter circuit at just above the resonant frequency, slightly nonlinear lamp behavior and non-ideal components. This is evident from V-I characteristic of the lamp shown in Fig. 7(a). The input ac voltage, current and dc-bus voltage waveforms shown in Fig. 8 substantiate the claim that the proposed circuit takes ripple-free input current at unity power factor even with variation in input voltage. The dc-bus voltage \(V_d \) is marginally above the peak of ac input voltage as shown in Fig. 8(c). The measured efficiency of the circuit is 94.2 % and its THD at 3.9 % at the rated input voltage.

V. CONCLUSION

This paper has presented a new circuit for the electronic ballast based on the two-stage boost converter topology. It uses the separately switched PFC circuit, which serves three functions viz. current injection; current feedback and generating the HF modulated voltage of constant magnitude at the input of the diode bridge rectifier to keep them in conduction even at valley point of the input ac line voltage to obtain the unity power factor. The very small leakage inductances of the coupling inductor of PFC circuit filter out the HF ripples of the input current, and no additional EMI filter is required. The operation and analysis of the proposed PFC circuit is given in detail. The experimental results are obtained of the laboratory prototype built for fluorescent lamp of 40 W at 230 V, 50 Hz. It maintains unity power factor, high efficiency and low THD (below 4.0 %) even under lamp power and input voltage variations. The proposed topology can also be used effectively with high reliability for high-power-lamp application at 230 V mains.

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Power Quality Improvement In Photovoltaic Systems

J.Devi Shree¹ and P.Anbalagan²

Abstract – In this paper, a maximum power point tracker and an optimum design of a pulse-width modulation (PWM) inverter for a grid connected photovoltaic energy conversion system is proposed. The MPPT provides the improved tracking operation under different conditions such as changing insolation and temperature. First, the implemented hardware of the system is described. Next, the principle of the MPPT control and selection of input and output variables and tuning of the membership functions are discussed. Then the multi-carrier pulse-width modulation (PWM) approach is introduced as a convenient way to implement a high-frequency link inverter. The approach is a direct extension of conventional PWM, and supports square-wave cycloconversion methods that have appeared in prior literature. Finally, the performance of the system is described. Simulation results of the experiments for inspecting the working of the system are presented.

Keywords - Phase detector (PD), phase locked loop (PLL), current source inverter (CSI), electro magnetic pollution, zero crossing detection.

I. INTRODUCTION

In recent years, the efforts to spread the use of renewable energy resources instead of pollutant fossil fuels and other forms have increased. As a result of advances in the production of photovoltaic modules and equipments like inverters and charge controllers, the use of photovoltaic on houses in urbanized areas has become more practical. A grid-connected inverter is a system, which is capable of converting the solar energy to AC electricity and supplying this electricity to the utility grid, to which the building is connected. Many methods have been proposed for maximum power point tracking (MPPT). So far, algorithms to achieve MPPT techniques are based on perturb and observe techniques [1] or incremental conductance methods and techniques employing intelligent control such as those using fuzzy logic, neural networks etc. [2-4]. In this study logic controller used for MPPT tracking of a grid connected photovoltaic conversion system. The method employed is believed to give a closer tracking of available energy from the sun. High-frequency (HF) ac link inverter topologies. It is possible to obtain the basic advantages directly in a PWM inverter, but only if the transformer can handle the low modulating frequency [5]. HF link topologies have not been common for medium power (1 to 20 kW), largely because of the number of power stages and control complexity. The complexity drawback has been overcome with a multiple-carrier PWM technique, which is introduced in this paper. We extend the control concept introduced in [6-7] and demonstrate that multiple-carrier PWM methods can lead to HF link inverters that are about as simple as the conventional PWM inverters. Here we also add elements to support natural commutation, thus reproducing results in [8] directly from familiar PWM processes.

II. MULTI-CARRIES PWM SEQUENCE GENERATION DESCRIPTION

A block diagram for the generation process is shown in Fig. 1. A base carrier (triangle or ramp) is phase-shifted, then divided into independent time segments by means of a decommutator [12] operating in synchronism with the carrier clock. A decommutator is more common in time-division multiplexing (TDM) communication systems, but its function here is the same segment the base carrier into time slices that can be used as the basis for the multiple-carrier approach.

III. HF LINK INVERTER CIRCUIT CONFIGURATION AND SWITCHING TIMING

Fig.2 shows a three-phase cycloconverter-type HF link inverter, which consists of an open-loop inverter to generate a 50% square wave, the HF link transformer, the output converter stack, and passive filtering for the output. The primary-side inverter bridge uses unipolar devices (MOSFETs or IGBTs with inverse diodes), while the three-phase output bridge consists of twelve unidirectional switches organized in six pairs. With natural commutation, only the leading edge of the gate pulses is needed, and the only feedback is the sign of the output currents [5]. The single-phase version of Fig.2 is interesting because control can be applied either at the input bridge or the output bridge. The gate sequence, multiplied by the square wave, recovers a conventional PWM output. Natural commutation in the HF link circuit is not affected significantly by dead time. When a short dead time is provided for the primary-side inverter, the output voltage cannot be quite as high, but the general operation is unchanged [11].

Digital ref: A070101133
¹Faculty EEE Department, Coimbatore Institute of Technology, Coimbatore
²Head of the Department, EEE, Coimbatore Institute of Technology, Coimbatore.

¹e-mail id – devi_567@yahoo.com
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Fig.1: The general two-carrier PWM sequence generation process
IV. DISCUSSION AND EXPERIMENTAL WORK

Fig. 3 shows a test circuit for a naturally-commutated square wave cycloconverter (similar to the power circuit in [10]), that uses the two-carrier process in Fig. 1 for control. Since the devices are SCRs, only the leading edge of the PWM pulse is needed. The decommutator is not necessary because only pulse transformers are needed to transmit the signal leading edge. Therefore, both comparators in Fig. 1 can be used directly with the original ramp. Two multivibrators use the rising edge to produce a 15 μs gate pulse train. The upper multivibrator creates a phase-delayed gate pulse train to be used when current is positive, while the lower multivibrator creates a phase-advanced gate pulse train. Simple logic is used with a current comparator to separate the positive and negative current conditions. Notice that in contrast with [9], the gate pulses have been generated directly with conventional sine-ramp PWM comparisons, with the ramp doing double-duty for both carriers.

Fig. 2: Main circuit configuration of the cycloconverter type HF link inverter

Fig. 3: Experimental circuit configuration

Fig. 4 shows experimental waveforms generated with the circuit of Fig. 3. The top trace is the ramp, at 2 kHz. The second trace is a 50Hz sinusoidal modulating function set for 70% modulation depth. Since only the leading edge is concerned, there is no need to add or subtract to produce a 50% duty ratio pulse train. We can consider signal P1(t) as phase lagging with respect to a 1 kHz square wave synchronized with the ramp, while P2(t) can be treated as phase leading. Fig. 5 shows waveforms from converter operation. The 2 kHz ramp is shown again at the top, along with a synchronized 1 kHz square wave from the HF link. The bottom two traces are the output voltage, which demonstrate the conventional two-level PWM behavior, and a signal proportional to the output current. Since the load is 60mH in series with 25 ohms, the filter allows a significant component to pass through in order to make the switch action and PWM behavior clear. Notice that this converter is using a 1 kHz link, and that the SCRs are switching at 1 kHz each. The combined behavior of devices in a pair gives rise to 2 kHz effective switching at the output. This property of the process can be used to extend the effective operating range of any given switching device [13].
In this paper, it has been shown how to generate such a switch sequence based on conventional PWM techniques. Just as important, the switch sequence can be configured to provide certain desirable properties, such as 50% duty ratio, effective frequency doubling, or natural commutation.

In our application [12], the use of two-carrier PWM leads to a more streamlined inverter topology. Total system losses can be reduced compared to a forward-converter/PWM inverter cascade, both because one conversion stage has been eliminated and because of the frequency doubling effect possible with two-carrier PWM.

V. MPPT TRACKING

A. PV Characteristics
Fig.6 shows the typical Power versus Voltage curve of the PV array [13]. In this figure, P is the power extracted from PV array and V is the voltage across the terminals of the PV array. The objective of the controller is to draw as much power as possible from the PV array. This point corresponds to the maximum power point (MPP) on the PV curve [14]. The change of PV curve and the new maximum power point is seen on the curve. It may be seen from Fig.6, that the PV curve changes when insolation changes e.g. if insolation increases the maximum power available from the PV array increases.
The PV curve is also dependent on the temperature of PV array as shown in Fig. 7. It is seen that as the temperature increases, the maximum power available from the PV array decreases. ΔP and ΔV are change in power and change in voltage respectively and calculated using P and V values as shown in Fig. 8 in successive steps. The slope of the tangent lines to the curve is different at different points. By inspecting Fig. 5, it may be seen that the slope is negative and large when power extracted from the PV array is small. It is zero at maximum power point. ΔP is required to ensure movement towards the peak i.e. MPP.

The technique is based on observing the calculated slope and ΔP and perturbing the system appropriately. The basic principle of the fuzzy controller can be explained with the following algorithm

1. Calculate slope (ΔP/ΔV) and ΔP.
2. If slope is negative, increase reference current so that more power is drawn from PV array.
3. Else if the slope is positive, system is operating at the left hand side of the MPP so decrease the reference current to return to MPP point.
4. Return to 1 in the next control step.

If some extreme cases are handled separately, much better performance can be obtained from the controller. Thus the conditions are checked to identify whether any extreme cases are present. If they do not exist then the controller is allowed

B. Priority Rules

Rule 1:
Starting algorithm:
IF PV array voltage is not very small AND system is shutdown
THEN Start applying reference current.

Rule 2.
IF “PV Array Voltage” is very small AND “PV current” is not very small
THEN Decrease “reference current” a little.

Rule 3
IF “PV Array Voltage” is very small AND “PV current” is very small
THEN Set “Current Reference” to zero.

Rule 4
IF Change in “PV Array Voltage” is very small
THEN Decrease “reference current” a little.

If the change in PV array voltage is very small then division by zero exception occurs in the calculation of the slope and slope is calculated as very large which is shown in Fig. 9. This condition may arise when change in PV curve occurs. For instance, assume the previous command was to increase reference current to extract more power. As a result, the PV array voltage is expected to decrease due to the fact that the power drawn from PV increases. On the other hand, if insolation increases as well, the PV curve moves also upwards increasing available power. Then the slope will be calculated incorrectly. In this condition, the fuzzy controller output will not be valid and it must be by-passed.

If the change in PV array voltage is very small then division by zero exception occurs in the calculation of the slope and slope is calculated as very large which is shown in Fig. 9. This condition may arise when change in PV curve occurs. For instance, assume the previous command was to increase reference current to extract more power. As a result, the PV array voltage is expected to decrease due to the fact that the power drawn from PV increases. On the other hand, if insolation increases as well, the PV curve moves also upwards increasing available power. Then the slope will be calculated incorrectly. In this condition, the fuzzy controller output will not be valid and it must be by-passed.

Fig: 6. Change of PV curve with increasing insolation

Fig: 7. Change of PV curve with increasing temperature

Fig: 8. The slope at different points on the PV curve.

Fig: 9. Occurrence of very small change in PV array voltage due to increase in insolation

A
In order to calculate slope correctly in the next control step, operating point is moved towards right simply by decreasing the reference current by 0.1A.

VI. CONCLUSION

In this paper a logic based MPP Tracker for a grid connected PV system is presented. The controller performance is optimized for better performance under changing PV conditions such as insolation and temperature. In order to increase the robustness of the system under exceptional conditions, and to maximize energy efficiency, the controller supported with a set of “if-then” like priority rules. Multi-carrier PWM serves as a direct way to construct HF inverter control waveforms. The results of multi-carrier PWM provide gating signals suitable for square-wave cycloconverters, for isolated gate drives, and for other implementation aspects of HF link inverters. The output results match those of conventional two-level PWM, except that the effective switching frequency doubles. Multi-carrier PWM techniques have special promise in the implementation of low-cost inverters. They support reduction in the number of stages, reduction in switching frequency, enhancements to gate drive design. When multi-carrier PWM is used, cycloconverter-type HF link inverters can be realized without additional complexity when compared to conventional cascaded inverters.

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BIographies

J.Devi Shree, received B.E Degree in Electrical and Electronics Engineering from Coimbatore Institute of Technology the year 1996 and M.E (Applied Electronics) from Bharathiar University in 1997. Currently she is pursuing Ph.D research work in the area of Non Conventional Energy under the guidance of Dr.P.Anbalagan. She is a lecturer of EEE department in Coimbatore Institute of Technology. She is having a 10 years in teaching experience. She has published six technical papers in national / international conferences. She is a member of IEEE. Her special fields of interest are Power electronics and Power Systems.

Dr.P.Anbalagan received B.E. Degree in Electrical and Electronics Engineering from Government College of Technology in the year 1973 and M.Sc(Engg.) from Madras University in 1977. He obtained Ph.D from Bharathiar University in the area of Digital Protection of Power Systems in the year 1994. He is having a teaching experience of 30 years. He is currently Professor and Head of EEE department in Coimbatore Institute of Technology. He has published 85 technical papers in national / international conferences and journals. He is a fellow member IE(India) and senior member of IEEE. His special fields of interest are Digital protection of power systems and Embedded Systems.
Operation of Three-Phase Resonant Converter in Single-Phase AC-to-DC Applications

*H. M. Suryawanshi¹, S. S. Tanavade², K. L. Thakre³ and M. A. Chaudhari⁴

Abstract – A single-phase ac-to-dc converter using three-phase modified series-parallel resonant converter is proposed in this paper. The three-phase resonant converter is analyzed using Fourier series approach. The design curves for a resonant converter of 2.5 kW rating are plotted. The converter components are selected based on the design curves. The converter is simulated for different load conditions using PSIM. A laboratory prototype of the converter is built. It is operated at 290 kHz on full load condition. The variable frequency control is implemented using digital signal processor for the output voltage regulation. The converter performance is verified using the simulation and experimental results. The use of three-phase high frequency for its output voltage regulation. Such a converter maintains high input power factor at the ac input line. Variable frequency control is implemented using a digital signal processor for the output voltage regulation. This converter maintains high input power factor without any active control of input line current. Apart from this, it requires narrow variation in switching frequency for its output voltage regulation.

Keywords - Three-phase resonant converter, high power factor, high frequency operation, ZVS operation

List of Symbols

\[\begin{align*}
N &= \text{Number of turns} \\
M &= \text{Normalised load current} \\
\omega_b &= \text{Switching frequency (rad/sec)} \\
\omega_r &= \text{Resonant frequency (rad/sec)} \\
\rho_c &= \text{Resistivity of copper} \\
b_c &= \text{Breadth of window area of the core} \\
k_f &= \text{Factor accounting for field distribution} \\
b_o &= \text{Breadth of bobbin} \\
h &= \text{Height allocated for winding} \\
F_p &= \text{Turn packing factor for turns in the winding relative to perfect square packing} \\
d_r &= \text{Diameter of 40 AWG wire} \\
F_{wp} &= \text{Factor accounting for serving area, bundle pack, strand packing and effect of twist on diameter} \\
\alpha, \beta &= \text{Constants with values 1.12 and 0.97 respectively} \\
C_n &= \text{Snubber capacitor}
\end{align*}\]

I. INTRODUCTION

The demand for isolated DC power with high power-packing density is ever increasing. Single-phase resonant converters are being used popularly in such small power tank circuits face severe voltage as well as current stresses. For high power requirements, the components in the single-phase resonant converter are much lower in the three-phase converter. Thus the three-phase resonant converters have many advantages over the single-phase resonant converters.

In this paper a single-phase ac-to-dc converter using three-phase modified series-parallel resonant converter (MSPRC) for input line power factor improvement is presented. Advantages of Modified series-parallel resonant converter are well known [12-13]. The converter is analyzed using Fourier series approach. Design curves for the converter are plotted to select the optimum value for the quality factor. The converter components for its optimum performance are selected using a step-by-step design procedure. The designs for the magnetic components and Litz wire are also discussed. A laboratory prototype of the converter is built for 2.5 kW rating. It is operated at minimum switching frequency of 290 kHz (on full load condition) to increase power-packing density. Since the power factor depends upon the ratio of switching frequency to the resonant frequency, the operation at higher switching frequency also results in the high power factor at the ac input line. Variable frequency control is implemented using a digital signal processor for the output voltage regulation. This converter maintains high input line power factor without any active control of input line current throughout the load range. It is shown that under varying load conditions, the converter operates in ZVS mode and requires a narrow variation in switching frequency for its output voltage regulation. Such a converter is useful in the sophisticated electrical drives and high power dc supplies.

Digital ref: A070101126
¹,²,³ Department of Electrical Engg, Visvesvaraya National Institute of Technology, Nagpur-440010, India,
*e-mail: hms_1963@rediffmail.com
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The major contribution of the paper includes the analysis using Fourier approach and design of three-phase HF resonant converter in single-phase AC-to-DC applications. The features of three-phase resonant inverter over single-phase resonant inverter: better utilization of HF transformer core, high power transfer for the same switch current, lower losses and component stresses owing to lower average switch current for the same power level and reduced HF output ripple allowing smaller size filter elements. High efficiency is achieved due to reduction in losses by zero-voltage switching (ZVS), and pure sinusoidal current flow through the switching devices because of resonant tank circuit. It also contributes to the design of litz wire for minimizing the eddy current loss due to skin effect.

II. OPERATING PRINCIPLE AND ANALYSIS

The proposed ac-to-dc resonant converter that employs the three-phase modified series-parallel resonant tank circuit with output LC filter is shown in Fig. 1. To regulate the output voltage of the converter variable frequency control with 1800 wide gating pulses scheme is used. The converter switching frequency is kept above the resonant frequency of the tank circuit. This scheme maintains the lagging power factor resulting in zero voltage switching (ZVS) of the HF inverter switches. Due to ZVS operation throughout the load range, the turn-on losses are practically eliminated. The turn-off losses are reduced by connecting loss-less capacitive snubbers across the HF switches. This results in higher efficiency over the entire load range. Moreover, since the converter operates above resonance frequency, the output filter can be designed for the full load operating frequency. Reactive components of the modified series-parallel resonant tank circuit in each phase of the three-phase HF inverter include L1, L2, C1, C2 and Cp. The capacitor Cp is connected across the secondary of HF transformer to achieve advantages of its leakage reactance referred to primary. This reduces the actual value of resonant inductor externally needed in the tank circuit.

Quasi-square wave voltages of HF inverter drive the three-phase tank circuit. Three-phase HF transformer (Y-Y) is used for isolation as well as voltage transformation.

Output voltage of HF transformer is rectified using three-phase HF diode Bridge to obtain dc output voltage. The output filter components \( L_f \) and \( C_f \) are designed at full load condition for the specified current and voltage ripple contents in the output respectively.

\[
V_B = V_{dc}, \quad Z_B = \sqrt{L_f/C_{eq}}, \quad I_B = V_B/Z_B \tag{1}
\]

where, \( C_{eq} = \frac{C_1}{1 + \alpha}, \quad \alpha = \frac{C_1/C_2}{1 - (1/y^2 \omega_r^2 L_f C_f)} \), \( y = \omega_f/\omega_r \).

All the normalized quantities are denoted by an additional
The resonant frequency \( \omega_r \) is given by,
\[
\omega_r = \sqrt{\frac{u}{L_1 C_1}}
\]  
(3)

where,
\[
u = \sqrt{a^2 + s^2 - 4},
\]
\[
a = \sqrt{pq}, \quad s = 1 + \frac{1}{p} + \frac{1}{pq}, \quad p = \frac{L_1}{L_2}, \quad q = \frac{C_1}{C_2}, \quad r = \frac{C_1}{C_p}
\]

The converter gain is given by, \( M = V_o / V_m \), where, \( V_o = n_1 V_o \).

The normalized load current \( J = I_o / I_B \) where, \( I_o = I_n/n_1 \).

The expressions for normalized line-to-line quasi-square wave voltage \( V_{RLn} \) and normalized line-to-neutral voltage \( V_{RLn} \) are as below,
\[
V_{RLn} = \frac{4}{\pi} \sum_{n=6}^{\infty} \frac{1}{n} \sin(n \omega t + n \pi/6) \cos(n \pi/6)
\]  
(4)

\[
V_{RLn} = \frac{2}{\pi} \sum_{n=6}^{\infty} \frac{1}{n} \sin(n \omega t)
\]  
(5)

The expressions for the other two phases can be obtained by phase shifting the above equations by 120° and 240° respectively. The rectifier input current of phase \( n \) is referred to primary side is represented by,
\[
i_{an} = \frac{4J}{\pi} \sum_{n=6}^{\infty} \frac{1}{n} \sin(n \omega t - n \phi) \cos(n \pi/6)
\]  
(6)

Referring to the Fig. 2 (a) following equations are written.
\[
V_{RLn} = I_{L1n} X_{C_{seriso}} + I_C \sin \phi
\]  
(7)

\[
i_{an} = I_{L1n} - I_C \sin \phi
\]  
(8)

Substituting \( I_C \) from equation (8) into equation (7) and simplifying it, the normalized instantaneous current flowing through the resonant tank circuit is,
\[
I_{L1n} = \frac{\sum_{n=6}^{\infty} a_n^2 \sin(n \omega t + \theta_n) + b_n^2 \cos(n \omega t)}{n \pi X_{C_{eqno}}}
\]  
(9)

where, \( a_n = \frac{4J \sin(n \phi) \cos(n \pi/6) X_{C_{eqno}}}{n \pi X_{C_{eqno}}} \)

\( b_n = \frac{2(1 - 2J \sin(n \phi) \cos(n \pi/6) X_{C_{eqno}}}{n \pi X_{C_{eqno}}} \)

\( \theta_n = \tan^{-1} \frac{b_n}{a_n} \)

Using equation (9), the expressions for the normalized instantaneous voltages across resonant tank components are written as follows.
\[
V_{RLn} = I_{L1n} X_{L1n} = \sum_{n=6}^{\infty} \sqrt{a_n^2 + b_n^2} \sin(n \omega t + \gamma_n)
\]  
(10)

\[
V_{CN} = I_{L1n} X_{C_{ino}} = \sum_{n=6}^{\infty} \sqrt{a_n^2 + b_n^2} \sin(n \omega t + \xi_n)
\]  
(11)

\[
V_{CN} = V_{L2n} X_{C_{c121n}} = \sum_{n=6}^{\infty} \sqrt{a_n^2 + b_n^2} \sin(n \omega t + \psi_n)
\]  
(12)

where, \( e_n = b_n X_{C_{ino}}, \quad f_n = a_n X_{C_{ino}}, \quad \xi_n = \tan^{-1} \frac{e_n}{f_n} \)

\( i_{an} = a_n X_{C_{c121n}}, \quad m_n = a_n X_{C_{c121n}}, \quad \eta_n = \tan^{-1} \frac{i_{an}}{m_n} \)

\( g_n = \frac{2}{n \pi}, \quad h_n = -a_n X_{C_{seriso}}, \quad \psi_n = \tan^{-1} \frac{g_n}{h_n} \)

\( X_{C_{c121}} = \text{equivalent reactance of parallel combination of } X_{L_2} \text{ and } X_{C_2}. \)

For evaluating the above equations, the angle \( \phi \) between \( i_{an} \) and \( V_{RLn} \) must be known. This can be determined numerically by using the condition that \( i_{an} \) starts flowing in the positive direction when \( V_{RLn} = V_{C_{ino}} \). The normalized converter gain \( M \) is given by,
\[
M = \frac{V_o}{V_m} = \frac{6 \sqrt{2}}{\pi} \frac{\phi \sin \phi}{\phi \^2/6} \int_{-\phi}^{\phi} d\omega_t
\]  
(14)

III. DESIGN OF CONVERTER

Owing to the filtering action of resonant tank circuit, the fundamental component of the inverter output current is much larger than the harmonics. Hence for the design procedure of the converter in this section, the sine wave approximation is considered for the voltage and the current waveforms. Further, the higher switching frequency is chosen at full load condition results in high input power factor, since the power factor depends upon the ratio of the switching frequency to resonant frequency.

Input voltage, \( V_m = 230 \text{ V (rms)}, f_m = 50 \text{ Hz} \)

Output voltage, \( V_o = 250 \text{ V} \)

Output power, \( P_o = 2.5 \text{ kW} \)

Resonant frequency, \( f_s = 282 \text{ kHz} \)
Minimum switching frequency, \( f_s = 290 \text{ kHz} \)

Peak to peak output current ripple, \( I_{pp} = \pm 5 \% \) of \( I_o \)

Peak to peak output voltage ripple, \( V_{pp} = \pm 10 \% \) of \( V_o \)

For near optimum values of converter gain, total kVA per kW rating of the resonant tank circuit and the inverter output current, the following inductor and capacitor ratios are selected [12].

\[
\frac{L_1}{L_2} = 0.1, \quad \frac{C_1}{C_2} = 0.1, \quad \frac{C_1}{C_p} = 10
\]

For the above inductor and capacitor ratios, the design curves as shown in Fig. 3 are plotted for various values of \( Q \), using program developed in MATLAB. From Fig. 3, it can be seen that for near optimum values of converter gain, kVA rating of the resonant tank circuit per kW output of the converter, peak inverter output current and switching frequency variation for output voltage regulation the value of 1.8 is selected for \( Q \).

Using equation (5), the rms value of the fundamental component of the line-to-neutral voltage of the HF inverter equals 93.18 V. Considering the design of resonant converter at resonant frequency, the tank gain is approximately unity. Thus from Fig.1, the voltage across primary winding of HF transformer is 93.18 V. To obtain 250 V dc output voltage, the phase voltage of 106.87 V is needed at the input terminals of three-phase HF diode bridge rectifier. Hence the transformation ratio \( n \) for the HF transformer is 93.18:106.87 \( \approx 0.87:1 \). The quality factor \( Q \) of resonant tank circuit is given by,

\[
Q = \frac{\omega L_1}{R_L}
\]  

(15)

Using equations (3) and (15), the optimum component values for the tank components are calculated as given below.

\[
L_1 = 19.22 \text{ \mu H}, \quad L_2 = 192.2 \text{ \mu H}, \quad C_1 = 0.0182 \text{ \mu F}, \quad C_2 = 0.182 \text{ \mu F}, \quad C_p = 0.00182 \text{ \mu F}, \quad C_p' = n^2 C_p = 0.00138 \text{ \mu F}
\]

A. Design of magnetic components and litz wire

Magnetic components of the converter shown in Fig.1 (inductors \( L_1 \) and \( L_2 \) in the tank circuit, HF transformer and the filter inductance \( L_f \)) need to be designed to minimize the core and the winding losses. Since ferrite materials provide very high specific resistance, the eddy current losses in the core made-up of these materials may be practically disregarded. Ferrite materials M33 (frequency range 200 kHz to 1.6 MHz) and N87 (frequency range up to 500 kHz) of Siemens make find their usage in high Q inductors in the resonant circuits and transformers respectively. Hence for \( L_1 \) and \( L_2 \), pot cores P26x16 made-up of M33 material while for the HF transformer E30x15x7 cores made-up of N87 material are used. Further to minimize the winding losses due to skin effect, Litz wires (conductors made-up of multiple, individually insulated strands twisted together) are used for the winding of the inductors and the HF transformer.

For the given number of turns and winding cross sectional area, as the number of strands in a litz wire is increased, cross sectional area of each strand must be decreased. This typically leads to reduction in eddy current loss. However, as the number of strands increase, the fraction of window area filled with copper decreases and the fraction filled with the insulation increases. This results in increased dc resistance. Eventually, eddy current loss is made small till increasing dc resistance offsets any further improvement in it. Thus there is an optimal number of strands \( n_{opt} \) that results in minimum winding loss [14, 15]. This is given by,

\[
n_{opt} = \left[ \frac{2}{\beta - 1} \right] \cdot \frac{1}{\sqrt{\left( \frac{1}{\beta - 1} \right)^2 - \left( \frac{1}{\beta} \right)^2}}
\]

(16)

where,

\[
y = \frac{\pi^2 - N^2 \cdot \alpha_x^2 \cdot \mu_0^2 \cdot d_e \cdot \left( \frac{6}{\beta} \right) - \frac{6}{\beta} \cdot \left( F_p \cdot F_p' \cdot b_h \cdot b_h / N \right)^{\frac{3}{\beta}} \cdot k_F}{768 \cdot \rho_e^2 \cdot b_c^2}
\]
The output filter inductance \( B \). Output filter design

Calculations for optimum number of strands for resistance and hence to minimize the winding loss. The integral number of strands can be chosen to minimize ac AWG wire for these calculations suggest the use of 2136 strands of 52 AWG wire for minimum winding loss. Although the design 'D7' with 48 secondary are wound. Table 2 shows the different designs 30x15x7, N87 ferrite core, 10 and 12 turns on primary and reference. To have best cost-loss compromise, the design with 44 AWG wire is taken as reference. To have best cost-loss compromise, the design with 260 strands of 42 AWG is selected for inductance L1. Similar design procedure is used to design inductance L2. To design the HF transformer of the ratio \( n_t = 0.87 \) on EE 30x15x7, N87 ferrite core, 10 and 12 turns on primary and secondary are wound. Table 2 shows the different designs for the HF transformer. Although the design ‘D7’ with 48 AWG wire results in minimum loss, its relative cost is high. Hence to have cost-loss trade-off, the design ‘D4’ with 42 AWG wire is selected that gives slightly higher loss with lesser relative cost.

B. Output filter design

The output filter inductance \( L_F \) must suppress the switching frequency component of rectified resonant capacitor voltage \( V_r \). This component has a minimum ripple frequency of 1.74 MHz (six times the inverter switching frequency). The magnitudes of its harmonic components are given by,

\[
V_{fn} = \frac{2V_o}{4n^2 - 1}
\]

where \( n \) is in multiples of 2\( f_s \). The dominant component of this voltage is at \( n = 3 \) i.e. at 6\( f_s \). This is given as,

\[
V_{r3} = \frac{2V_o}{35}
\]

The value of filter inductance is calculated using the peak-to-peak ripple specification of output current as below.

\[
L_F = \frac{2(2V_o/35)}{6\omega_d I_p-p} = \frac{V_o}{105\pi f_s I_p-p}
\]

The magnitudes of the harmonic components of the rectified output current are given by,

\[
I_{rn} = \frac{2I_o}{4n^2 - 1}
\]

The dominant component of this current is at \( n = 1 \) i.e. at 2\( f_o \).

This is given by, \( I_{r1} = \frac{2I_o}{3} \)

The output filter capacitance \( C_F \), which is required to limit the double line frequency component of the rectifier output voltage to the ripple specification \( V_{p-p} \) is determined using the equation (20) given as

\[
C_F = \frac{2(2I_o/3)}{2 \omega_{in} V_{p-p}} = \frac{I_o}{3 \pi f_{in} V_{p-p}}
\]

The use of \( L_F \) reduces the charging current of \( C_F \). This in turn reduces the line current of the inverter, improving the efficiency of converter. This also reduces the stresses on the resonant tank components. The filter inductance \( L_F \) is

![Image](https://example.com/image1.png)

**Fig. 3:** Converter design curves for \( L_1/L_2 = 0.1, C_1/C_2 = 0.1 \) and \( C_1/C_2 = 10. \) (a) Converter gain (b) kVA per kW for tank circuit (c) Switching frequency variation for output voltage regulation and (d) Peak inverter output current.

![Image](https://example.com/image2.png)

**Fig. 4:** Variation of resistance factors with strands for a Litz wire wound inductor (L1)

**Table 1:** Design table for \( L_1 \) for optimal and sub-optimal stranding.

<table>
<thead>
<tr>
<th>AWG Strands</th>
<th>Fr</th>
<th>Relative Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>38</td>
<td>70</td>
<td>3.886</td>
</tr>
<tr>
<td>39</td>
<td>100</td>
<td>3.231</td>
</tr>
<tr>
<td>40</td>
<td>175</td>
<td>2.607</td>
</tr>
<tr>
<td>41</td>
<td>225</td>
<td>2.431</td>
</tr>
<tr>
<td>42</td>
<td>260</td>
<td>2.351</td>
</tr>
<tr>
<td>44</td>
<td>485</td>
<td>2.132</td>
</tr>
<tr>
<td>52</td>
<td>2136</td>
<td>2.002</td>
</tr>
</tbody>
</table>

**Table 2:** Winding design table for HF transformer.

<table>
<thead>
<tr>
<th>Design</th>
<th>Gauge</th>
<th>( W_1 )</th>
<th>( W_2 )</th>
<th>Strands</th>
<th>Relative Cost</th>
<th>Relative Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>38</td>
<td>38</td>
<td>70</td>
<td>70</td>
<td>0.29</td>
<td>1.95</td>
</tr>
<tr>
<td>D2</td>
<td>40</td>
<td>40</td>
<td>175</td>
<td>175</td>
<td>0.51</td>
<td>1.54</td>
</tr>
<tr>
<td>D3</td>
<td>41</td>
<td>41</td>
<td>225</td>
<td>225</td>
<td>0.57</td>
<td>1.36</td>
</tr>
<tr>
<td>D4</td>
<td>42</td>
<td>42</td>
<td>260</td>
<td>260</td>
<td>0.59</td>
<td>1.24</td>
</tr>
<tr>
<td>D5</td>
<td>44</td>
<td>44</td>
<td>485</td>
<td>485</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D6</td>
<td>46</td>
<td>46</td>
<td>972</td>
<td>972</td>
<td>2.65</td>
<td>0.97</td>
</tr>
<tr>
<td>D7</td>
<td>48</td>
<td>48</td>
<td>1524</td>
<td>1524</td>
<td>7.35</td>
<td>0.69</td>
</tr>
<tr>
<td>D8</td>
<td>50</td>
<td>50</td>
<td>1932</td>
<td>1932</td>
<td>20.38</td>
<td>0.72</td>
</tr>
<tr>
<td>D9</td>
<td>52</td>
<td>52</td>
<td>2136</td>
<td>2136</td>
<td>53.55</td>
<td>0.95</td>
</tr>
</tbody>
</table>
designed to suppress the switching frequency ripple in the output current. This ripple frequency is six times the switching frequency (1.74 MHz at full load for switching frequency of 290 kHz). Thus, the filtering requirements are drastically reduced. The values of $L_F$ and $C_F$ calculated using equations (18) and (20) are 2.61 $\mu$H and 424 $\mu$F respectively.

**IV. EXPERIMENTAL RESULTS**

The converter designed in section 3 is simulated using PSIM. The behavior of the converter at different load conditions is studied. Fig. 5 shows the results of ac input line voltage and line current at full load condition, at 50% and 25% of full load condition. The converter maintains high input line power factor for the entire load range. The inverter switches operate in ZVS mode.

The single-phase ac-to-dc converter using three-phase MSPRC, designed in section 3, is built to verify its performance. The actual components used for experimentation are as follows. The IGBT-HGTG20N60A4D, HF diodes DSEI 60-12A, $L_1=19.25$ $\mu$H including 1.66 $\mu$H leakage inductance of HF transformer, $L_2=190$ $\mu$H, $C_1=0.02$ $\mu$F, $C_2=0.2$ $\mu$F, $C_p=1500$ pF, $L_F=2.61$ $\mu$H, $C_F=440$ $\mu$F, load resistance at full load 25 $\Omega$. A small EMI filter as shown in Fig. 6 is used at the input to suppress the high frequency switching noise and ripple.

To regulate the output voltage of this converter, the variable frequency control scheme is implemented using a digital signal processor (DSP) TMS320LF2812. The use of DSP facilitates the accurate generation of gating pulses for the HF inverter switches with the minimal hardware requirement. The insertion of equal and precisely calculated dead bands between the switching instants of the devices in all the three HF inverter legs is an easy task using the inbuilt programmable dead band units of the DSP. Moreover, along with the output voltage regulation, the functions like overload protection, analog to digital conversion of various analog parameters used for converter control, digital filtering of these sensed parameters and PID control algorithm are also implementable using the software techniques. At high switching frequencies transistorized gate driver circuits are insufficient to drive IGBTs. Further to achieve good performance and to avoid false triggering of the IGBTs during their off state, bipolar gate drivers are needed. Hence a high performance bipolar gate driver scheme using high speed MOSFETs (IRF510 and IRF9510) is fabricated for driving three-phase HF inverter.

The inductors $L_1$ and $L_2$ in the resonant tank circuit are wound on P26x16, M33 ferrite cores using 260/42 AWG (260 strands made-up of 42 AWG wire) and 100/42 AWG (100 strands made-up of 42 AWG wire) litz wires respectively. Use of M33 ferrite cores and litz wires greatly reduced the core losses and winding losses respectively. The HF transformer is built on E30x15x7 core sections made-up of N87 ferrite material using 260/42 AWG litz wire. The leakage inductance of the HF transformer referred to its primary (1.66 $\mu$H) is used as a part of resonant inductor. All the capacitors used in the resonant tank circuit are of polypropylene type to achieve good performance.

The experimental waveforms of the converter are shown in Figs.7-11. It can be seen from Fig.7 that the converter maintained excellent input line power factor throughout the load range. The three-phase HF inverter is operated above the resonant frequency, making current flow through the resonant tank circuit (inverter output current) lagging the inverter output voltage. Hence the lagging power factor mode of operation of HF inverter is achieved. Thus, HF inverter switches turns-on only when the voltage across switches falls to zero due to already conducting their anti-parallel diodes. This results in zero-voltage switching operation of all switches. This is evident from Fig.8. The peak inverter output current and voltage across resonant capacitor went on reducing with load as it can be seen from Fig.9. Thus apart from maintaining good part load efficiency, reduced peak stresses on the resonant components were found to exist in the converter. The line-to-line voltage outputs of the three-phase HF inverter are shown in Fig.10. Fig.11 shows the experimentally obtained operating area of the HF inverter switch over one switching period at peak of ac input cycle. The operation is seen well within the safe operating area (SOA) of the device. The dc output voltage of the converter is regulated at 250 V. The output voltage and output current
waveforms of the converter at full load condition are shown in Fig.12. The overall performance of the converter is given in Table 3.

![Fig. 6: EMI filter at the input of ac line](image)

Fig. 6: EMI filter at the input of ac line

![Fig. 7: Experimental waveforms for input voltage and input line current for the converter under variable frequency (VF) control.](image)

Fig. 7: Experimental waveforms for input voltage and input line current for the converter under variable frequency (VF) control. Scales: time 5 mS/div, voltage 100 V/div. (a) Full load. Current scale: 10 A/div. (b) 50% load. Current scale: 5 A/div. (c) 25% load. Current scale: 2 A/div.

![Fig. 8: Experimental waveforms for phase voltage and phase current of three-phase HF inverter under Variable frequency control at full load.](image)

Fig. 8: Experimental waveforms for phase voltage and phase current of three-phase HF inverter under Variable frequency control at full load. Scales: time 2 µS/div, voltage 100 V/div., Current scale: 10 A/div.

V. CONCLUSION

![Fig. 9: Experimental waveforms for currents (I_{L1} and I_{L2}) through resonant inductors (L_{1} and L_{2}) and capacitor voltages (V_{C1} and V_{C2}).](image)

Fig. 9: Experimental waveforms for currents (I_{L1} and I_{L2}) through resonant inductors (L_{1} and L_{2}) and capacitor voltages (V_{C1} and V_{C2}). (a) Full load, (b) 50% load, Scales: time 1 µS/div, voltage 100 V/div, current 5 A/div.

![Fig. 10: Experimental waveforms for line-to-line voltage output of three-phase HF inverter.](image)

Fig. 10: Experimental waveforms for line-to-line voltage output of three-phase HF inverter Scales: time 2 µS/div, voltage 100 V/div.

![Fig. 11: Curve for the operating area of HF inverter switch over one switching period near peak of ac input cycle.](image)

Fig. 11: Curve for the operating area of HF inverter switch over one switching period near peak of ac input cycle. Scales: voltage 100 V/div, current 5 A/div.

Table 3: Overall experimental performance of the converter under variable frequency control

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Full load</th>
<th>50% Load</th>
<th>25% Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Factor</td>
<td>1.00</td>
<td>1.00</td>
<td>0.99</td>
</tr>
<tr>
<td>THD (%)</td>
<td>3.0</td>
<td>3.1</td>
<td>7.1</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>92</td>
<td>95</td>
<td>90</td>
</tr>
<tr>
<td>Switching Frequency (kHz)</td>
<td>290</td>
<td>317</td>
<td>370</td>
</tr>
<tr>
<td>Total HF inverter Losses, Watt</td>
<td>100.8</td>
<td>32.2</td>
<td>28.4</td>
</tr>
<tr>
<td>Peak Inverter current (Amp.)</td>
<td>16.35</td>
<td>8.09</td>
<td>4.31</td>
</tr>
</tbody>
</table>


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A single-phase ac-to-dc converter employing three-phase MSPRC has been proposed. This topology has several advantages such as excellent power factor without any active control of input current, usefulness for high power applications, the use of HF transformer leakage inductance as a part of resonant inductor, narrow variation of switching frequency for wider load variation, higher power packing density and minimal filtering requirements due to high switching frequency, high power conversion efficiency due to reduced conduction losses. Although the number of components required in this converter is more as compared to single-phase converter, the current and voltage stresses on these components are much lower. Such a converter will definitely be useful for high power applications.

Fourier series analysis has been carried out for the converter. The design curves for the converter have been plotted. A systematic design procedure, based on the design curves, has been given along with a design example of a 2.5 kW resonant converter. PSIM simulation and detailed experimental results have been presented. These results demonstrate the high power factor operation for the entire load range without any active control of ac input line current. The converter maintains good part load efficiency, since the peak inverter currents have been shown decreasing with the load current. The variable frequency control has been implemented for the output voltage control under varying load conditions using a digital signal processor. The converter has been shown operating in ZVS mode for the entire load range.

REFERENCES


Reduced PWM Harmonic Distortion for a New Topology of Multilevel Inverters

Tamer H. Abdelhamid

Abstract—Harmonic elimination problem using iterative methods produces only one solution, not necessarily the optimal solution. In contrast to using iterative methods, an approach based on solving polynomial equations using the theory of resultant, which produces all possible solutions, is used. The set of switching angles that produces the lowest THD is considered. This paper demonstrates how reduced harmonic distortion can be achieved for a new topology of multilevel inverters. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels. The modes of operation are outlined for 5-level inverter, as similar modes will be realized for higher levels. Simulation of different number of levels of the proposed inverter topology along with corroborative experimental results are presented.

Keywords—Multilevel inverter, harmonic elimination, programmed PWM.

I. INTRODUCTION

The general concept of multilevel power conversion was introduced more than twenty years ago. However, most of the development in this area has occurred over the past five years. Multilevel converters have emerged as a very important alternative in the area of high-power medium-voltage applications [1]. Multilevel inverters have the ability to synthesize waveforms with a better harmonic spectrum. However, their increasing number of devices tends to reduce the overall reliability and efficiency of the power converter.

The principal function of multilevel inverters is to synthesize a desired ac voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells [2]. The desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. With an increasing number of dc sources, the inverter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme.

While many different multilevel inverter topologies have been proposed, the two most common topologies are the cascaded H-bridge inverter and its derivatives [3], and the diode-clamped inverter [4]. The main advantage of both topologies is that the rating of the switching devices is highly reduced to the rating of each cell. However, they have the drawback of the required large number of switching devices which equals \(2(k-1)\) where \(k\) is the number of levels. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency.

Cascaded H-bridge inverter has a modularized layout and the problem of the dc link voltage unbalancing does not occur, thus easily expanded to multilevel. Due to these advantages, cascaded H-bridge inverter has been widely applied to such applications as HVDC, SVC, stabilizers, and high power motor drives.

Diode-clamped inverter needs only one dc-bus and the voltage levels are produced by several capacitors in series that divide the dc bus voltage into a set of capacitor voltages. Balancing of the capacitors is very complicated specially at large number of levels. Moreover, three-phase version of this topology is difficult to implement due to the neutral-point balancing problems.

The output waveforms of multilevel inverters are in a stepped form, therefore they have reduced harmonics compared to a square wave inverter. To reduce the harmonics further, carrier-based PWM methods are suggested in the literature [5]. Another approach to reduce the harmonics is to calculate the switching angles in order to eliminate certain low order harmonics. The harmonic elimination problem was formulated as a set of transcendental equations that must be solved to determine the angles in an electrical cycle for turning the switches on and off so as to produce a desired fundamental amplitude while eliminating specific low order harmonics. Available techniques to determine such angles include iterative techniques and resultant theory. Iterative numerical techniques, such as Newton-Raphson [6], method gives only one solution, while the theory of Resultant produces all possible solutions [7]. These sets of solutions have to be examined for its corresponding THD in order to select the set which generate the lowest harmonic distortion.

This paper presents how reduced harmonic distortion is achieved for a new topology of multilevel inverters using programmed PWM technique. This new topology has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. It can also be extended to any number of levels. The modes of operation of a 5-level inverter is presented, where similar modes can be realized for higher levels. The inverter operation is controlled using switching angles based on programmed PWM method. These angles are obtained from solving the waveform equations using the theory of resultants. Simulation of higher levels of the proposed inverter topology is carried out using PSpice. The validity of the proposed topology and the harmonic elimination method are verified experimentally for 5 and 7 level inverters.
II. MULTILEVEL INVERTER NEW TOPOLOGY

In order to reduce the overall number of switching devices in conventional multilevel inverter topologies, a new topology has been proposed. The circuit configuration of the new 5-level inverter is shown in Fig. 1. It has four main switches in H-bridge configuration Q1-Q4, and two auxiliary switches Q5 and Q6. The number of dc sources (two) is kept unchanged as in similar 5-level conventional cascaded H-bridge multilevel inverter. Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Fig. 2. The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, and for the sake of simplicity, the modes of operation will be illustrated for 5-level inverter, these modes are:

**Powering Mode**
This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is $V_{dc}$, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is $2V_{dc}$, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.

**Free-Wheeling Mode**
Free-wheeling modes exist when one of the main witches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.

**Regenerating Mode**
In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vise-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4.

The 7-level version of the proposed topology is shown in Fig. 3, where another dc supply, and two auxiliary switches, Q7 and Q8, are added while keeping the four main switches, Q1-Q4, unchanged. The corresponding output voltage waveform, load current, and gating signals are shown in Fig. 4, where the abovementioned modes of operation can also be realized.

A generalized circuit configuration of the new topology is shown in Fig. 5. The proposed topology has the advantage of the reduced number of power switching devices, but on the expense of the high rating of the main four switches. Therefore, it is recommended for medium power applications.

The percentage reduction in the number of power switches compared to conventional H-bridge multilevel inverter is shown in Table 1.
In order to verify the ability of the proposed multilevel inverter topology to synthesize an output voltage with a desired amplitude and better harmonic spectrum, programmed PWM technique is applied to determine the required switching angles. It has been proved that in order to control the fundamental output voltage and eliminate n harmonics, therefore n+1 equations are needed. Therefore, 7-level inverter, for example, can provide the control of the fundamental component beside the ability to eliminate or control the amplitudes of two harmonics, not necessarily to be consecutive. The method of elimination will be presented for 7-level inverter such that the solution for three angles is achieved.

The Fourier series expansion of the output voltage waveform using fundamental frequency switching scheme shown in Fig. 2 is as follows:

\[
V_o(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s))\sin(n\omega t)
\]

(1)

Where s is the number of dc sources in the multilevel inverter. Ideally, given a desired fundamental voltage V1, one wants to determine the switching angles \(\theta_1, \theta_2, \ldots, \theta_s\) so that \(V_o(\omega t) = V_1\sin(\omega t)\), and a specific higher harmonics of \(V_o(\omega t)\) are equal to zero. The switching angles can be found by solving the following equations:

\[
\begin{align*}
\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) &= m \\
\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) &= 0 \\
\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0
\end{align*}
\]

(2)

Where \(m = V_1/(4V_{dc}/\pi)\), and the modulation index \(m_a\) is given by \(m_a = m/s\), where \(0 \leq m_a \leq 1\).

One approach to solving the set of nonlinear transcendental equations (2), is to use an iterative method such as the Newton-Raphson method [6]. In contrast to iterative methods, the approach here is based on solving polynomial equations using the theory of resultants which produces all possible solutions [7]. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Then the resultant method is employed to find the solutions when they exist. These sets of solutions have to be examined for its corresponding total harmonic distortion (THD) in order to select the set which generate the lowest harmonic distortion (mostly due to the 11th and 13th harmonics). The computed THD in percent is defined by:

<table>
<thead>
<tr>
<th>Inverter type</th>
<th>Number of switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascaded H-bridge</td>
<td>8</td>
</tr>
<tr>
<td>7-level</td>
<td>12</td>
</tr>
<tr>
<td>9-level</td>
<td>16</td>
</tr>
<tr>
<td>11-level</td>
<td>20</td>
</tr>
<tr>
<td>Proposed topology</td>
<td>6</td>
</tr>
<tr>
<td>% Reduction</td>
<td>25%</td>
</tr>
<tr>
<td></td>
<td>33.3%</td>
</tr>
<tr>
<td></td>
<td>37.5%</td>
</tr>
<tr>
<td></td>
<td>40%</td>
</tr>
</tbody>
</table>
Transforming the transcendental equations (2) into polynomial equations using the change of variables:

\[ x_1 = \cos \theta_1, \quad x_2 = \cos \theta_2, \quad x_3 = \cos \theta_3 \]  

(4)

And the trigonometric identities:

\[
\begin{align*}
\cos(3\theta) &= -3\cos \theta + 4\cos^3 \theta \\
\cos(5\theta) &= 5\cos \theta - 20\cos^3 \theta + 16\cos^5 \theta 
\end{align*}
\]

(5)

To transfer (2) into the equivalent conditions:

\[
\begin{aligned}
p_1(x) &= x_1 + x_2 + x_3 - m = 0 \\
p_2(x) &= \sum_{i=1}^{3} (-3x_i + 4x_i^3) = 0 \\
p_3(x) &= \sum_{i=1}^{3} (5x_i - 20x_i^3 + 16x_i^5) = 0
\end{aligned}
\]

(6)

System (6) is a set of three polynomial equations in three unknowns \( x_1, x_2, \) and \( x_3, \) where \( x = (x_1, x_2, x_3) \), and the angles condition must satisfy \( 0 \leq x_i \leq 1 \). Polynomial systems were also considered to compute the solutions of the harmonic elimination equations by iterative numerical methods which give only one solution [9]. In contrast, this system of polynomial equations will be solved using resultant such that all possible solution of (2) can be found. A systematic procedure to do this is known as elimination theory and uses the notion of resultants. The details of this procedure can be found in [9].

IV. COMPUTATIONAL RESULTS

Using the abovementioned technique, the polynomial (6) are solved for all possible solutions (sets of switching angles) for any given value of \( m \). The THD produced by output waveform using each of these sets of switching angles is then computed and the particular solution (set of switching angles) that produces the smallest THD is then chosen. That is, the particular waveform and switching angles are simply dictated by the process of solving the harmonic elimination equations for the solution that produces the lowest THD.

A considerable number of simulation results were obtained for different values of inverter levels. Simulation results for 5-level inverter at \( V_{dc}=50V, \) and \( m_s=0.8 \) (where \( s=2, \) and \( m=1.6) \) are shown in Figs. 6 and 7. To verify the harmonic elimination method, FFT of the inverter output voltage is shown in Fig. 8. Since only two angles are available in 5-level inverter, it is only possible to eliminate the 3rd harmonic and to control the fundamental component by \( m \). For \( m_s=0.8, V_{rms}(4mV_{dc}/\pi)=101.8V. \)

The corresponding simulation results, at the same values of \( V_{dc} \) and \( m_s \) for 7-level inverter are shown in Figs. 9, 10, and 11, where 3 angles are obtained such that the 3rd and 5th harmonics are eliminated and \( V_{rms}=152.78V. \) Note also that the current waveform is improved as a result of the increased number of levels.
V. EXPERIMENTAL VERIFICATION

The proposed multilevel inverter circuits with the described harmonic elimination method have been implemented. The prototype inverters have been built using IRF520 100V-10A MOSFETs as switching devices. A real-time controller based on the available MCB-1A Hampden microprocessor kit is used to implement the harmonic elimination PWM method. The switching angles obtained from solving the polynomial equations, using the theory of resultant, are stored in the form of look-up tables for different values of modulation indices. Then, these switching angles are converted into time-interval switching patterns using a down-counter and some logic operations, and then stored in an in-house EPROM. The switching patterns obtained from the controller are interfaced to the inverter power switches through optocoupler isolators.

In order to verify the presented idea, the hardware implementation is only developed for 5-level and 7-level inverters, where it can be extended to any number of levels with any desired harmonic profile. The gating signals of the proposed 5-level inverter are shown in Fig. 14, while those of the proposed 7-level inverter are shown in Fig. 15, where signals of \( Q_2 \) and \( Q_3 \) (not shown) are similar to those of 5-level inverter. A nominal dc link of 20V is used for dc sources. The 5-level inverter output voltage is shown in Fig. 16 at \( m_a = 0.8 \) (\( m = 1.6 \)). The corresponding FFT is shown in Fig. 17, where a fundamental output voltage of 37V is obtained while the 3\( \text{rd} \) harmonic is eliminated.

Simulation results are extended to 9-level inverter which has four dc sources (\( s=4 \)) as shown in Figs. 12 and 13, where the 3\( \text{rd} \), 5\( \text{th} \), and 7\( \text{th} \) harmonics are eliminated and an output voltage of 203.7V is obtained at \( V_{dc} = 50V \), and \( m_a = 0.8 \).

It can be seen that the experimental results are in close agreement with the simulation results. The THD on simulation and experiments are 1.8% and 2.4% respectively. The THD of the experiments is a little higher than that of the simulation because the control resolution is limited 8\( \mu \)s, and the switches are not ideal. The effective switching frequency of the main four switches is 50Hz, while it is 100Hz for the auxiliary switches.
VI. CONCLUSIONS

A new family of multilevel inverters has been presented. It has the advantage of its reduced number of switching devices compared to conventional similar inverters. However, the high rating of its four main switches limits its usage to the medium voltage range. The modes of operation and switching strategy of the new topology are presented. A programmed PWM algorithm based on the theory of resultant has been applied for harmonic elimination of the new topology. Since the solution algorithm is based on solving polynomial equations, it has the advantage of finding all existed solutions, where the solution produces the lowest THD is selected. Other PWM methods and techniques are also expected to be successively applied to the proposed topology. The simulation results and experimental results show that the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD.

REFERENCES


BIOGRAPHY

Tamer H. Abdelhamid was born in Egypt. Received the B.Sc. and M.Sc. degrees in Electrical Engineering from Alexandria University, Egypt in 1984 and 1989 respectively. In 1995 he received the Ph.D. from Brunel University, England. During the periods 1984 to 1989 and 1989 to 1992 he was demonstrator and assistant teacher at the department of electrical engineering, Alexandria University. In 1996 he joins the same department as a lecturer. Since 2000, he has been with the department of electrical engineering, college of technological studies, Kuwait, where he is presently an assistant professor. His research interests include power factor correction techniques, multilevel inverters, and soft switching techniques.
Switching Algorithms for the Dual Inverter fed Open-end Winding Induction Motor Drive for 3-level Voltage Space Phasor Generation

S. Srinivas\textsuperscript{1} and V.T. Somasekhar\textsuperscript{2}

Abstract – An open-end winding induction motor, fed by two 2-level inverters connected at either end produces space vector locations, identical to those of a conventional 3-level inverter. In this paper, two switching algorithms are proposed to implement space vector PWM for the dual inverter scheme. The proposed algorithms do not employ any look-up tables. The time consuming task of sector identification is altogether avoided in both these algorithms. The proposed algorithms employ only the instantaneous reference phase voltages for the implementation of the space vector PWM. An equal switching duty for both the inverters is also ensured with one of the proposed PWM strategies. Also, it is observed that the zero-sequence voltage in motor phases is significantly reduced with the proposed PWM strategies.

Keywords - Open-end winding induction motor drive, dual-inverter system, V/f control, space vector modulation

I. INTRODUCTION

Three-level inversion has been extensively researched in the past and several circuit topologies were suggested. Of these topologies, the neutral point clamped topology \cite{1}, the flying capacitor topology \cite{2} and the H-bridge topology \cite{3} have become popular. Recently, a circuit configuration to obtain three-level inversion by cascading two 2-level inverters has also been suggested \cite{7}.

Stemmler’s pioneering work has shown that three-level inversion can be achieved by the open-end winding connection of an induction motor with two two-level inverters feeding the motor from either end \cite{4}. In this work \cite{4}, sine-triangular modulation technique is employed for the control of inverters. Various derivatives of this power circuit and/or the associated PWM schemes are also reported in the recent past \cite{6}-\cite{14}. The inverters may be controlled with space vector modulation technique as it improves the DC-bus utilization compared to the sine-triangle modulation technique. A space vector modulation technique for the open-end winding topology has been suggested in \cite{6}. In this work \cite{6}, the implementation of space vector modulation requires sector identification, which is a time consuming task. Further, this switching scheme employs lookup tables, enhancing the memory requirement with a typical Digital implementation.

In this paper, two space vector modulation techniques are suggested, which obviate the need for the sector identification. Also these PWM schemes do not employ any look-up table, thus reducing the memory requirement.

This section gives a general background and review of the paper or work done by other engineers in the field. It should be well supported by citations. Moreover, the citations are served as a guide for those who want to learn more about the field.

Fig.1 shows the basic open-end winding induction motor drive operated with a single power supply. The symbols $v_{do}, v_{go}$ and $v_{co}$ denote the pole voltages of inverter-1. Similarly, the symbols $v_{ce}, v_{ge}$ and $v_{co}$ denote the pole voltages of inverter-2. The space vector locations from individual inverters are shown in Fig.2. The numbers 1 to 8 denote the states assumed by inverter-1 and the numbers 1’ through 8’ denote the states assumed by inverter-2 (Fig.2).

Table-1 summarizes the switching state of the switching devices for both the inverters in all the states. In Table-1, a ‘+’ indicates that the top switch in a leg of a given inverter is turned on and a ‘-’ indicates that the bottom switch in a leg of a given inverter is turned on.

As each inverter is capable of assuming 8 states independently of the other, a total of 64 space vector combinations are possible with this circuit configuration. The space vector locations for all space vector combinations of the two inverters are shown in Fig.3. In Fig.3, $|OA|$ represents the DC-link voltage of individual inverters, and is equal to $V_d/2$ while $|OG|$ represents the DC-link voltage of an equivalent single inverter drive, and is equal to $V_d$.

![Diagram](image)

Fig.1: The primitive open-end winding induction motor drive
Fig. 1 shows the basic open-end winding induction motor drive. It cannot be operated with a single power supply, due to the presence of zero-sequence voltages (common-mode voltages) [5], [6]. Consequently, a high zero-sequence current would flow through the motor phase windings, which is deleterious to the switching devices and the motor itself. To suppress the zero-sequence current in the motor phase windings, each inverter is operated with an isolated dc-power supply as shown in Fig. 4. From the Fig.4, when isolated DC power supplies are used for individual inverters, the zero-sequence current cannot flow as it is denied a path. Consequently, the zero-sequence voltage appears across the points ‘O’ and “O”.

The zero-sequence voltage resulting from each of the 64 space vector combinations is reproduced in Table 2 from [6] to facilitate an easy reference.

In Fig. 5, the vector OT represents the reference vector (also called the reference sample), with its tip situated in sector-7 (Fig.3). This vector is to be synthesized in the average sense by switching the space vector combinations situated in the closest proximity (the combinations situated at the vertices A, G and H in the present case) using the space vector modulation technique. In the work reported in reference [7], the reference vector OT is transformed to OT’ in the core hexagon ABCDEF by using an appropriate coordinate transformation, which shifts the point A to point O. In the core hexagon, the switching timings of the active vectors OA, OB and the switching time of the null vector situated at O to synthesize the transformed reference vector OT’ are evaluated. The switching algorithm described in reference [5] is employed to evaluate these timings. These timings are then employed to produce the actual reference vector OT situated in sector-7 by switching amongst the switching states of the individual inverters.

<table>
<thead>
<tr>
<th>Table 1: Switching states of the individual inverters</th>
</tr>
</thead>
<tbody>
<tr>
<td>State of Inverter-1</td>
</tr>
<tr>
<td>1 (+ - -) S6 S1 S2</td>
</tr>
<tr>
<td>2 (+ + -) S1 S2 S3</td>
</tr>
<tr>
<td>3 (- + -) S2 S3 S4</td>
</tr>
<tr>
<td>4 (- + +) S3 S4 S5</td>
</tr>
<tr>
<td>5 (-- +) S4 S5 S6</td>
</tr>
<tr>
<td>6 (+ - +) S5 S6 S1</td>
</tr>
<tr>
<td>7 (+ + +) S1 S3 S5</td>
</tr>
<tr>
<td>8 (- - -) S2 S4 S6</td>
</tr>
</tbody>
</table>

Table 2: Zero-sequence voltage contributions in the difference of the pole-voltages of individual inverters

<table>
<thead>
<tr>
<th>-Vd/2</th>
<th>-Vd/3</th>
<th>-Vd/6</th>
<th>0</th>
<th>Va/c/6</th>
<th>Vd/3</th>
<th>Vd/2</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 - 5</td>
<td>8 - 6</td>
<td>8 - 7</td>
<td>8 - 8</td>
<td>5 - 1</td>
<td>4 - 8</td>
<td>4 - 8</td>
</tr>
<tr>
<td>8 - 4</td>
<td>8 - 3</td>
<td>8 - 2</td>
<td>8 - 1</td>
<td>5 - 6</td>
<td>6 - 6</td>
<td>7 - 8</td>
</tr>
<tr>
<td>8 - 1</td>
<td>8 - 2</td>
<td>8 - 4</td>
<td>8 - 5</td>
<td>5 - 7</td>
<td>6 - 6</td>
<td>7 - 2</td>
</tr>
<tr>
<td>8 - 7</td>
<td>8 - 8</td>
<td>8 - 9</td>
<td>8 - 10</td>
<td>5 - 6</td>
<td>6 - 7</td>
<td>7 - 2</td>
</tr>
<tr>
<td>8 - 6</td>
<td>8 - 5</td>
<td>8 - 4</td>
<td>8 - 3</td>
<td>5 - 7</td>
<td>6 - 6</td>
<td>7 - 2</td>
</tr>
<tr>
<td>8 - 7</td>
<td>8 - 8</td>
<td>8 - 9</td>
<td>8 - 10</td>
<td>5 - 6</td>
<td>6 - 7</td>
<td>7 - 2</td>
</tr>
</tbody>
</table>
The space vector combinations at the sub-hexagonal center ‘A’ are given by the active vector to which inverter-1 is clamped (in this case to state-1) and the null vectors of inverter-2 (states 8’ and 7’, Table-1) respectively.

4. All the seven locations of a given sub-hexagonal center (i.e. six vertices and the corresponding sub-hexagonal center) show redundancy of space vector combinations. For the sub-hexagon OFSGHB, the space vector combinations for these seven locations may alternatively be obtained by clamping inverter-2 to state 4’(-++) while inverter-1 assumes all the eight states.

5. Of the 20 space vector combinations with a common-mode voltage contribution of zero, 8 are located at the origin O (Table-2, Fig.3). Therefore, any PWM strategy that makes a good use of these states is expected to cause a reduction in the zero-sequence voltages, in the difference of the pole-voltages of respective inverters.

The following PWM strategies are proposed in this paper:
- The Decoupled PWM strategy
- The Biasing inverter PWM strategy

III. THE DECOUPLED PWM STRATEGY

This PWM strategy is based on the fact that the reference voltage space vector $V_r$ can be synthesized with two equal and opposite components $V_r/2$ and $-V_r/2$, by subtracting the latter component from the former. It is also based on the observation that the effect of applying a vector with inverter-1 while inverter-2 assumes a null state is the same as that of applying the opposite vector with inverter-2 while inverter-1 assumes a null state. Figure 6 shows the method of this PWM strategy. It is worth noting that the phase axes of the motor viewed with reference to individual inverters are in phase opposition.

In Fig.6, the vector $OT$ represents the actual reference voltage space vector that is to be synthesized from the dual-inverter system and is given by $V_r \angle \alpha$. This vector is resolved into two equal and opposite components $OT_1 (V_r/2 \angle \alpha)$ and $OT_2 (V_r/2 \angle 180^\circ + \alpha)$. The vector $OT_1$ is synthesized by inverter-1 in the average sense by switching amongst the states (8-1-2-7) while the vector $OT_2$ is reconstructed by inverter-2 in the average sense by switching amongst the states (8'-5'-4'-7').

The basic switching algorithm described in reference [5] for the classical case of a 2-level inverter feeding an ordinary induction motor is extended for the dual-inverter system to compute the switching timings for individual inverters.

These two strategies are described in detail in the following sub-sections.

This algorithm [5] uses only the instantaneous phase reference voltages and is based on the concept of ‘effective time’. The effective time is defined as the time combinations available at the vertices A, G and H. The latter step requires a lookup table in which the space vector combinations available at each space vector location are stored.

Thus, it is evident that with this switching algorithm, the controller negotiates a considerable computational burden primarily because of sector identification and coordinate transformation. Also, there is a need requirement for look-up tables, enhancing the memory requirement. Further, the zero-sequence voltage in the difference of the respective pole voltages of individual inverters (which is dropped across the points ‘O’ and ‘O’” in Fig.4) is also high with this PWM scheme.

II. PROPOSED PWM STRATEGIES

The proposed PWM strategies are based on the following observations:

1. The resultant space vector locations in the dual-inverter scheme (Fig.3) are obtained by superposing the space vector locations resulting from inverter-2 (i.e. by superposing the center of the right hexagon, Fig.2) at each space vector location caused by inverter-1 (left hexagon, Fig.2). Alternatively, the space vector locations of the resulting dual inverter scheme may be obtained by superposing the center of the left hexagon at each of the space vector locations of the right hexagon.

2. Apart from the core hexagon ABCDEF centered around O, there exist six outer sub-hexagons namely OBGHSF, OCJHBA, ODLKJB, OENMLC, OFQPND and OASRQE centered around the points A, B, C, D, E and F respectively. For the rest of this paper, they are referred to as sub-hexagonal centers.

3. The space vector combinations at the vertices and at the center of a given sub-hexagon are obtained by clamping one inverter to a given state while the other inverter assumes all the eight states. For example, the space vector combinations at the vertices of the sub-hexagon OFSGHB (centered around the point ‘A’, Fig.3), are obtained by clamping inverter-1 to the state of 1(+-), while inverter-2 assumes the states 1’ to 6’ respectively.
In the context of a dual inverter drive, there exist two sets of phase switching times, one for each inverter. The procedure is adopted for all the other sectors. Sector-1 is pictorially depicted in Fig.7. A similar pulses for the individual devices using this algorithm in switching times. The procedure to generate the gating timing is instantaneous reference phase voltages of the reference vector. Phase reference voltages are obtained by projecting the tip of the reference vector \( V_{ref} \) on to the respective phase axis and multiplying the values of these projections with a factor of \( (2/3) \). These instantaneous phase reference voltages are denoted as \( v_{a}, v_{b}, \) and \( v_{c} \). This algorithm accomplishes the automatic generation of the gating pulses for the individual switching devices while placing the effective time exactly at the center of a given sampling period. The symbols \( T_{ga} \), \( T_{gb} \) and \( T_{gc} \) respectively denote the time duration for which a given motor phase is connected to the positive rail of the input DC power supply of the inverter in the given sampling time period \( T_s \). The timings \( T_{ga} \), \( T_{gb} \) and \( T_{gc} \) are termed as the phase switching times. The procedure to generate the gating pulses for the individual devices using this algorithm in sector-1 is pictorially depicted in Fig.7. A similar procedure is adopted for all the other sectors.

In the context of a dual inverter drive, there exist two sets of phase switching times, one for each inverter. The timings \( T_{ga}, T_{gb}, \) and \( T_{gc} \) correspond to inverter-1 while the timings \( T_{ga}', T_{gb}', \) and \( T_{gc}' \) correspond to inverter-2. The instantaneous reference phase voltages \( v_{a}, v_{b}', \) and \( v_{c}' \) correspond to the actual reference space vector \( V_{ref} \) of the dual-inverter system. As individual inverters operate with the references \( V_{ref}/2 \) and \( -V_{ref}/2 \) respectively, it follows that the corresponding phase references are given by, \( v_{a}/2 \), \( v_{b}/2 \) and \( v_{c}/2 \) for inverter-1 and \( -v_{a}/2 \), \( -v_{b}/2 \) and \( -v_{c}/2 \) for inverter-2. These references are then employed to determine the phase switching timings of each inverter using the aforementioned switching algorithm [8]. It can be shown mathematically that the phase switching times of the inverters are related by (the proof of this result is presented in appendix-A):

\[
T_{ga} = T_s - T_{go} \quad T_{gb} = T_s - T_{go} \quad T_{gc} = T_s - T_{go}
\]

Thus, the phase switching timings need not be exclusively computed for inverter-2. Both inverters are operated with the same sequence so that the null vector combinations are 88’ and 77’. From table-1, it may be noted that these two combinations result in the zero-sequence voltage that is zero. If one inverter is operated with on-sequence and the other with off-sequence, the null vector combinations would be 87’ and 78’. From table-2 it is evident that the zero-sequence voltage of the difference of the pole-voltages is maximum for these two combinations. It is interesting to note that this zero-sequence voltage is much lesser with this algorithm than the lookup table approach used in [6]. This is because the combinations 87’ and 78’ are used extensively with that approach [6]. The merit of the coupled control is that there is no computational burden on the controller and is therefore amenable to be used with slower controllers (processors) and possibly the reduced zero-sequence voltage in the difference of pole-voltages. However, in this approach, both inverters are to be switched.

IV. EXPERIMENTAL VERIFICATION FOR THE DECOUPLED PWM STRATEGY

The performance of the dual-inverter scheme is first evaluated with simulation studies using MATLAB and the induction motor is operated with the V/f control scheme. The experiment is performed on a 1 H.P. open-end winding induction motor with V/f control and the gating signals to the dual-inverter are generated with TMS320F240 Digital Signal Processor. A fixed number of samples (48) are employed for the implementation of the space vector modulation per cycle in the entire range of operation. This means that the sampling time period is a variable quantity. In the present case, the number of samples used per cycle is 48. This means that the angular displacement between successive samples is \( 7.5^\circ \) (360°/48). Fig.8 shows a typical sample. This is the 4th sample from the beginning of the cycle and occurs at \( \alpha = 22.5^\circ \) (Fig.6). The modulation index, denoted as ‘m,’ is given by \( \frac{V_m}{V_{ref}} \).

It may be noted from Fig.8 that \( T_{ga} + T_{ga}' = T_s \) as mentioned earlier. Therefore, the phase timings for inverter-2 need not be evaluated separately. They are obtained simply by subtracting the timings of the corresponding phases from \( T_s \).
For example, the normalized third harmonic component is about 1.4 p.u. with the strategy adopted in [7], while it is only about 0.2 p.u. (Fig.16) with the decoupled control of the dual-inverter scheme for the same modulation index of \(m_i=0.4\). It may be noted from Fig.16 that, apart from the fundamental, the 47th and the 49th harmonics are dominant as the sampling frequency is 48 times the frequency of the fundamental component. The corresponding waveforms for a modulation index of \(m_i=0.7\) are shown through Fig.18 to Fig.25.

Figures 16 and 17 respectively shows the normalized harmonic spectra of the difference in pole voltages and actual motor phase voltage presented in Fig.12 and 13. It is seen from Fig.16 that the zero-sequence voltage in the difference of pole voltages is significantly reduced compared with the strategy adopted in [7].
Fig. 12: The difference of pole voltages of individual inverters for $m_i = 0.4$.

Fig. 13: Simulated (top) & experimentally obtained result (bottom) of the actual motor phase voltage for $m_i = 0.4$.

Fig. 14: Simulated (top) & experimentally obtained result (bottom) of the common-mode voltage for $m_i = 0.4$.

Fig. 15: Experimentally obtained motor phase current at no-load for $m_i = 0.4$.

Fig. 16: The normalized harmonic spectrum of the difference of pole voltages for $m_i = 0.4$.

Fig. 17: The normalized harmonic spectrum of the actual motor phase voltage for $m_i = 0.4$. 
Fig. 18: Gating signals and the difference of pole-voltages derived as the difference of two gate signals of top switch of the a-phase legs of the two inverters for \( m_i = 0.7 \)

Fig. 19: Simulated (top) & experimentally obtained result (bottom) of Pole voltage of inverter-1 for \( m_i = 0.7 \)

Fig. 20: Simulated (top) & experimentally obtained result (bottom) of Pole voltage of inverter-2 for \( m_i = 0.7 \)

Fig. 21: The difference of pole voltages of individual inverters for \( m_i = 0.7 \)

Fig. 22: Simulated (top) & experimentally obtained result (bottom) of the common-mode voltage for \( m_i = 0.7 \)
V. THE BIASING INVERTER PWM STRATEGY

This PWM strategy is based on the observation that the space vector combinations at the vertices and the center of a given sub-hexagon are obtained by clamping one inverter with an active state, while the other inverter assumes all the eight states. Consequently, one inverter may be employed as the biasing inverter to realize the biasing vector and the other inverter may be switched around this biasing vector. Figure 26 shows the basic operating principle of this PWM strategy.

In Fig 26, OT represents the reference vector with its tip situated in sector-7. It is resolved into two components OA and AT. The vector OA may be output with inverter-1 with its state clamped at 1(+--, Table-1) throughout the sampling time interval. The vector AT is realized in the average sense by switching inverter-2 around the sub-hexagonal center, A. Alternatively, the biasing vector OA may be output with inverter-2 with its state clamped at 4'(+-, Table-1) throughout the sampling time interval. In that case, the switching vector AT is generated with inverter-1.

The instantaneous phase references denoted by, \( v_a, v_b, v_c \) corresponding to the reference vector OT are obtained by projecting its tip on to the respective phase axes and multiplying the values of these projections (OU, OV and OW, Fig.26) with a factor of (2/3). The symbols \( v'_a, v'_b \) and \( v'_c \) respectively denote the components of OT on the \( \alpha \)- and the \( \beta \)- axes (OU and OX, Fig.26). The modified instantaneous voltage phase references corresponding to the switching vector AT are denoted by, \( v'_a, v'_b \) and \( v'_c \) are obtained by the following procedure:

1. The instantaneous phase references \( v'_a, v'_b, v'_c \) corresponding to the reference vector OT are transformed into the corresponding equivalent two-phase system references \( v'_\alpha \) and \( v'_\beta \) using the classical three phase to two phase transformation given by:

\[
\begin{bmatrix}
  v'_\alpha \\
  v'_\beta
\end{bmatrix} = \frac{3}{2} \begin{bmatrix}
  0 & 0 \\
  \sqrt{3} & -\sqrt{3}
\end{bmatrix} \begin{bmatrix}
  v_a \\
  v_b \\
  v_c
\end{bmatrix}
\]
2. The sub-hexagonal center situated nearest to the tip of the reference vector $\mathbf{OT}$ is then determined.

3. The coordinates of the nearest sub-hexagonal center in the $v_a - v_p$ plane (the point ‘A’ in this example, Fig.26), denoted as $v_{a,sub}$ and $v_{p,sub}$ are known for all the six sub-hexagonal centers. For example, the coordinates of the point ‘A’ in the $v_a - v_p$ plane are given by $(V_{dc}/2,0)$.

4. Since the vector $\mathbf{OA}$ is output by the biasing inverter, the coordinates of the switching vector (AT in the present case) denoted as $V_{a,sw}$ and $V_{p,sw}$ are given by:

$$V_{a,sw} = v_a - v_{a,sub} \quad \text{and} \quad V_{p,sw} = v_p - v_{p,sub}$$

5. The modified reference phase voltages $v_a$, $v_b$ and $v_c$ for the switching inverter are then obtained by transforming $V_{a,sw}$, $V_{p,sw}$ into the corresponding three phase variables by using the classical two phase — three phase transformation given by:

$$
\begin{bmatrix}
  v_a \\
  v_b \\
  v_c \\
\end{bmatrix} =
\begin{bmatrix}
  2/3 & 0 & -1/3 \\
  0 & 1/\sqrt{3} & 1/\sqrt{3} \\
 -1/3 & 1/\sqrt{3} & -1/3 \\
\end{bmatrix}
\begin{bmatrix}
  V_{a,sw} \\
  V_{b,sw} \\
\end{bmatrix}
$$

6. If inverter-2 is employed as the biasing inverter, the modified references are used directly to generate the switching vector AT with inverter-1. On the other hand, if inverter-1 is used as the biasing inverter, it is obvious that the modified references must be negated to generate the switching vector AT with inverter-2.

The principal advantage with this PWM strategy is that the inverter switching is significantly reduced as one inverter switches only six times, while the other switches for 48 times. With decoupled control both inverters are switched in all the 48 samples.

It is important to note that the most important part of this algorithm is to find the nearest sub-hexagonal center to the tip of the reference vector $\mathbf{OT}$ (Fig.26). Fig.27 and Fig.28 explain the method to determine the same. In the discussion to follow, the symbol ‘0’ denotes the angle subtended by the tip of the reference voltage space vector with respect to an instant where the instantaneous value of the A-phase reference voltage is zero. Fig.27 shows various values of ‘0’ corresponding to the positive and the negative zero crossings of the reference phase voltages in the $V_a - V_p$ plane. From Fig.27, it may be noted that if $0^\circ \leq \theta \leq 60^\circ$, the tip of $V_a$ is situated in the quadrangle OSQR. It may also be seen that ‘F’ is the nearest sub-hexagonal center for this condition. Should the tip of the reference vector be situated within the quadrangle OSGH, ‘A’ is the nearest sub-hexagonal center to it. Similar observations may be made for the rest of the sub-hexagonal centers. It is desirable to identify the nearest sub-hexagonal center directly from the instantaneous phase references without having to evaluate $V_a$ and there by the value of ‘0’, as it would be very time consuming.

The instantaneous phase reference voltages $v_a$, $v_b$ and $v_c$ (solid lines) normalized w.r.t $V_a'$ and their respective negations (dotted lines) are shown in Fig.28. From Fig.28 it may be noted that $v_a'$ is the most positive quantity amongst these six quantities when $60^\circ \leq \theta \leq 120^\circ$ and ‘A’ is the nearest sub-hexagonal center as recognized by Fig.27. Similarly $v_b'$ is the most positive quantity amongst these six when $240^\circ \leq \theta \leq 300^\circ$ and ‘D’ is the nearest sub-hexagonal center. Fig.27 also reinforces this fact. Thus, it is clear that by finding the maximum value amongst these six quantities, one can determine the nearest sub-hexagonal center.

![Fig.27: Zero crossing of the instantaneous phase voltages corresponding to the reference voltage space vector](image)

![Fig.28: Recognition of the nearest sub-hexagonal center with instantaneous reference quantities](image)

VI. EXPERIMENTAL VERIFICATION FOR BIASING INVERTER

PWM STRATEGY:

The top traces of Fig.29 show the gating signals of the top devices of the A-phase legs of the individual inverters for $m_i = 0.4$. In this case, the samples of the reference vector always lie within the core hexagon ABCDEF. The bottom trace of the same figure shows the difference of the two pole voltages. Figures 30 and 31 show the respective pole voltages (both simulated & experimental results) of the
individual inverters with this PWM strategy. From these two figures, it is evident that the switching of inverter-1 is drastically reduced as it is made to operate as the biasing inverter for all samples in a cycle. However, the switching of inverter-2 remains unaltered as it is used as the switching inverter for all the samples in a cycle. Figure 32 shows the difference of the pole voltages, while Fig.33 shows the actual motor phase voltage (obtained after the subtraction of the zero-sequence voltage from the waveform shown in Fig.34). In this case, the phase voltage waveform is similar to the one obtained by a conventional two-level inverter. However, the switching ripple with the open-end winding configuration is much lesser compared to the one obtained with a two-level inverter. This is because; the space vector locations situated at the closest proximity are switched with open-end winding drive. Specifically, if the sample is situated in sector-1, the vertices ‘O’, ‘A’ and ‘B’ are switched, unlike in a two-level inverter, where the location ‘O’, ‘G’ and ‘I’ are switched to construct the same sample (Fig.3). Fig.34 shows the simulated and experimentally obtained results of the zero-sequence voltage. Figures 35 and 36 respectively show the harmonic spectra of the difference in pole voltages (shown in Fig.32) and the actual motor phase voltage (shown in Fig.34). Figure 37 shows the experimentally obtained motor phase current at no-load for the same $m_i$ of 0.4.

The corresponding waveforms for a modulation index of $m_i=0.7$ are shown through Fig.38 to Fig.45. In this case, the tip of the reference vector traverses through the outer sectors i.e. 7 to 24. It is also evident that the phase voltage waveform is similar to the one obtained in a 3-level inverter, as the nearest vertices are switched to synthesize the sample.

With this PWM strategy, the space vector combinations-11', 22', 33', 44', 55' and 66' are exclusively employed, whenever the location ‘O’ is switched. It is worth noting that with this PWM strategy, the location ‘O’ is employed as an ‘active’ location while the sub-hexagonal centers constitute the ‘null’ locations as switching is performed around them. From table-2, it may be observed that these combinations result in a zero-sequence voltage that is zero. In contrast, the PWM strategy proposed in [6] employs the location ‘O’ as a ‘null’ location. Whenever the location ‘O’ is switched with this PWM strategy [6], the combinations 87' and 78' are used. From table-2, it may be noted that these two combinations result in maximum zero-sequence voltages, particularly for low modulation indices wherein the dwell time associated with the ‘null’ vector location ‘O’ is more. Thus, a significant reduction in the zero-sequence voltage in the difference of pole voltages is possible with the PWM strategy proposed in this paper. For a modulation of 40%, the zero-sequence voltage resulting with the strategy adopted in [6] is about 1.4 p.u., while with the biasing inverter strategy it is 0.4 p.u. for the same modulation depth. The normalized harmonics spectra of the difference of a-phase pole voltages of the two inverters with the PWM scheme adopted in the earlier work reported [6], and using the two PWM schemes proposed in this paper i.e. Decoupled PWM scheme and Biasing Inverter PWM scheme for different modulation indices are shown in Fig.46.
Fig. 31: Simulated (top) & experimentally obtained result (bottom) of Pole voltage of inverter-2 for $m_i = 0.4$

Fig. 32: The difference of pole voltages of individual inverters for $m_i = 0.4$

Fig. 33: Simulated (top) & experimentally obtained result (bottom) of the actual motor phase voltage for $m_i = 0.4$

Fig. 34: Simulated (top) & experimentally obtained result (bottom) of the common-mode voltage for $m_i = 0.4$

Fig. 35: Normalized harmonic spectrum of the difference of the pole voltages for $m_i = 0.4$

Fig. 36: Normalized harmonic spectrum of the motor phase voltage for $m_i = 0.4$
Fig. 37: Experimentally obtained motor phase current at no-load for $m_i = 0.4$

Fig. 38: Gating signals and the difference of pole-voltages derived as the difference of two gate signals of top switch of the a-phase legs of the two inverters for $m_i = 0.7$

Fig. 39: Simulated (top) & experimentally obtained result (bottom) of Pole voltage of inverter-1 for $m_i = 0.7$

Fig. 40: Simulated (top) & experimentally obtained result (bottom) of Pole voltage of inverter-2 for $m_i = 0.7$

Fig. 41: The difference of pole voltages of individual inverters for $m_i = 0.7$
Fig. 42: Simulated (top) & experimentally obtained result (bottom) of the common-mode voltage for \( m_i = 0.7 \)

Fig. 43: Simulated (top) & experimentally obtained result (bottom) of the actual motor phase voltage for \( m_i = 0.7 \)

Fig. 44: Normalized harmonic spectrum of the difference of the pole voltages for \( m_i = 0.7 \)

VII. CONCLUSIONS

Comparing the resultant motor phase voltages with the two PWM strategies proposed in this paper, (Fig.23 and Fig.43) it is clear that it is possible to synthesize a conventional three-level inverter waveform with the biasing inverter PWM strategy. With the biasing inverter PWM strategy the reference space vector is reproduced in the average sense by switching amongst the vector combinations available at the nearest three vertices. Consequently the switching ripple with this strategy is lesser than the decoupled PWM strategy. From the harmonic spectra of the resultant motor phase voltage with these two strategies (Fig.17 and Fig.29), it is seen that the distribution of harmonic energy is better with the biasing inverter PWM strategy. However, as pointed out earlier, the principal advantage with the decoupled PWM algorithm is its fastness and its amenability of implementation with slower controllers. It is interesting to note that the PWM strategies proposed in this paper result in a significant reduction in the zero-sequence voltage in the difference of pole-voltages compared to the look-up table approach proposed in [6] at lower indices of modulation, which could be desirable. Both strategies obviate the time consuming process of sector identification and the coordinate transformations. Look-up tables are not needed with the proposed PWM strategies, reducing the memory requirements of the controller.

REFERENCES

When the reference vector is situated in sector-1, the imaginary switching times [5] for inverter-1 and inverter-2 are related to the respective phase reference voltages as follows:

\[ T_{as} = 2\left(\frac{T_{dc}}{v_a}\right)v^* \]

\[ T_{bs} = 2\left(\frac{T_{dc}}{v_b}\right)v^* \]

\[ T_{cs} = 2\left(\frac{T_{dc}}{v_c}\right)v^* \]

\[ T'_{as} = -2\left(\frac{T_{dc}}{v_a}\right)v^* \]

\[ T'_{bs} = -2\left(\frac{T_{dc}}{v_b}\right)v^* \]

\[ T'_{cs} = -2\left(\frac{T_{dc}}{v_c}\right)v^* \]

When the reference vector is situated in sector-1, For Inverter-1:

\[ T_{\max} = T_{as} \]

\[ T_{\min} = T_{CS} \]

\[ T'_{\max} = T'_{as} \]

\[ T'_{\min} = T'_{CS} \]

\[ T_{eff} = T_{\max} - T_{\min} \]

Similarly for Inverter-2:

\[ T'_{eff} = T_{CS} - T_{cs} \]

Using equations (1), (2) & (3), we have

\[ T_{eff} = 2\left(\frac{T_{dc}}{v_a}\right)(v^*_a - v^*_c) \]

When the reference vector is situated in sector-2, For Inverter-1:

\[ T_{\max} = T_{as} \]

\[ T_{\min} = T_{CS} \]

\[ T'_{\max} = T'_{as} \]

\[ T'_{\min} = T'_{CS} \]

\[ T_{eff} = T_{\max} - T_{\min} \]

Similarly for Inverter-2:

\[ T'_{eff} = T_{CS} - T_{cs} \]

Using equations (4), (5) & (6), we have

\[ T_{eff} = 2\left(\frac{T_{dc}}{v_a}\right)(v^*_a - v^*_c) \]
It is obvious that the effective-time period for inverter-1 and inverter-2 are equal, as the reference vector is resolved into two equal halves.

From equations (7) & (8), we have
\[ T_{\text{eff}} = T'_{\text{eff}} \]  \tag{9}

\[ T_o = T_s - T_{\text{eff}} \quad \text{&} \quad T'_o = T_s - T'_{\text{eff}} \quad [5] \]

\[ \Rightarrow T_o = T'_o \quad [\text{from eqn.}(9)] \]

It was shown in [5] that the time-offset required to place the effective time period at the centre of the sampling time interval is given by:
\[ T_{\text{offset}} = \frac{T_o}{2} - T_{\text{min}} \]

Hence for inverter-1, the time-offset is:
\[ T_{\text{offset}} = \frac{T_o}{2} - 2\left(\frac{T_s}{V_{\text{dc}}}\right)v^*_c \]

\[ T'_{\text{offset}} = \frac{T_o}{2} - T_{\text{min}} \]

Similarly,
\[ = \frac{T_o}{2} + 2\left(\frac{T_s}{V_{\text{dc}}}\right)v^*_a \]

From the algorithm proposed in [5], the phase switching time for phase-A for inverter-1 is given by:
\[ T_{\text{ga}} = T_{\text{as}} + T_{\text{offset}} \]

\[ = 2\left(\frac{T_s}{V_{\text{dc}}}\right)v^*_a + \frac{T_o}{2} - 2\left(\frac{T_s}{V_{\text{dc}}}\right)v^*_c \]

\[ \therefore T_{\text{ga}} = \frac{T_o}{2} + 2\left(\frac{T_s}{V_{dc}}\right)(v^*_a - v^*_c) \quad \tag{11} \]

Similarly for inverter-2,
\[ T_{\text{ga}} = T'_{\text{as}} + T'_{\text{offset}} \]

\[ = -2\left(\frac{T_s}{V_{\text{dc}}}\right)v^*_a + \frac{T_o}{2} + 2\left(\frac{T_s}{V_{\text{dc}}}\right)v^*_a \]

\[ \therefore T'_{\text{ga}} = \frac{T_o}{2} \quad \tag{12} \]

From equations (11) & (12), it is evident that
\[ T_{\text{ga}} + T'_{\text{ga}} = T_o + 2\left(\frac{T_s}{V_{\text{dc}}}(v^*_a - v^*_c) \right) \]

From eqn.7,
\[ T_{\text{ga}} + T'_{\text{ga}} = T_o + T_{\text{eff}} = T_s \]

\[ \therefore T_{\text{ga}} = T_s - T_{\text{gb}} \]

Similarly, the phase switching times for the other two phases are given as:
\[ T'_{\text{gb}} = T_s - T_{\text{ge}} \]

\[ T'_{\text{ge}} = T_s - T_{\text{gc}} \]

**BIographies**

S. Srinivas received the B.E degree in Electrical Engineering from Osmania University College of Engineering and his Masters degree from Regional Engineering College-Warangal in 1997 and 2002 respectively.

He is currently working towards the Ph.D degree at National Institute of Technology-Warangal.

He joined the Faculty of Electrical Engineering National Institute of Technology-Warangal in the year 1997.

His research interests are multi-level inverters, PWM Switching Strategies, Multi-level inversion realized through Open-end winding Induction motor drives, AC drives etc.

Dr. V.T. Somasekhar received his graduate degree from Regional Engineering College Warangal (presently the National Institute of Technology) in 1988 and the post graduate degree from the Indian Institute of Technology, Bombay in 1990, his area of specialization being Power Electronics.

He worked as an R&D engineer at M/s Perpetual Power Technologies, Bangalore and as a senior engineer at M/s Kirloskar Electric Co. Ltd., Mysore. He joined the faculty of electrical engineering at the National Institute of Technology in 1993, where he is currently serving. He received his doctoral degree from the Indian Institute of Science in 2003. His current interests are multilevel inversion with open-end induction motors, AC drives and PWM strategies.
Neuro-Fuzzy Controller for a Non Linear Power Electronic Buck & Boost Converters

S. Joseph Jawhar¹, N.S. Marimuthu², S.K Pillai³ and N. Albert Singh⁴

Abstract – This paper describes the design and development of a novel controller for a non-linear power electronic converter. Neuro-Fuzzy controller is proposed to improve the performance of the buck & boost converters. The duty cycle of the buck & boost converters are controlled by Neuro-Fuzzy controller. The conventional PI controllers for such converters, designed under the worst case condition of maximum load and minimum line condition, present a lower loop bandwidth, and the system response is sluggish. The common bottleneck in fuzzy logic is the derivation of fuzzy rules and the parameter tuning for the controller. The Neural Networks have powerful learning abilities, optimization abilities and adaptation. The Fuzzy logic and Neural Networks can be integrated to form a connectionist adaptive network based Fuzzy logic controller. This integrated adaptive system modifies the characteristics of rules and the structure of the control system so that the proposed controller is adaptive for all operating conditions. This paper aims to establish the superior performance of Neuro-Fuzzy controller over the conventional PI controllers and Fuzzy controllers at various operating points of the buck & boost converters.

Keywords - ANFIS, DC-DC converter, FLC, ANN, AI.

I. INTRODUCTION

Traditional frequency domain methods for design of controllers for power converters are based on small signal model of the converter. The small signal model of the converter has restricted validity and changes due to changes in operating point. Also the models are not sufficient to represent systems with strong non-linearity. Moreover the performance of the controllers designed by frequency domain methods is dependent on the operating point, the parasitic elements of the system, and the load and line conditions. Good large signal stability can be achieved only by decreasing the bandwidth, resulting in slow dynamics. A state space averaged model of the classical buck & boost DC/DC converters suffers from the well known problem of Right-Half-Plane zero in its control to output transfer function under continuous conduction mode. The movement of the zero on the complex S-plane as the operating point changes further compounds the problem.

Designers are generally forced to limit the overall closed loop bandwidth to be much less than the corner frequency due to the worst case right half plane zero location. As a result of this, the system has a sluggish small signal response and a poor large signal response. There are two possible routes to achieve fast dynamic response. One way is to develop a more accurate non-linear model of the converter based on which the controller is designed. The other way is the artificial intelligence way of using human experience in decision-making. Among the various techniques of artificial intelligence, the most popular and widely used technique in control systems is the Neuro-fuzzy logic. Several researchers have contributed in evolving such artificial intelligent (AI) controllers for the buck converters[1],[2]. Among the various techniques of artificial intelligence, the most popular and widely used technique in control systems is the Neuro-fuzzy logic. In recent years fuzzy logic control (FLC) has emerged as one of the practical solution when the process is too complex and non-linear for analysis by conventional quantitative techniques[3],[4]. However the development of a fuzzy controller has to rely on the experience of the experts for deriving effective fuzzy control rules. Recently there has been an increasing use of artificial neural networks (ANNs) for various applications particularly because of their capability for learning from examples and adaptation. This paper aims to establish the superior performance of Neuro-fuzzy controllers at various operating points of the buck & boost converters. The basic concept of Neuro-Fuzzy control method [5] is first to use structure-learning algorithm to find appropriate Fuzzy logic rules and then use parameter-learning algorithm to fine-tune the membership function and other parameters. The proposed controller reveals that it is adaptive for all operating conditions. Simulation results are shown and settling time and peak overshoot have been used to measure the performance.

II. LINEARIZED MODEL FOR BUCK CONVERTER

Rigorous determination of the stability and the control characteristics of power electronic converters require solving the non-linear model. Linearization of the non-linear model greatly simplifies analysis. Linearized model approximately describe small deviations or perturbations from nominal operation of the system.

A. Deriving the small signal model of the converter

The buck converter in Fig. 1, when operating in continuous conduction mode, switches between these two linear states, depending on the state of the switch ‘S’[6]. The first step in the design of controller for such a bi-linear system is to obtain its control-to-output transfer function. Using the state space averaging technique, the control-to-output transfer function of the classical buck converter operating in continuous conduction mode can be obtained as in [7],[8]. The transfer function shows a right-
half-plane zero, which moves with the operating point in the s-plane.

\[
\frac{V_o(s)}{D(s)} = \frac{V_s}{s^2 + s/RC + 1/LC}
\]

where \(D\) = duty ratio at the operating point, \(V_s\) = supply voltage, \(L\) = filter inductor, \(C\) = filter (output) capacitor, \(V_o\) = output voltage, \(R\) = load resistor.

It can be seen from (1) that the control-to-output transfer function is dependent on the operating point and its validity is limited to in and around the operating point. As the operating region of the converter is wide, the conventional way of designing the controllers involves selecting the worst case operating point i.e. under the minimum line and maximum load conditions. The transfer function of the converter under the worse case conditions is taken as the base in the design of the controller.

**B. Control requirements**

The control specifications of the converter are
1. Steady state error
2. Settling time and allowable transient overshoot

In frequency domain terms, the steady state error is related to the dc loop gain. Thus the higher the open loop dc gain, the lower will be the steady state error.

This section gives a general background and review of the paper or work done by other engineers in the field. It should be well supported by citations. Moreover, the citations are served as a guide for those who want to learn more about the field.

**III LINEARIZED MODEL FOR BOOST CONVERTER**

Rigorous determination of the stability and the control characteristics of power electronic converters require solving the non-linear model. Linearization of the non-linear model greatly simplifies analysis. Linearized model approximately describe small deviations or perturbations from nominal operation of the system.

**A. Deriving the small signal model of the converter**

The boost converter in Fig. 2, when operating in continuous conduction mode, switches between these two linear states, depending on the state of the switch ‘S’. The first step in the design of controller for such a bi-linear system is to obtain its control-to-output transfer function. Using the state space averaging technique, the control-to-output transfer function of the classical boost converter operating in continuous conduction mode can be obtained as in [7],[8]. The transfer function shows a right-half-plane zero, which moves with the operating point in the s-plane.

\[
\frac{V_o(s)}{D(s)} = \frac{V_s}{(1-D)s^2 + s/L + 1/LC/(1-D)\cdot s^2}
\]

where \(D\) = duty ratio at the operating point, \(V_s\) = supply voltage, \(L\) = filter inductor, \(C\) = filter (output) capacitor, \(V_o\) = output voltage, \(R\) = load resistor.

It can be seen from (2) that the control-to-output transfer function is dependent on the operating point and its validity is limited to in and around the operating point. As the operating region of the converter is wide, the conventional way of designing the controllers involves selecting the worst case operating point i.e. under the minimum line and maximum load conditions[9]. The transfer function of the converter under the worse case conditions is taken as the base in the design of the controller.

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1. Steady state error
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**IV. DESIGN PROCEDURE**

Neuro-Fuzzy controller is designed based on an average state space model of the classical buck & boost DC-DC
converters. The design of Neuro Fuzzy controller needs a good knowledge of the system operation (fig.4). The various steps involved in the design of Neuro Fuzzy controller for power converter are stated below. A universal Sugeno type Neuro Fuzzy controller has been simulated for the buck converter.

A. Identification of inputs and outputs:

This step in the design identifies the key inputs that affect the system performance. The goal of the designer is to ensure that the output voltage matches the reference voltage. The inputs to the Neuro Fuzzy controller are

i. The voltage error.

ii. The change of voltage error.

Some controllers even may use more information in the form of inductor current. The voltage error input is sampled once in every cycle.

The output of the controller is the incremental control action i.e. the incremental duty ratio.

B. Fuzzifying the inputs and outputs:

The universe of discourse of the inputs is divided into seven fuzzy sets of triangular shapes (fig.3). Outputs are also mapped into several fuzzy regions of several singletons.

\[
O_{1,i} = \max \left( \min \left( \frac{x-a}{b-a}, \frac{c-x}{c-b} \right), 0 \right), \quad i=1\ldots7. \quad (3)
\]

where the parameters \(a\) and \(c\) locate the “feet” of the triangle and the parameter \(b\) locates the peak of the fuzzy set, \(x\) is the input to the node \(i\).

Layer 2:

Every node in this layer (fig.3) represents the firing strength of the rule.

\[
O_{2,i} = w_i = \min \left( u_{A_i}(x), u_{B_i}(y) \right), \quad i=1\ldots7. \quad (4)
\]

Eventually the nodes of this layer perform fuzzy AND operation.

Layer 3:

The nodes of this layer calculate the normalized firing strength of each rule.

\[
O_{3,i} = w_i = w_i / \sum w_i, \quad i=1\ldots7. \quad (5)
\]

\(w_i\) – firing strength of a rule.

Layer 4:

The nodes in this layer output the weighted consequent part of the rule table.

\[
O_{4,i} = w_i f_i = w_i (p_i x + q_i y + r_i), \quad i=1\ldots7. \quad (6)
\]

where \(\{p_i, q_i, r_i\}\) is the parameter set of this node.

Layer 5:

The single node in this layer computes the overall output as the summation of all the incoming signals.

\[
O_{5,i} = \frac{\sum w_i f_i}{\sum w_i}, \quad i=1\ldots7. \quad (7)
\]

where \(O_{5,i}\) denote the output of the ‘i’th node in layer 5.

The Adaptive Neuro-Fuzzy Inference System (ANFIS) training is done assuming that no expert available and the initial values of the membership functions parameters are equally distributed along the universe of discourse and all
consequent parts of the rule table set to zero. The ANFIS starts from zero output and during training it gradually learns the rules and functions as close to the desired controller. Thus during training the network structure update membership functions and rule base parameters according to the gradient descent update procedure.

V. TEST RESULTS

A. Buck Converter
The Neuro-fuzzy control algorithm is now verified by simulation. The simulation is performed in the time domain for the load regulation and line regulation of buck converter [10]. The specification for the 54V, 200 W bench mark converter used is given in Table I. The switching frequency of the converter is taken as 50 kHz.

Table I Converter Specifications

<table>
<thead>
<tr>
<th>Input Voltage</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>120-150V</td>
<td>1mH</td>
<td>100µF</td>
<td>11-100Ω</td>
<td>54V</td>
</tr>
</tbody>
</table>

L – Inductance, C – Capacitance, R – Load Resistance

![Fig. 5 Output voltage for a minimum line and load condition V_s=130 V, R=100Ω](image)

Fig. 5 Output voltage for a minimum line and load condition V_s=130 V, R=100Ω

![Fig. 6 Output voltage for a midrange line and load condition V_s=135 V, R=40Ω](image)

Fig. 6 Output voltage for a midrange line and load condition V_s=135 V, R=40Ω

![Fig. 7 Output voltage for a maximum line and load condition V_s=140 V, R=11Ω](image)

Fig. 7 Output voltage for a maximum line and load condition V_s=140 V, R=11Ω

The above figs. 5 - 7 demonstrate the effectiveness of the proposed Neuro-fuzzy controller for output voltage regulation in the closed loop control of buck converter.

B. Boost Converter
The Neuro-fuzzy control algorithm is now verified by simulation. The simulation is performed in time domain for load regulation and line regulation of boost converter [10]. The specification for the 25V, 50 W bench mark converter used is given in Table 2. The switching frequency of the converter is taken as 50 kHz.

Table 2 Converter Specifications

<table>
<thead>
<tr>
<th>Input Voltage</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>10-20V</td>
<td>275µH</td>
<td>540µF</td>
<td>12.5-100Ω</td>
<td>25V</td>
</tr>
<tr>
<td>50W</td>
<td></td>
<td></td>
<td>100Ω</td>
<td>50W</td>
</tr>
</tbody>
</table>

L – Inductance, C – Capacitance, R – Load Resistance

![Fig. 8 Output voltage for a minimum line and maximum load condition V_s=10 V, I_o=2A](image)

Fig. 8 Output voltage for a minimum line and maximum load condition V_s=10 V, I_o=2A

![Fig. 9 Output voltage for a midrange line and load condition V_s=15 V, I_o=1A](image)

Fig. 9 Output voltage for a midrange line and load condition V_s=15 V, I_o=1A

![Fig. 10 Output voltage for a maximum line and load condition V_s=140 V, R=11Ω](image)

Fig. 10 Output voltage for a maximum line and load condition V_s=140 V, R=11Ω

The above figs. 8 - 10 demonstrate the effectiveness of the proposed Neuro-fuzzy controller for output voltage regulation in the closed loop control of boost converter.
VI. CONCLUSION

The buck & boost converters are subjected to various disturbances of input voltage and load changes is performed to demonstrate the effectiveness of the proposed controller.

The conclusions drawn from the results are

i. The proposed novel controller gives small overshoots and has much superior performance compared to the local PI controllers.

ii. The Neuro-Fuzzy controller behaves effectively like an adaptive local tuned controller designed for each operating point and gives an improved performance compared to the conventional PI controller.

iii. The proposed Neuro-Fuzzy controller is adaptive for all the operating point as compared to Fuzzy controller.

REFERENCES


BIOGRAPHY

S. Joseph Jawhar obtained the B.E. degree from Madurai Kamaraj University, Tamilnadu, India in 1990, the M.Tech. degree from Bharthiyar University, Tamilnadu, India in 1993. He is working as part time toward the Ph.D. degree at Anna University, Chennai, Tamilnadu, India. His present research interests are Soft Computing Techniques and Power Electronics. He is now Professor and Head, Department of EEE, Noorul Islam College of Engineering, Kumaracoil, Tamilnadu, India.
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